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Ultra-Low Power Read-Decoupled SRAMs with Ultra-Low Write-Bitline Voltage Swing

Junchao Chen, Kwen-Siong Chong, Bah-Hwee Gwee

Abstract — We propose an ultra-low power memory design method based on the ultra-low ($\sim 0.2V$) write-bitline voltage swing to reduce the write power dissipation for read-decoupled SRAM (RD SRAM) cells. By keeping the write bitlines at ground level (0V) during standby and charging them to a low voltage V_L ($\sim 0.2V$) during write operations, the power dissipation for the write bitlines is greatly reduced ($((0.2V/V_{DD})^2 \times 100\%)$) due to reduced voltage swing (from $V_{DD} = 1.2V$ to $0.2V$) on the write bitlines. The proposed method is applicable to both dual-voltage and single-voltage operations. We analyze the proposed ultra-low write-bitline voltage swing method and investigate its reliability based on 10k Monte-Carlo simulations. We further verify the functionality and performance of our proposed design through measurements on the fabricated prototypes based on the 65nm CMOS process. By means of a 256x64 bit RD-SRAM memory implementation, we show that our proposed method reduces 87% write power dissipation when compared to a conventional design.

I. INTRODUCTION

Ultra-low power operation is highly desirable in power-critical portable applications such as wireless sensor networks [1] and unmanned vehicles [2] for extended battery lifespan and possibly for enabling energy-harvesting (e.g. RF energy [3], kinetic, thermal energy [4] and etc.). Of various digital building blocks, memory often dissipates a significant portion of power (and occupies large IC area). For example, in our asynchronous-logic low-power acoustic signal processor [2], the memory therein dissipates $> 60\%$ of the total power. It is well-established that dynamic power dissipation of memories is largely dominated by the charging and discharging of highly capacitive bitlines [5]. Hence, a common low power design practice for low power memory designs is to limit their bitline voltage swing – this practice has been adopted widely during read operation (by means of sense-amplifiers) but remains challenging during write operation.

The underlying challenges to enable write operation with low bitline voltage swing pertain to the reliability/noise margin issues, and in some extent, to the power-area/power-speed tradeoffs. Reported designs to enable write operation with low bitline voltage swing include designs embodying the current-mode technique [6], [7], the half- V_{DD} swing [8], the port-less approach [9], the hierarchical bitline structures [10], the charge-recycling approach [11], and the row-by-row controlled floating supplies V_{DD}/V_{SS} [5], [12]. Although the bitline voltage in the reported designs [6]-[9] was reduced, the 6-transistor

SRAMs embodied therein suffered from a reduced noise margin and read stability (especially if the bitline voltage is less than $V_{DD} - V_t$ [13]). The design with the hierarchical bitline structures [10] required local sense-amplifiers in every SRAM sub-segment, hence increasing the area overhead (and the ensuing power overhead). The designs with the charge-recycling approach undesirably reduced the speed significantly, for example up to 96% slower in the design [11]. The designs with the row-by-row controlled floating supplies [5], [12] could compromise the stability of other half-selected SRAM cells, increase power overhead, and increase the complexity of the layout implementation using thin cell layout [14], [15].

In this paper, we propose to leverage on Read-Decoupled (RD) SRAMs to realize memories with ultra-low write-bitline voltage swing to reduce write power dissipation. The RD SRAMs [16]-[19], whose write-access and read-access transistors are not shared, are advantageous to eliminate the disturbance during the read operation, hence enabling a low write-bitline voltage swing without compromising the read stability. Particularly, by discharging the write-bitlines (of the RD-SRAMs) to ground level during standby and charging them to a low voltage V_L ($V_L < \text{the nominal supply } V_{DD}$) during the write operation, the power dissipation for the write operation is greatly reduced.

There are several novelties in our proposed work. First, we propose two implementation approaches – dual-voltage and single-voltage – for our RD SRAMs. The dual-voltage approach employs a secondary lower supply V_L to partially charge the write-bitline (in each column during the write operation) to form a voltage difference, and the accessed RD-SRAM cell, powered by the primary voltage V_{DD} , then senses and amplifies the voltage difference to store the datum correctly and locally. Conversely, the single-voltage approach employs a single voltage source where a controlled pulse-width circuit is used to partially charge the write-bitline same as the dual-voltage approach. In both approaches, their associated overheads are negligible. We also show that the dual-voltage approach is more power-efficient than the single-voltage approach. Second, based on the standard 8-transistor (8-T) RD SRAM cell [15] and on the basis of 10k Monte-Carlo simulations, we investigate the stability of the RD SRAM cell with respect to the threshold voltage of the transistors, the sizing of the transistors, and the write-bitline voltage effect. Third, by means of a 256×64-bit memory example, we made a deliberate effort to design, fabricate and compare both our proposed RD SRAM design (with ultra-low write-bitline voltage swing embodying the dual-voltage approach) and the conventional RD SRAM design. Both designs are realized using the same 65nm CMOS process and the same thin-cell layout technique [14]. We show that our proposed design ($V_L=0.2V$, $V_{DD}=1.2V$ @ 100MHz) dissipates 87% lower write power than the conventional design ($V_{DD}=1.2V$ @ 100MHz) with only slight increase in IC area. Our proposed design is also functional by varying $V_{DD} = 0.8V$ to $1.2V$, and is suitable in the targeted low power acoustic signal processor design [2] that exploits the wide-operating lifespan (~95%) of a battery.

The organization of the paper is as follows. Section II describes the proposed ultra-low write-bitline voltage swing approaches for RD SRAM designs. Section III analyzes the write operation of the proposed approaches. Section IV shows the 10k Monte-Carlo simulation results. Section V presents the other simulation and measurement results. Section VI draws the conclusion.

II. ULTRA-LOW WRITE-BITLINE VOTAGE SWING

We now describe two implementations to realize the ultra-low power RD SRAMs with ultra-low write-bitline voltage swing. The first implementation pertains to the dual-voltage approach, and the other to the single-voltage approach.

(A) Dual-Voltage Approach

Fig. 1 depicts the block diagram of a 256×64-bit RD SRAM design with ultra-low write-bitline voltage swing. The SRAM cell used is an 8-T RD SRAM cell [15] (shown in the dotted oval shape) whose write-bitlines (BL_x and BLB_x) and the read-bitline (RBL_x) are separated. In Fig. 1, the subscript x denotes the bit position from 0 to 63, and the subscript y the row position from 0 to 255. The Dual-Voltage block provides two supply voltages, V_L and V_{DD} , where $V_L < V_{DD}$ (for low power purpose). The V_L supplies power to charge the write-bitlines, BL_x or BLB_x . The V_{DD} supplies power to the rest of the blocks. The Clock and Controllers control the NOR-NAND address decoder that asserts the read-wordline (RWL_y) and write-wordline (WWL_y). The Clock and Controllers control the write and read circuitries in the Dual-Voltage block, and enable the transfer of the output via the Output Buffer block (during read operations).

The write operation of the RD SRAM design is as follows. Initially, both the write-bitlines (BL_x and BLB_x) are discharged to ground level of 0 V. During a write operation, depending on the input data, one of the write-bitlines (either BL_x or BLB_x) remains discharged to ground, and the other one is charged to V_L and then left floating. WWL_y is also asserted. Subsequently, two phases of operation, as shown in Fig. 2, will be performed in the accessed 8T RD SRAM cell; in Fig. 2, we assume that the prevailing stored datum $Q_x = '0'$ ($QB_x = '1' @ V_{DD}$), and the next written input is '1'. In Phase I, QB_x will be discharged from V_{DD} close to ground. Meanwhile, Q_x is charged from '0' to V_L , and continually increasing due to the feedback mechanism of the cross-coupled inverters (see the RD SRAM cell in Fig. 1). A voltage difference (between Q_x and QB_x) is then obtained, and when sufficient, Q_x will be further amplified to a full voltage swing in Phase II (due to the positive feedback mechanism in the cross-coupled inverters [20]). The datum is hence successfully written to the memory. We remark that the WWL_y needs to generate a short pulse to prevent an unnecessary charging of bitlines (after the write operation is completed), hence minimizing any unnecessary power dissipation.

Fig. 1 A 256×64-bit RD SRAM memory design with ultra-low write-bitline voltage swing; 8-T RD SRAM cells are used

Fig. 2 Write Operation: Q_x is switched from '0' to '1' in two phases

The read operation of the RD SRAM design operates same as the conventional designs. Initially, the read-bitlines (RBL_y) are pre-charged to V_{DD} . During a read operation where RWL_y is asserted and the datum QB_x in the RD SRAM cell asserts/negates the read transistor N5 (see Fig. 1) so that the datum is eventually read out (via the Output Buffer block).

From a low power perspective, as the capacitance on the write-bitlines is large, the low voltage swing on the write-bitlines efficiently reduces write power dissipation. Although the full voltage swing still exists within the RD SRAM cells locally, the capacitance of the RD SRAM cells is much smaller and is insignificant to the overall power dissipation. When compared to the reported designs (having a full voltage swing write-bitlines), our proposed dual-voltage approach will have a write-bitline power reduction of $(V_{DD}/V_L)^2$ times.

(B) Single-Voltage Approach

If the dual voltages are not available, the RD SRAM design can be re-designed using only one V_{DD} . In this single-voltage approach, the Single-Voltage block, as shown in Fig. 3, charges either BL_x or BLB_x . This is done as follows. When the $PreC$ signal is activated, a *Pulse* signal will be generated by a Digitally Controlled Pulse width (DCP) circuit. The *Pulse* signal, with the NAND gates, in turn asserts one of the PMOS pre-charge transistors to charge one of the write-bitlines to a voltage V_L . During the charging process, the higher the voltage level of V_L , the higher the wastage of power. Conversely, the lower the voltage level of V_L , the higher chance of an unsuccessful write operation. The duration of the charging process can be estimated through the time-constant of the write-bitline capacitance and the resistance of the PMOS pre-charge transistor. As the pulse width of the *Pulse* signal and driving strength of the PMOS precharge transistor may be varied due to Process-Voltage-Temperature (PVT) variations. The DCP circuit is designed to generate a tunable pulsewidth such that, under any PVT variations, the bitlines will always be precharged to V_L .

The write and read operations are the same as that described earlier in Section II.A. When compared to the reported designs (having a full voltage swing write-bitlines), our proposed single-voltage approach will have a write-bitline power reduction of (V_{DD}/V_L) time.

Fig. 3 The Single-Voltage block (showing for one column)

III. ANALYSIS OF WRITE OPERATION

It is prudent to analyze the reliability of the write operation in the RD SRAM cell in view of the ultra-low write-bitline voltage swing. Assuming the same case study where the prevailing stored datum Q_x is '0' ($QB_x = '1'$) in the RD SRAM cell (refer to Fig. 1), and the next written datum is '1' for the write operation, we now further analyze the write operation of the RD SRAM cell.

During the write operation, BL_x is raised to V_L , BLB_x is kept at 0V, and WWL_y is then raised up to V_{DD} , the N4 transistor will try to discharge QB_x to ground and the N3 transistor will try to charge Q_x to V_L . Because the N4 transistor has much larger driving strength than the P2 transistor, QB_x will be at very low voltage. Meanwhile, Q_x will be at a very low voltage. After QB_x is pulled down to a low voltage, Q_x will begin to rise. As Q_x increases, QB_x will be pulled to an even lower voltage level. As QB_x becomes even lower, Q_x will become even higher. This feedback continues and will settle Q_x and QB_x to a nearly steady value quickly, and a voltage difference between Q_x and QB_x is then formed in this phase – Phase I (see Fig. 2). An interesting study here is, during the Phase I, how much the voltage difference is formed by taking consideration into the characteristics/variations of the transistors therein. The larger the voltage difference formed, the better the robustness of the RD SRAM cell as the later amplification process can commence easily and the datum will be written into the RD SRAM cell correctly.

Consider the Phase I, we can assume both the P1 and P2 transistors operate in saturation region, both the N3 and N4 transistors in triode region, and both the N1 and N2 transistors in the sub-threshold region. We first plot Fig. 4 the voltage difference ($V_Q - V_{QB}$) at the end of Phase I against the threshold voltage variations of the N3, N4, P1 and P2 transistors (@ $V_L = 0.2V$, $V_{DD} = 1.2V$), and remark the following. First, if either the N3 transistor or the P2 transistor becomes weak (i.e. with an increased threshold voltage), the voltage difference formed will increase, enabling the later amplification process (in the Phase II) easily. Conversely, if either the N4 transistor or the P1 transistor becomes weak, the voltage difference formed will decrease, impeding the later amplification process. Second, the P2 and N4 transistors are somewhat not critical to change Q_x from '0' to '1'. Third, a weak P1 significantly reduce the voltage difference.

Fig. 4 Phase I: Voltage difference, $V_Q - V_{QB}$, against the variation of the transistors N3, N4, P1 and P2

The sizing of the N3, N4, P1 and P2 transistors also plays a role in determining the voltage difference formed in the Phase I. Assuming at the worst-case scenario where the N3 and P2 transistors are strong by shifting ΔV_t by $-0.2V$ and $+0.2V$ respectively, and the N4 and P1 are weak by shifting ΔV_t by $+0.2V$ and $-0.2V$ respectively, we plot in Fig. 5 the voltage difference against the sizing ratio $\beta ((W/L)_{N3,N4}/(W/L)_{P1,P2})$ both in the nominal case and the worst case @ $V_L = 0.2V$, $V_{DD} = 1.2V$. As expected, at the nominal case, increasing β will reduce the voltage difference formed as the N3 transistor effectively becomes stronger. However, at the worst case condition, the voltage difference formed is smaller than that in the nominal case. Increasing β will increase the voltage difference formed. In view of this, to increase the yield at the worst case condition, β could be increased.

Fig. 5 Phase I: Voltage difference in the normal and worst case at various β

We further plot in Fig. 6 the voltage difference against various V_L both in the nominal case and the worst-case @ $\beta = 1$, $V_{DD}=1.2V$. We remark the following. First, as expected, the higher the V_L voltage, the larger the voltage difference formed. Second, in the worst-case condition, when the $V_L < 0.18V$, the voltage difference is negative, and the RD SRAM cell will fail as the amplification process cannot take place.

Fig. 6 Phase I: Voltage difference in the normal and worst case at various V_L

IV. 10K MONTE-CARLO SIMULATION RESULTS

The write ability of the proposed near-ground bitlines write method are verified by 10k Monte-Carlo simulations including both global and local variations provided by the foundry. The simulated threshold voltages for NMOS transistors vary from 0.345V to 0.720V and the threshold voltages for PMOS transistors vary from 0.385V to 0.636V.

As shown in Fig. 7 (a) the number of write failures by using a fixed V_{DD} is lower than that of using floating V_{DD} [5] [12]. Some of RD-SRAMs are asymmetrical, e.g. single-ended 8T. Asymmetric memory cell will face more failure in the Phase II due to the asymmetric capacitance in nodes Q and QB . QB has higher capacitance than Q because QB is connected to the gate of N5 for read operation. At the beginning of the Phase II, Q and QB will initially be set at low voltages and both their voltages will begin to increase. The voltage at Q will increase faster than the voltage at QB because of low capacitance. This makes the write access with input of '1' easier than with input of '0' for single-ended 8T. As shown in Fig. 7 (b), the number of write failure is much higher for the case where input is '0' and Q is '1' (8TR) than the case where input is '1' and Q is '0' (8TL).

The number of failures versus bitline differential voltage with conventional write method is also shown in Fig. 7 (c) for comparison purpose. It requires a bitline differential voltage of 0.93V for zero failure compared to 0.15V in proposed method.

Fig. 7 10k Monte-Carlo simulation results on number of failures for (a) Floating V_{DD} and Fixed V_{DD} , (b) 8TR, 6T and 8TL SRAM designs, and (c) Conventional Write method

V. IMPLEMENTATION AND RESULTS

On the basis of pre-layout simulations, we simulated the write power dissipation of the conventional memory design, and our memory designs embodying the single-voltage and dual-voltage approaches respectively, all based on a 65nm CMOS process. Fig. 8 shows the comparison of the write power dissipation (@ 100% data change) of these designs with different wordlengths. From, Fig. 8, it is apparent that in the conventional design, the power dissipation due to the write-bitlines dominates the overall power. However, in the designs embodying our single-voltage and dual-voltage approaches, the power dissipation due to the write-bitlines reduces significantly. The power reduction will be even more significant if the wordlength of the memory is larger. Particularly, our 8-bit, 16-bit, 32-bit and 64-bit designs embodying the single-voltage approach dissipate 59%, 67%, 72% and 75% lower power than the conventional designs respectively. Our 8-bit, 16-bit, 32-bit and 64-bit designs embodying the dual-voltage approach dissipate even lower power, by 69%, 78%, 84% and 87% lower power than the conventional designs respectively.

Fig. 8 Write power comparison according to word length

To demonstrate the power-efficiency in prototypes, we fabricate a 256×64-bit memory design embodying the dual-voltage approach and the conventional 256×64-bit memory design; their IC microphotographs are depicted in Fig. 9. Both designs embody the same RD SRAM cells. To minimize the area, we adopt the thin-cell layout technique to realize the RD SRAM cell. Fig. 10 (a) depicts simplified transistor floorplan of an RD SRAM cell, and Fig. 10 (b) depicts the floorplan, with an example of three RD SRAM cells, to show how these RD SRAM cells are integrated together. A pearl-script was written to floorplan the various sub-blocks (in the both the conventional and our memory designs) in the Cadence Virtuoso platform.

Fig. 9 The IC microphotograph of two 256×64-bit SRAMs based on the conventional and our dual-voltage approaches respectively

Fig. 10 Floorplan: (a) a 8-T thin cell, and (b) three 8-T thin cells in a column

Fig. 11 shows the pass/fail testing among all the 13 packaged chips of our proposed design by varying the write-bitline voltage of V_L from 0.01V to 0.2V (and $V_{DD} = 1.2V$). All the chips are fully functional when $V_L \geq 0.15V$. In our prototypes, the built-in testing circuits embodied in the fabricated chip can only support a programmable clock up to 500MHz. For ease of testing, we set the clock frequency to 100MHz for power measurement. Fig. 12 depicts measured power dissipations for the conventional design from $V_{DD} = 0.8V$ to 1.2V and for the proposed design from $V_{DD} = 0.8V$ to 1.2V, and $V_L = 0.2V$. Both V_{DD} and V_L are external supplies. From $V_{DD} = 0.8V$ to 1.2V, on average, the proposed design dissipates ~85% lower power than the reported design. Table I summarizes the characteristics of the proposed and conventional designs.

Fig. 11 Measured minimum V_L for proposed design for zero write failures

Fig. 12 Power dissipation of two 256×64-bit SRAMs based on the conventional and our dual-voltage approaches respectively at room temperature

Table I Comparison between conventional and proposed design

	Process	Size ($\mu\text{m} \times \mu\text{m}$)	Test Speed	Write Power
Conventional	65nm	220x190	100MHz	720uW
Proposed	65mn	220x201	100MHz	122uW

VI. CONCLUSIONS

An ultra-low power ultra-low write-bitline voltage swing method for RD-SRAMs (whose write bitlines and read bitlines are separated) has been proposed. The stability of the write methods has been analyzed through 10k Monte-Carlo simulations. The functionality and performance of our design has been verified through simulations and measurements in 65nm STM process. The proposed method achieves more than 80% write power reduction for a 256×64 Kb SRAM memory design.

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