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Design of a Time-Mode Analog-to-Digital Converter Utilizing a Time-to-Digital Converter That Is Scalable with CMOS Technology

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirements for the degree of
Doctor of Philosophy

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

26 August 2019

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Teh Jian Sen

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

26 August 2019

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Assoc Prof Liter Siek

Authorship Attribution Statement

This thesis contains material from 5 papers to be submitted, submitted to, or published in the following peer-reviewed conferences or journals in which I am listed as an author.

Section 3.1 of Chapter 3 is published as J. S. Teh and L. Siek, “Novel Edge Comparator with Input Time Hysteresis for Improved Edges Arbitration,” *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018, pp. 1-5.

The contributions of the co-authors are as follows:

- Assoc Prof Siek supervised the project developments, provided guidance during the project, and reviewed the manuscript drafts.
- I prepared the manuscript drafts.
- I designed and analyzed the proposed edge comparator. I also designed a printed circuit board (PCB) for the measurement of the test chips of this proposed edge comparator.
- I measured the fabricated test chips of this proposed edge comparator, and analyzed the collected data.

Section 3.2 of Chapter 3 is submitted as J. S. Teh, A. R. Palaniappan and L. Siek, “Analysis of Negative Skewed Delay Scheme for Ring Oscillator With Multiphase Outputs,” to *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*.

The contributions of the co-authors are as follows:

- Assoc Prof Siek supervised the project developments, provided guidance during the project, and reviewed the manuscript drafts.
- I prepared the manuscript drafts. The manuscript drafts are revised with Mr A. R. Palaniappan.

- I analyzed the negative skewed ring oscillator and designed a test chip for the verification of this analysis. I also measured the fabricated test chips and analyzed the collected data.
- Mr A. R. Palaniappan assisted in the phase noise analysis. He also helped to collect and analyze the phase noise measurement data from the fabricated test chips.

Section 4.1 of Chapter 4 is submitted as J. S. Teh and L. Siek, “A 12-bit Branching Time-to-Digital Converter With Power Saving Features and Digital Based Resolution Tuning for PVT Variations,” to *Analog Integrated Circuits and Signal Processing*.

The contributions of the co-authors are as follows:

- Assoc Prof Siek supervised the project developments, provided guidance during the project, and reviewed the manuscript drafts.
- I prepared the manuscript drafts.
- I designed and analyzed the proposed branching Time-to-Digital converter (TDC). I also designed a PCB for the measurement of the test chips of this proposed branching TDC.
- I measured the fabricated test chips of this proposed branching TDC, and analyzed the collected data.

Section 4.2 of Chapter 4 is published as J. S. Teh, L. Siek, A. M. Alonso, A. Firdauzi and A. Matsuzawa, “A 14-b, 850fs Fully Synthesizable Stochastic-Based Branching Time-to-Digital Converter in 65nm CMOS,” *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018, pp. 1-5.

The contributions of the co-authors are as follows:

- Assoc Prof Siek and Prof Matsuzawa supervised the project developments, provided guidance during the project, and reviewed the manuscript drafts.
- I prepared the manuscript drafts.

- I designed and analyzed the proposed stochastic-based branching TDC. Mr A. M. Alonso and Mr A. Firdauzi also assisted in the design of this proposed stochastic-based branching TDC.
- Together with Mr A. M. Alonso, we fully synthesized the layout of this proposed stochastic-based branching TDC.
- I also simulated this proposed stochastic-based branching TDC, and analyzed the simulated data.

Chapter 5 is to be submitted as J. S. Teh, L. Siek and H. Graeb, “An 8-b Time-Mode ADC with a Time Amplifying VCO-based VTC and a Stochastic-Based Branching TDC in 40nm CMOS,” to a peer-reviewed journal.

The contributions of the co-authors are as follows:

- Assoc Prof Siek and Prof Gräb are supervising the project developments, providing guidance for the project, and will be reviewing the manuscript drafts.
- I will be preparing the manuscript drafts.
- I designed and analyzed the proposed time-mode Analog-to-Digital converter (ADC). I also designed a PCB for the measurement of the test chips of this proposed time-mode ADC.
- I measured the fabricated test chips of this proposed time-mode ADC, and analyzed the collected data.

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Date

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To my dearest family,

Abstract

Aggressive scaling of CMOS technology into deep sub-micron nodes enables analog front-end circuitries to be integrated with digital back-end processors, forming System-on-Chip (SoC) solutions. However, the reduction of supply headroom available to circuits and other impairments resulting from device scaling limit the scalability of conventional front-end Analog-to-Digital converters (ADC).

Time-mode ADC, comprising of a Voltage-to-Time converter (VTC) and a Time-to-Digital converter (TDC), is proposed as a solution for enabling ADCs to scale with advancing CMOS technology. Both the VTC and TDC can be realized using highly digital building blocks, circumventing the reduced supply headroom issue and benefiting from the advantages of device scaling. This research aims to design and implement a time-mode ADC that scales with advancing CMOS technology.

In the research into TDCs, two sub-blocks of TDCs are investigated. Firstly, a novel edge comparator that incorporates an input time hysteresis window of about 55 fs is proposed. This edge comparator allows a TDC to be more robust against noise and jitters in repeated measurements. Secondly, ring oscillators employing the negative skewed delay scheme are analyzed to understand the mechanism behind this scheme. Therefore, an optimum configuration of negative skewed ring oscillator can be chosen for the TDC implementation. Both the proposed edge comparator and the analysis of negative skewed ring oscillators are verified using prototype chips fabricated in a standard 0.18 μm CMOS technology.

In addition, a novel branching TDC architecture is proposed. The branching technique interpolates between the phases of a core ring oscillator used by the TDC. Hence, the TDC time resolution can be finer than the tap-to-tap delay of the ring oscillator. The branching technique allows two phase interpolation methods to be realized. Namely, through deterministic or stochastic positioning of the interpolating edges. The former and latter methods are demonstrated by a 12-bit

branching TDC prototype chip fabricated in a standard 40 nm CMOS technology, and a 14-bit fully synthesizable stochastic-based branching TDC simulation in a standard 65 nm CMOS technology, respectively. The former and latter TDCs achieve interpolation factors of 4 and 85.3, respectively.

Finally, an 8-bit highly digital time-mode ADC is proposed. It comprises of a novel voltage-controlled oscillator (VCO)-based VTC with time interval amplification capability and a stochastic-based branching TDC. The proposed time-mode ADC accepts rail-to-rail inputs, not limited by the reduced supply headroom issue. It also does not require any voltage references or amplifiers. Hence, it is able to scale well with advancing CMOS technology. The proposed time-mode ADC is verified using prototype chip fabricated in a standard 40 nm CMOS technology. At a sampling rate of 15 MS/s, it achieves a signal-to-noise and distortion ratio (SNDR) of 39.9 dB and a Walden figure of merit of 464 fJ/conv.-step.

Table of Contents

Acknowledgements	xi
Abstract	xv
List of Figures	xix
List of Tables	xxvii
Symbols and Acronyms	xxix
1 Introduction	1
1.1 Background	1
1.2 Motivation	4
1.3 Research Objectives	6
1.4 Organization of Thesis	7
2 Overview of Time-Mode ADCs	9
2.1 Voltage-to-Time Converter	9
2.2 Time-to-Digital Converter	17
2.3 Gap in the Literature	30
3 TDC Building Blocks	35
3.1 Edge Comparator With Time Hysteresis	36
3.2 Analysis of Negative Skewed Ring Oscillators	54
3.3 Summary	89
4 Branching TDC Architecture	91
4.1 12-bit Branching TDC	92
4.2 14-bit Stochastic-Based Branching TDC	133
4.3 Summary	162
5 Scalable Time-Mode ADC	165
5.1 Track and Hold	167
5.2 VCO-Based VTC with Time Amplification	173

5.3	13-bit Stochastic-Based Branching TDC	186
5.4	Back-End LUT Based Calibration	201
5.5	Overall Time-Mode ADC Operation	202
5.6	Measurement Results	204
5.7	Summary	223
6	Conclusion and Outlook	225
6.1	Conclusion	225
6.2	Prospects of Time-Mode ADC	228
6.3	Recommendations for Future Works	229
	List of Author's Publications	231
	Bibliography	233

List of Figures

1.1	Simplified analog front-end representation. The ADC converts the pre-conditioned analog signals into their digital representations. . .	2
1.2	V_{DD} and V_{th} projections by the International Roadmap for Devices and Systems (IRDS). V_{th} takes up to 35% of V_{DD}	2
1.3	Schematic of a simple differential common-source amplifier with illustration of its input voltage range limit.	3
1.4	Digital stage delay and dynamic power at 1 GHz projections by IRDS. Both stage delay and dynamic power are decreasing as CMOS technology scales.	4
1.5	Simplified block diagram of a time-mode ADC. It comprises of a VTC, a TDC, and an overall control block.	6
1.6	Overview of the contributions of this thesis. The specific positions of the contributions within a time-mode ADC are illustrated.	8
2.1	Simplified schematic of a linear capacitor discharge VTC. The input voltage is converted into the discharge time of the capacitor.	10
2.2	Propagation delay of an inverter.	11
2.3	Three methods of modulating the propagation delay of an inverter. (A) Through the supply. (B) Current starving with NMOS in cascode. (C) Current starving with NMOS in parallel.	14
2.4	Delay line TDC. The input time difference is quantized in terms of the propagation delay of the unit delay stage. (A) Schematic. (B) Timing diagram.	18
2.5	Vernier delay line TDC. The input time difference is quantized in terms of the differential delay between the fast and slow stages. . .	20
2.6	Parallel delay lines TDC. The sub-delay lines interpolate the main delay line to achieve sub-gate delay TDC time resolution of τ_{stage}/P . (A) Schematic. (B) Timing diagram.	22
2.7	Parallel sampling TDC. The delay line is interpolated by sampling it at τ_{stage}/P instances apart.	23
2.8	Stochastic phase interpolation TDC. The input clock is interpolated by the stochastic positioning of the buffered clocks. Redundancy through LSB truncation is employed. (A) Schematic. (B) Timing diagram.	24

2.9	Normalized overall PDF of rising edges collected with respect to n for $\tau_{stage,nom} = 50$ ps, $\sigma_{mis} = 0.05\tau_{stage,nom}$, and $\sigma_{jit} = 0.005\tau_{stage}[i]$. It converges into an uniform distribution as n increases.	26
2.10	Ring oscillator based TDC. The input time difference is quantized in terms of the phase change of the ring oscillator. (A) Schematic. (B) Timing diagram.	28
2.11	General block diagram of a coarse-fine TDC. The input time difference is first quantized by the coarse TDC, producing a residue that is further quantized by the fine TDC.	29
2.12	Effective number of bits (ENOB), sampling rates, and scalabilities of recent time-mode ADCs published in the literature. There is limited research for low to moderate speed time-mode ADCs with more than 7-bit ENOB.	32
3.1	Conventional SAFF edge comparator. It is a modification from the standard StrongARM latch, allowing it to be self-clocked. The OR gate is implemented with a balanced structure. (A) Schematic. (B) Timing diagram.	37
3.2	Proposed edge comparator with input time hysteresis. Input time hysteresis is achieved by connecting node Q and node Qb directly to a SR latch, and the addition of M11 and M12 negative feedback transistors.	39
3.3	Transistor level schematic of the SR latch formed by cross-coupled NAND gates. Parasitic capacitors associated with node Q and node Qb are also shown. The inputs to the transistors are connected by node names.	42
3.4	Simulation of the parasitic capacitance contributed by the NAND gates to node Q and node Qb before the onset of positive feedback. $C_{Qb,NAND}$ is smaller than $C_{Q,NAND}$ during this period.	43
3.5	Simulation and timing diagram illustrating the oscillation behavior of the edge comparator output due to the SR latch memory effect.	44
3.6	Negative feedback NMOS transistor is modeled as a voltage controlled resistor degenerating the source of the NMOS in its inverter.	45
3.7	Plot of $V_{o,inv}$ against $V_{th,inv}$ using Equation (3.7) and simulation. There is an inverse relationship between the threshold voltage and output voltage of the inverter.	46
3.8	Exaggerated timing diagram illustrating the comparison result evaluation process of the proposed edge comparator.	47
3.9	Small signal differential model of the proposed edge comparator.	48
3.10	Chip micrograph of the conventional and proposed edge comparators. The core of the proposed edge comparator, highlighted in the center, occupies an area of 0.026×0.014 mm ²	49
3.11	Method to create an input time ramp in simulations. It can be created using two clocks with a slight difference in frequencies.	50

3.12	Simulation results of the time hysteresis sweep applied to the proposed edge comparator. A symmetrical input time hysteresis window of 55 fs is achieved.	50
3.13	Measurement setup. A single 100 MHz source is fed to separate chains of inverters. A small sine input time difference is created by modulating the supply of one of the inverters with a small 10 kHz sine wave.	51
3.14	Measurement result of the SR latch memory effect. The output of the edge comparator oscillates at the zero-crossing regions of V_{DDsin} since the input time differences created are too small to overcome ΔV_{SD}	52
3.15	Measurement result of the proposed edge comparator. Input time hysteresis effect is verified since the output of the edge comparator only transits once after the zero-crossing points of V_{DDsin} despite V_{DDsin} being noisy.	53
3.16	Simulation of the time required for the conventional and proposed edge comparators to resolve a decision while working in the metastability region. The latter takes about twice as long to resolve its decision.	55
3.17	(A) Negative skewed inverter stage. (B) $N = 11$, $S = 9$ NSRO. Each stage is defined by its output node. The PMOS are connected by node names. (C) Its simulated oscillation waveform and that of its conventional. f_S has increased by 89 %, even though τ_{dfs} and τ_{drs} have also increased.	57
3.18	(A) Proposed sequence tree. It represents the propagation relationship between the stages of an NSRO. (B) Sequence tree of an $N = 11$, $S = 9$ NSRO. Arrows are removed for compactness. (C) Sequence tree of an $N = 9$, $S = 3$ NSRO. There are repetitions in the same level.	62
3.19	Simulated oscillation waveforms of a conventional 5-stage ring oscillator, Stage 1 and Stage 6 outputs of an $N = 10$, $S = 5$ NSRO. They are oscillating with the same frequency and phase.	63
3.20	(A) Sequence tree and (B) simulated oscillation waveform of an $N = 11$, $S = 5$ NSRO. The single edge sequence of this NSRO (SQ_{11}^5) can be derived from any straight column in its sequence tree.	65
3.21	Timing diagram illustrating two separate single edge sequences occurring simultaneously in an $N = 11$, $S = 9$ NSRO. The two single edge sequences increase the oscillation frequency of this NSRO by a factor of 2.	66
3.22	Timing diagram illustrating three separate single edge sequences occurring simultaneously in an odd N , $S = N - 4$ NSRO. The three single edge sequences increase the oscillation frequency of this NSRO by a factor of 3.	68

3.23	Timing diagram illustrating three separate single edge sequences occurring simultaneously in an even N -stage NSRO with optimum S . The three single edge sequences increase the oscillation frequency by a factor of 3.	70
3.24	(A) Sequence tree and (B) simulated oscillation waveform of an $N = 10$, $S = 3$ NSRO. Level N of the sequence tree shows the overall phase sequence of this NSRO as described by Equation (3.30). . . .	71
3.25	Small signal model of an inverter stage in an NSRO.	73
3.26	Normalized eigenvalues of an $N = 16$, $S = 7$ NSRO. Each complex eigenvalues pair in the RHP of the complex plane corresponds to a possible mode of oscillation for this NSRO at steady state.	75
3.27	Single differential stage schematics of (A) source-coupled logic (SCL) type and (B) saturated delay (SD) type. (C) Schematic of an $N = 5$, $S = 3$ differential NSRO.	76
3.28	Micrograph of test chip with 28 different configurations of single-ended (SE) and differential NSROs in 0.18 μm /1.8 V CMOS technology.	81
3.29	(A) Calculated and simulated f_S of SE NSROs for $N = 7$ to 22 with varying S configurations such that $k_{osc} = 2$ or 3. They are in good agreement. (B) Measured f_S/f_C of SE NSROs for $N = 9, 10, 13$ and 16.	82
3.30	Measured PDPs of SE conventional ring oscillators and NSROs. Negative skewed even N configurations consume least additional power as compared to conventional ring oscillators.	83
3.31	Measured f_S/f_C of differential NSROs. $N = 11, 12, 14$, & 15 differential NSROs and $N = 17$ to 20 differential NSROs are built using SCL and SD stages, respectively.	84
3.32	Measured PDPs of SD differential NSROs. Their conventional cases are also plotted. Negative skewed even N cases have the best PDP performances.	85
4.1	Branching phase interpolation principle. The branching delay lines enable $4\times$ phase interpolation between the tap-to-tap phases of the ring oscillator to be achieved. (A) Simplified circuit schematic. (B) Timing diagram.	94
4.2	Illustration of the first edge produced by the ring oscillator propagating through and reaching the ends of the first two branching delay lines that it is fed into.	99
4.3	Block diagram of the 12-bit BTDC prototype. It composes of a 6-bit ring oscillator based coarse TDC and a 6-bit branching fine TDC. . .	100
4.4	Schematics of (A) branching GRO, (B) a GRO delay stage, and (C) a branching GDL delay stage. The GRO is a gated $N = 16$, $S = 7$ NSRO. Digital coarse delay tuning through the header PMOS and footer NMOS transistors, and digital fine delay tuning through the output capacitor bank.	103

4.5	Simplified schematic illustrating the fixed offset capacitors that are added along the branching GDLs to fine tune the positions of the interpolating rising edges.	104
4.6	Measured coarse and fine delay tuning responses of the GRO stage delay (τ_{GRO}). (A) Individual and (B) combined tuning response. . .	107
4.7	(A) Example of a conventional 5-stage ring oscillator with bridging capacitors connected to back-to-back rising edges. (B) Model for a first-order approximation of the effective output capacitance ($C_{O,B}$). . .	108
4.8	(A) Timing Diagram of spatial mismatch filtering. The skewed rising edge is shifted back to its ideal position. (B) Simplified model in Laplace domain of a GRO delay stage output node with bridging capacitors.	110
4.9	Schematic of a gated inverters based sampler. These samplers extract the phase of the branching GRO by sampling the held voltages of its delay stages. Two separate paths are used for the START and STOP sampling.	112
4.10	Simplified timing diagram of the BTDC prototype.	114
4.11	Simplified schematic of the pulse generator. It is a modified phase-frequency detector where buffers, OR and AND gates are added. . .	116
4.12	Chip micrograph of the BTDC prototype. It occupies an area of $0.25 \times 0.17 \text{ mm}^2$	118
4.13	Measurement setup for measuring the DNL, INL, and SSP of the BTDC prototype.	119
4.14	Measured (A) DNL and (B) INL of the BTDC prototype. It achieves a maximum/minimum DNL and INL of 1.30 LSB/ -0.93 LSB and 3.43 LSB/ -3.61 LSB, respectively. The non-linearity periodicity of the BTDC prototype can be observed from the INL plot.	120
4.15	(A) Measured SSP against output code of the BTDC prototype with and without averaging applied. Within 12-bit range, SSPs of 0.75 LSB and 0.43 LSB, respectively, are obtained. (B) SSP histograms for mean output codes of 185 and 2881.	121
4.16	SSP histograms for mean output code of 13932.	122
4.17	Measured (A) mean output codes and (B) SSPs of the BTDC prototype for a fixed input time difference over a temperature range of -40°C to 125°C . The mean output codes variation, and hence, the TDC time resolution variation is reduced by 92.3 %.	125
4.18	Illustration of the mismatch in rise times between the GRO delay stage and the branching GDLs delay stage. This mismatch degrades the linearity of the BTDC prototype.	131
4.19	(A) Architecture of the enable signals for the GRO and branching GDLs in this BTDC prototype. Different loadings result in a mismatch between disabling instants during phase sampling. (B) Proposed improved version.	132

4.20	Timing diagram of stochastic-based branching phase interpolation principle. An oscillation period of the ring oscillator is stochastically interpolated by 2^n rising edges. Redundancy through truncation is used to improve linearity.	136
4.21	Block diagram of the 14-bit SBTDC-I prototype. It composes of a 6-bit ring oscillator based coarse TDC and an 8-bit stochastic-based branching fine TDC.	139
4.22	Schematic of the branching GROs. There are a total of 4107 unit NAND gates, producing the 2^{12} rising edges for the stochastic phase interpolation operation.	141
4.23	Simple digital based foreground calibration method for the SBTDC-I prototype. The oscillation period of the main GRO is measured by counting the number of its cycles within a reference time period. . .	143
4.24	Simplified schematic and timing diagram of the proposed residue generator. The STOP signal will be selectively delayed depending on the arbitration result of the D flip-flop.	146
4.25	Violation of the timing margin for the fixed time delay. The delayed STOP signal can occur too close to the next main GRO rising edge if the fixed time delay is too small or too large.	148
4.26	Simplified schematic of digital synchronizer circuit that adds a time offset of t_{GRO} into the residue time generated. Reset signals are not shown.	149
4.27	Simplified timing diagram of the SBTDC-I prototype.	150
4.28	Flowchart of the calibration scheme for the SBTDC-I prototype. . .	155
4.29	Chip layout of the SBTDC-I prototype. It occupies an area of $0.79 \times 0.28 \text{ mm}^2$	155
4.30	Simulated DNL and INL of the scaled-down SBTDC-I PoC across temperature corners. It achieves a maximum/minimum DNL and INL of 0.34 LSB/−0.38 LSB and 0.63 LSB/−0.40 LSB, respectively. .	156
4.31	Simulated SSP results of the scaled-down SBTDC-I PoC due to process variation. It achieves SSPs of 1.00 LSB and 1.11 LSB for fixed input time differences of 268 ps and 385 ps, respectively.	158
4.32	Simulated DNL and INL of the full scale 14-bit SBTDC-I prototype. It achieves an estimated maximum/minimum DNL and INL of 0.27 LSB/−0.11 LSB and 2.94 LSB/−1.16 LSB, respectively. . .	159
5.1	Block diagram of the proposed 8-bit highly digital time-mode ADC. . .	166
5.2	The track and hold circuit. It directly connects to the VTC without buffer. The sampling switch is a bootstrapped switch. Bottom plate sampling principle is utilized. (A) Simplified schematic. (B) Timing diagram.	168
5.3	Schematic of the conventional bootstrapping circuit.	169
5.4	Post-layout simulated performances of the track and hold circuit. (A) SNDR, (B) tracking gain, and (C) total change in held sampled voltage as functions of input frequency.	174

5.5	Schematic of the proposed VCO-based VTC with $8\times$ time interval amplification. Voltage-to-time conversion and time interval amplification are achieved using GRO based VCOs and 3-bit counters, respectively.	175
5.6	Schematics of the inverters in the (A) N-type VCO and (B) P-type VCO. Their propagation delays are modulated using a current starved transistor in parallel with a non-current starved transistor. .	176
5.7	Simulated performances of the proposed VCO-based VTC. (A) t_{osc} of both VCOs and overall T_{diff} generated as functions of the sampled voltage. (B) Output spectrum for a near Nyquist f_{IN} of 8.12 MHz at F_S of 16.67 MS/s.	180
5.8	Simulated performances of proposed VCO-based VTC for process and temperature variations. Its linearity is degraded. (A) Voltage-to-time transfer functions. (B) SNDR, SNR, THD, and SFDR performances.	181
5.9	Simplified timing diagram of the proposed VCO-based VTC.	184
5.10	Block diagram of the 13-bit SBTDC-II prototype. It composes of a 7-bit ring oscillator based coarse TDC and a 6-bit stochastic-based branching fine TDC.	187
5.11	Schematic of the branching GRO in the SBTDC-II prototype. The core GRO is a gated $N = 10$, $S = 3$ NSRO. The 2^7 stochastic interpolating rising edges are produced by the 2^7 simple inverters of the branching DLs.	189
5.12	Output from a simple inverter at the end of a branching DL across PVT variations. High frequency oscillation from the core GRO is able to reach the end of the branching DL.	191
5.13	Simplified schematic and timing diagram of the improved residue generator. Either the GRO or GROb signal will be chosen to produce the residue time depending on the arbitration result of the D flip-flop.	193
5.14	Simplified timing diagram of the SBTDC-II prototype.	195
5.15	Flowchart of the calibration scheme for the SBTDC-II prototype. .	200
5.16	Illustration of the $2^{9.46}$ raw output codes and their LUT matched ideal 2^8 output codes.	202
5.17	Simplified timing diagram of the proposed time-mode ADC. It illustrates the combined operation of the track and hold circuit, the proposed VCO-based VTC, the SBTDC-II prototype, and the back-end LUT.	203
5.18	Chip layout of the proposed time-mode ADC. It occupies an area of $0.365 \times 0.06 \text{ mm}^2$. The track and hold, proposed VCO-based VTC, and SBTDC-II prototype take up 15%, 14%, and 71% of the total area, respectively.	205
5.19	Measurement setups for measuring the SBTDC-II prototype as a stand-alone TDC and the overall proposed time-mode ADC.	205

5.20	Measured DNL and INL of the SBTDC-II prototype. It achieves a maximum/minimum DNL and INL of 1.98 LSB/−0.82 LSB and 1.63 LSB/−1.58 LSB, respectively. Its expected non-linearity periodicity can be seen from the INL plot.	207
5.21	Measured SSP results of the SBTDC-II prototype. It achieves a maximum SSP of 1.05 LSB. (A) SSP against output code. (B) SSP histograms for mean output codes of 181 and 8060.	208
5.22	Measured DNL and INL of the proposed time-mode ADC. It achieves maximum/minimum DNL and INL of 0.40 LSB/−0.43 LSB and 0.46 LSB/−0.50 LSB, respectively.	213
5.23	Measured output spectrums of the proposed time-mode ADC for f_{IN} of 7.49 MHz at F_S of 15 MS/s. The LUT reduces the harmonic distortions of the proposed VCO-based VTC. (A) Before LUT is applied. 27.03 dB SNDR is achieved. (B) After LUT is applied. 39.90 dB SNDR is achieved.	213
5.24	Measured SNDR, SNR, and THD of the proposed time-mode ADC as functions of input frequency. (A) Before LUT is applied. 4.11-bit ENOB is achieved. (B) After LUT is applied. 6.33-bit ENOB is achieved.	214
5.25	Measured SNDR, SNR, and THD of the proposed time-mode ADC for f_{IN} of 183 kHz as functions of sampling rate. It achieves SNDR and ENOB of 39.69 dB and 6.30-bit, respectively, across varying sampling rates.	216

List of Tables

2.1	Single-Ended Specifications of Recent VTCs in the Literature	17
2.2	Other TDC Architectures Proposed in the Literature, and Their Main Disadvantages.	30
2.3	Targeted Specifications of the Proposed Time-Mode ADC Design. .	34
3.1	Comparison Between the Conventional and Proposed Edge Comparators	53
3.2	Truth Table of a Negative Skewed Inverter Stage	60
3.3	Performance Comparison Between Negative Skewed and Other Reported Multi-Path Differential Ring Oscillators	86
3.4	Measured Phase Noise Performances of Fabricated Single Ended NSROs Divided-by-32 Outputs	87
3.5	Measured Phase Noise Performances of Fabricated SCL Differential NSROs Divided-by-32 Outputs	88
3.6	Measured Phase Noise Performances of Fabricated SD Differential NSROs Divided-by-32 Outputs	88
4.1	Simulated Oscillation Frequency of the GRO and Resulting TDC Time Resolution at Nominal and Worst Case Corners	105
4.2	Noise Breakdown of the BTDC Prototype	124
4.3	Performance Summary of Proposed BTDC Prototype and Other Recently Reported TDCs	127
4.4	Performance Summary of Proposed BTDC and SBTDC-I Prototypes and Other Recently Reported TDCs	161
5.1	Noise Breakdown of the SBTDC-II Prototype	210
5.2	Performance Summary of Proposed TDCs and Other Recently Reported TDCs	211
5.3	Noise Breakdown of the Proposed Time-Mode ADC	216
5.4	Performance Summary of Proposed Time-Mode ADC and Other Recently Reported ADCs	219
5.5	Comparison Between Conventional SAR ADC and Proposed Time-Mode ADC	221

Symbols and Acronyms

Symbols

A_x	Gain of x
C_x	Capacitance of x
f_x	Frequency of x
gm_x	Transconductance of x
I_x	Current of x
R_x	Resistance of x
T_x & t_x	Time quantities of x
V_x	Voltage of x
XQ	Single edge sequence of X
Z_x	Impedance of x
ϕ_x	Phase of x
σ_x	Standard deviation of x, represents noise
τ_x	Propagation delay of x
ARB	Arbitration result of residue generator
B_{OUT}	Binary output code
C_{OUT}	Counter output code
C_i	Coarse output code of length i
c_i	Constant scaling factors
F_{BW}	Bandwidth
F_i	Fine output code of length i
F_S	Sampling rate
f'_f	Maximum slope of falling edge
f'_r	Maximum slope of rising edge
k	Boltzmann constant

k_{osc}	Number of oscillating edges
L	Length of transistor
m	Subthreshold slope factor
N	Total number of stages
N_{linear}	Effective number of linear bits
n	Number of bits
P	Number of parallel delay lines or sets of arbiters
q	Electron charge
q_e	Quantization error
r	Number of truncated LSBs
S	Number of stages in the smaller loop of an NSRO
$s_{N/P}$	Fixed constant scaling factors
T	Temperature
W	Width of transistor
2^{cm}	Maximum length of counter in decimal
α_i	Gain factors
Δ	Delta
η	A proportionality constant
γ	Body-effect coefficient
$\mathcal{L}$	Single-sideband phase noise power spectral density
λ_i	Eigenvalues
$\mathbf{x}_i$	Eigenvectors for λ_i
ϕ_F	Fermi potential
Σ	Sigma
$u_{n/p}$	Mobility of electrons/holes in the inversion layer
ζ	A proportionality constant
$\mathbf{v}$	An array of voltages
$\dot{\mathbf{v}}$	A first-order differential array of voltages
$\cup$	Union operator
$\{ \cdot \}$	A set of elements

Acronyms

ADC	Analog-to-Digital Converter
ADPLL	All-Digital PLL
AFE	Analog Front-End
AFG	Arbitrary Waveform Generator
BEC	Bubble Error Correction
BTDC	Branching TDC
CMOS	Complementary Metal-Oxide-Semiconductor
CDR	Clock and Data Recovery
CDS	Correlated Double Sampling
DAC	Digital-to-Analog Converter
DDP	Dependent Discharging Paths
DEM	Dynamic Element Matching
DL	Delay Line
DLL	Delay-Locked Loop
DNL	Differential Non-Linearity
DTC	Digital-to-Time Converter
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FinFET	Fin Field-Effect Transistor
FoM	Figure-of-Merit
GDL	Gated Delay Line
GRO	Gated Ring Oscillator
IF	Interpolation Factor
INL	Integral Non-Linearity
IoT	Internet-of-Things
IRDS	International Roadmap for Devices and Systems
ISF	Impulse Sensitivity Function
KCL	Kirchhoff's Current Law
LDO	Low Dropout
LHP	Left Half Plane
LSB	Least Significant Bit
LUT	Lookup Table
MOM	Metal-Oxide-Metal

MSB	Most Significant Bit
NMOS	N-type Metal-Oxide-Semiconductor
NSRO	Negative Skewed Ring Oscillator
PDF	Probability Density Function
PDP	Power-Delay-Product
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PMOS	P-type Metal-Oxide-Semiconductor
PoC	Proof of Concept
PSD	Power Spectral Density
PVT	Process, Voltage, and Temperature
PWM	Pulse-Width Modulation
RHP	Right Half Plane
RMS	Root-Mean-Square
RNS	Residue Number System
SAFF	Sense-Amplifier based Flip-Flop
SAR ADC	Successive Approximation ADC
SBTDC	Stochastic-Based Branching TDC
SCL	Source-Coupled Logic
SD	Saturated Delay
SE	Single-Ended
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
SR	Set-Reset
SRO	Switched Ring Oscillator
SSB	Single-Sideband
SSP	Single-Shot Precision
TDC	Time-to-Digital Converter
THD	Total Harmonic Distortion
VCO	Voltage-Controlled Oscillator
VCR	Voltage-Controlled Resistor
VTC	Voltage-to-Time Converter

Chapter 1

Introduction

SENSORS have become an indispensable part of our lives. They improve the quality of our lives by helping us make use of our physical world information. This information presents itself as continuous-time analog signals with infinite resolution. However, the bulk of our sensors uses digital processors which process data using discrete-time digital signals with finite resolution. The preference of processing digital signals over analog signals is due to the greater noise immunity of digital signals. Analog signals are highly susceptible to additive noise which is indistinguishable from the useful signals. Hence, the noise degrades the signal quality. Therefore, an interface is required to convert the physical world analog signals into their digital representations. This interface is referred to as the analog front-end (AFE). The AFE forms an integral part of any sensors, as it bridges the physical world to the digital world.

1.1 Background

A simplified representation of an AFE is shown in Figure 1.1. The AFE comprises of pre-conditioning amplifiers and filters, and an Analog-to-Digital converter (ADC). As its name implies, the ADC is the block that converts the physical world analog signals into their digital representations. The digital signals can then be processed by the digital back-end systems.

FIGURE 1.1: Simplified analog front-end representation. The ADC converts the pre-conditioned analog signals into their digital representations.

In order to reduce cost and size, the AFE should be integrated together with the digital back-end systems on a single chip, forming System-on-Chip (SoC) solutions. This integration has been enabled by the aggressive scaling of complimentary metal-oxide-semiconductor (CMOS) technology into deep sub-micron nodes.

However, as CMOS technology scales, the supply voltage (V_{DD}) has to be reduced in order to protect the transistors from breaking down. Unfortunately, the threshold voltage of the transistors (V_{th}) cannot be scaled proportionally in order to control the amount of subthreshold leakage current [1]. Since the threshold voltage takes up an increasing portion of the supply voltage, the amount of supply headroom available for the circuits has been drastically reduced. These trends are illustrated by the projections from the International Roadmap for Devices and Systems (IRDS) shown in Figure 1.2 [2].

FIGURE 1.2: V_{DD} and V_{th} projections by the International Roadmap for Devices and Systems (IRDS) [2]. V_{th} takes up to 35% of V_{DD} .

The reduced supply voltage and supply headroom limits the input and output voltage swings of analog circuits, and the stackability of transistors. These limitations in turn limit the input voltage range ($V_{IN,Range}$) and resolution of conventional ADCs. For instance, all conventional ADC architectures¹ use amplifiers either directly in their conversion paths, or indirectly in their voltage references and buffers. Consider a simple differential amplifier shown in Figure 1.3 as an example. Note that in this figure and for the rest of the thesis, the body connections of all NMOS and PMOS transistors are tied to ground and V_{DD} , respectively, unless otherwise stated or shown. The input voltage range of this amplifier is limited by the following relationship so as to keep the transistors operating in the saturation region.

$$V_{eff} + V_{thn} - |V_{thp}| \leq V_{IN,Range} \leq V_{DD} - 2V_{eff} - |V_{thp}| \quad (1.1)$$

Using the supply and threshold voltages of the 10 nm FinFET technology node in 2017, i.e. $V_{DD} = 0.75$ V and $V_{thn} \approx |V_{thp}| = 190$ mV [2], and assuming the gate overdrive voltage (V_{eff}) to be 50 mV, the input voltage range of the amplifier is limited to 410 mV. If this amplifier is used for an ADC with a resolution of 10-bit, the least significant bit (LSB) size will be 400 μ V. Such a small LSB size is unfeasible, since it is at the same level as the overall ADC system noise. This system noise encompasses device noise from the circuits, noise from the supplies, and noise due to sampling jitter.

FIGURE 1.3: Schematic of a simple differential common-source amplifier with illustration of its input voltage range limit.

¹Conventional ADC architectures refer to flash, pipeline, successive approximation (SAR), and delta-sigma ($\Delta\Sigma$) ADCs.

Moreover, as CMOS technology scales, there will be more mismatch issues resulting from smaller devices, and larger undesirable leakage currents [1, 2]. It is also difficult to design accurate voltage references in the reduced supply headroom. All these issues mean that the design of conventional ADCs in advanced CMOS technology is becoming increasingly challenging, hindering the development of SoC solutions.

On the other hand, the advancement of CMOS technology has benefited the digital circuits. Since devices are smaller, the intrinsic gate and parasitic fringing capacitances associated with the devices are also smaller. The smaller capacitance, coupled with a lower voltage swing, results in an increase in the operational speed of transistors and overall digital gates. In addition, the reduction of supply voltage also reduces the dynamic power consumption of digital circuits, since dynamic power is proportionate to the square of the supply voltage. Both of these trends are illustrated by the stage delay and dynamic power projections from IRDS as shown in Figure 1.4 [2].

FIGURE 1.4: Digital stage delay and dynamic power at 1 GHz projections by IRDS [2]. Both stage delay and dynamic power are decreasing as CMOS technology scales.

1.2 Motivation

The emergence of big data, cloud computing, artificial intelligence and machine learning is driven by the huge quantities of highly-connected data. These data

are constantly being collected by various sensor nodes. These sensors and data processors form part of the Internet-of-Things (IoT). Many of these sensors are remotely operated, such as portable devices, unmanned vehicles, biomedical implants, and etc. These remote sensors require small footprint and low power consumption so that they can be easily distributed and do not rely on heavy duty batteries [3]. These requirements can be fulfilled by the lower area and power consumption benefits of scaling CMOS technology. Hence, there is a need for the AFE to be continuously integrated into SoC solutions in advanced CMOS technology.

As mentioned, the scaling of CMOS technology has enabled digital gates to have lower delays. Hence, digital gates are able to produce signals, or specifically edges, that are more finely spaced in the time. In other words, time resolution of digital signals in the time-domain is becoming more superior than voltage resolution in the voltage-domain as CMOS technology scales. In light of this phenomenon, time-mode ADC is proposed as a solution that enables ADCs to continuously scale with advancing CMOS technology.

A time-mode ADC uses time as an intermediate in the conversion of the analog input into the digital output. Hence, it capitalizes on the benefit of having better time resolutions in advancing CMOS technology. The simplified block diagram of a time-mode ADC is shown in Figure 1.5. As can be seen, it is built using two main sub-blocks, namely,

- a Voltage-to-Time converter (VTC), and
- a Time-to-Digital converter (TDC).

The VTC converts the analog input into an equivalent time representation, usually in the form of a time difference between a START and a STOP signal. This time representation is then digitized by the TDC, producing the final digital output.

Both the VTC and TDC can be realized using highly digital building blocks, enabling the overall time-mode ADC to avoid the use of complex analog circuitries that suffer from device scaling. In other words, the highly digital nature of time-mode ADC allows it to circumvent the reduced supply headroom and other aforementioned issues plaguing conventional ADC designs in advanced CMOS technology nodes. In addition, being highly digital in nature, time-mode ADC is able to benefit from and scale with advancing CMOS technology.

FIGURE 1.5: Simplified block diagram of a time-mode ADC. It comprises of a VTC, a TDC, and an overall control block.

1.3 Research Objectives

The main objective of this research is to design and implement a time-mode ADC that is scalable with advancing CMOS technology. This time-mode ADC can enable SoC solutions to be implemented in advanced CMOS technology nodes, reducing cost in general, and meeting the small area and low power requirements of remote sensors for IoT.

In order to achieve this main objective, the following two sub-objectives have to be accomplished.

1. A VTC that overcomes the reduced supply headroom issue has to be designed. In order to do so, it has to be built with highly digital building blocks such that the use of voltage amplifiers and references can be avoided. These analog blocks do not scale well with advancing CMOS technology. The output time difference of the VTC and the required TDC time resolution of the subsequent TDC block are interdependent. Hence, the VTC has to generate an output time difference that is compatible to the TDC block.
2. Similarly, a compatible TDC that interfaces with the proposed VTC has to be designed. Despite TDCs being highly digital in nature, not all TDC architectures benefit well from scaling devices. Hence, a suitable TDC architecture has to be chosen such that the proposed TDC can also benefit from and scale well with advancing CMOS technology.

1.4 Organization of Thesis

The background, motivation, and research objectives of this thesis are introduced in this chapter. In summary, the scaling of devices has hindered the development of SoC solutions since it is harder to realize conventional ADCs in advanced CMOS technology nodes. At the same time, it is imperative that SoC solutions are continuously realized in advancing CMOS technology to meet the demands of remote sensing for IoT. Hence, this thesis proposes a time-mode ADC that is scalable with advancing CMOS technology, enabling SoC solutions to be continuously realized.

The rest of this thesis is organized as follows.

Chapter 2 provides an overview and discussion of the VTC and TDC architectures in the literature. In addition, specifications for the proposed time-mode ADC of this research are determined based on a gap identified in the literature.

As part of the research into TDCs, Chapter 3 investigates two building blocks of TDCs. An improved edge comparator with input time hysteresis, and the analysis of ring oscillators employing the negative skewed delay scheme are presented.

Chapter 4 proposes a novel branching phase interpolation TDC architecture that is compatible with CMOS scaling.

Chapter 5 presents an 8-bit time-mode ADC that is built with highly digital building blocks. Its highly digital nature allows it to be scalable with advancing CMOS technology.

Chapter 6 summarizes and draws a conclusion to this thesis. The recommendations and prospects for future research into time-mode ADCs are also discussed.

An overview of the contributions of this thesis is illustrated in Figure 1.6.

FIGURE 1.6: Overview of the contributions of this thesis. The specific positions of the contributions within a time-mode ADC are illustrated.

Chapter 2

Overview of Time-Mode ADCs

AS introduced in Section 1.2, the two main building blocks of time-mode ADCs are the VTC and the TDC. The VTC converts the analog input voltage into a time difference. Then, the TDC converts the time difference into the final digital representation. This chapter provides an overview and discussion of the VTC and TDC architectures in the literature. Following the overview, limitations of the current state-of-the-art time-mode ADCs are discussed, revealing a gap in the literature. Hence, specifications for the proposed time-mode ADC of this research are defined such that it is able to fill this gap in the literature.

2.1 Voltage-to-Time Converter

Since the VTC forms the front-end of an overall time-mode ADC, it is the bottleneck. The input range, linearity, and resolution of a time-mode ADC will be limited by its VTC performance.

In time-mode ADCs, two VTC architectures are mainly employed to perform the voltage-to-time conversion. They are based on the linear capacitor discharge [4–8], and the propagation delay modulation of inverters [9–18].

2.1.1 Linear Capacitor Discharge

The linear capacitor discharge is the simplest VTC architecture. Its simplified schematic is shown in Figure 2.1.

FIGURE 2.1: Simplified schematic of a linear capacitor discharge VTC. The input voltage is converted into the discharge time of the capacitor.

In this VTC, there are two phases, ϕ_1 and ϕ_2 . In the first phase, the capacitor is precharged to the input voltage (V_{IN}). Next, during the second phase, the capacitor will be discharged by the constant current source (I_{dis}). When the voltage across the capacitor (V_{Cap}) crosses the threshold voltage of the inverter ($V_{th,inv}$), an output edge will be produced. Assuming that the RC time constant is sufficiently large, the time taken for the capacitor to discharge (T_{dis}) will be approximately proportional to V_{IN} , and can be described by the following equation.

$$T_{dis} \approx \frac{C}{I_{dis}}(V_{IN} - V_{th,inv}) \quad (2.1)$$

A time difference can be generated by using a second channel. In the second channel, V_{Cap} is precharged to a reference voltage (V_{REF}) instead. Hence, the time difference (T_{diff}) between the two generated edges can be described as follows.

$$T_{diff} \approx \frac{C}{I_{dis}}(V_{REF} - V_{IN}) , \text{ where } V_{REF} \geq V_{IN} \quad (2.2)$$

Albeit simple and straightforward, this VTC architecture has several drawbacks. Firstly, it is fundamentally a non-linear RC circuit. Hence, it has a non-linear transfer function. A large capacitor is required to ensure that the RC time

constant is sufficiently large for approximate linear operations. Secondly, a highly linear and accurate constant current source is required. This current source is a non-trivial analog circuit to design in advanced CMOS technologies, and do not scale well with technology. Thirdly, the input voltage range of this VTC is limited by the requirements for approximate linear operation, the headroom required for the current source, and the threshold voltage of the triggering inverter.

2.1.2 Delay Modulation of Inverters

Voltage-to-time conversion can also be achieved by modulating the propagation delay of an inverter with the input voltage.

2.1.2.1 Propagation Delay Derivation

Consider a chain of identical inverters, the propagation delay (τ_d) of an inverter is defined as the time between when its input crosses its threshold voltage to the time its output crosses the threshold voltage of the next inverter in the chain [19]. This definition is illustrated in Figure 2.2 for both the propagation delays of rising (τ_{dr}) and falling (τ_{df}) output transitions.

FIGURE 2.2: Propagation delay of an inverter.

A complete but complicated analytical expression for the propagation delay can be found in [20]. However, simpler estimation of the propagation delay based

on RC delay are more useful and sufficient for hand designs. Using the following assumptions,

- the voltage ramp at the output of the inverter is based on a response to a step input positioned at when its input crosses its threshold voltage (Figure 2.2),
- $V_{th,inv} = \frac{V_{DD}}{2}$, and
- the saturation drain current of the NMOS or PMOS does not change appreciably even if it enters the triode region.

The propagation delay for a falling output transition can be estimated by the following RC relationship [19].

$$\tau_{df} = \frac{C_{tot}V_{DD}}{2I_{Dn}} \quad (2.3)$$

where C_{tot} and I_{Dn} are the total capacitance including parasitic capacitance at the output of the inverter and the NMOS saturation drain current, respectively. Note that the parasitic capacitance includes the related output capacitance of this inverter stage and the related input capacitance of the next inverter stage. In addition, the gate-drain capacitance of this inverter needs to be replaced by its Miller equivalent. The gain for the Miller equivalent will be high as the NMOS will be in the saturation region. Readers are referred to the textbook by Rabaey et al., Chapter 5, Section 5.4.1 [21] for detailed explanation and breakdown of the total capacitance at the output of the inverter. The NMOS saturation drain current can be expressed as follows.

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{DD} - V_{thn})^2 \quad (2.4)$$

where μ_n is the mobility of electrons in the inversion layer, C_{ox} is the gate capacitance per unit area, and $(\frac{W}{L})_n$ is the width to length ratio of the NMOS transistor. However, if velocity saturation in short channel transistors is considered, the NMOS saturation drain current can be approximated by following expression [21].

$$I_{Dn} = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left((V_{DD} - V_{thn})V_{DSATn} - \frac{V_{DSATn}^2}{2} \right) \quad (2.5)$$

where V_{DSATn} is the NMOS drain-source voltage at velocity saturation.

For the propagation delay of a rising output transition, it can be derived by replacing the NMOS drain current and related parameters in Equation (2.3) to Equation (2.5) by the PMOS counterparts.

2.1.2.2 Propagation Delay Modulation Methods

The propagation delay of the inverter can be modulated by the input voltage using three methods:

1. Modulating the supply of the inverter (Figure 2.3(a)).
2. Current starving of the inverter through NMOS in cascode (Figure 2.3(b)).
3. Current starving of the inverter through NMOS in parallel (Figure 2.3(c)).

In the following derivations, it is assumed that the transistors are not in velocity saturation for simplicity. In addition, only the modulated propagation delay for a falling output transition will be derived. However, the same derivations can be easily applied to derive the propagation delay of a rising output transition.

For the first method, the input voltage directly modulates the supply of the inverter. Hence, the propagation delay can be derived by substituting $V_{DD} = V_{IN}$ in Equation (2.3) and Equation (2.4).

$$\tau_{df} = \frac{C_{tot}V_{IN}}{2I_{Dn}} \quad (2.6)$$

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{IN} - V_{thn})^2 \quad (2.7)$$

For the current starving methods, the propagation delay can be expressed by Equation (2.3). However, the drain current that discharges the output capacitor will be limited and starved by transistor M_A . The drain current of M_A is dependent on the input voltage.

For the second method, the NMOS are connected in cascode. Hence, the discharging drain current can be simply expressed by Equation (2.7) as well.

FIGURE 2.3: Three methods of modulating the propagation delay of an inverter. (A) Through the supply. (B) Current starving with NMOS in cascode. (C) Current starving with NMOS in parallel.

Whereas in the third method, current starved M_A is connected in parallel to M_B which is not current starved. Hence, the total discharging drain current will be a weighted sum of M_A and M_B drain currents.

$$I_{Dn} = I_{DA} + I_{DB}$$

$$I_{Dn} = \frac{1}{2} \mu_n C_{ox} \left(\left(\frac{W}{L} \right)_A (V_{IN} - V_{thn})^2 + \left(\frac{W}{L} \right)_B (V_{DD} - V_{thn})^2 \right) \quad (2.8)$$

For all three methods, when the input voltage falls below the threshold voltage of the NMOS, this NMOS will work in the subthreshold region. Hence, its subthreshold drain current ($I_{Dn,sub}$) can be expressed as follows [21].

$$I_{Dn,sub} = I_{DO} \left(\frac{W}{L} \right)_n \exp \left(\frac{V_{IN}}{mkT/q} \left(1 - e^{-\frac{V_{o,inv}}{kT/q}} \right) \right) \quad (2.9)$$

where I_{DO} is a characteristic current, m is the subthreshold slope factor, k is the Boltzmann constant, T is temperature, q is the electron charge, and $V_{o,inv}$ is the output voltage of the inverter. For the current starving methods, assuming that $V_{DD}/2 \gg kT/q$, Equation (2.9) can be approximated as follows.

$$I_{Dn,sub} = I_{DO} \left(\frac{W}{L} \right)_n \exp \left(\frac{V_{IN}}{mkT/q} \right) \quad (2.10)$$

A time difference can be generated by using a second channel as well, where the propagation delay of the inverter in the second channel is modulated by a reference voltage. Note that in a differential setup, for both the linear capacitor discharge VTC and this VTC architecture, the reference voltage is not required. Instead, the differential input is applied across the two channels.

The simulated transfer function of all three propagation delay modulating methods are also shown in Figure 2.3. It can be seen that this VTC architecture is also highly non-linear. The non-linearity is due to the RC characteristic of the propagation delay. Hence, the input voltage range of this VTC architecture is also limited so as to linearize its transfer function. Between these three delay modulation methods, it can be seen that method 3 has the best linearity.

Despite the non-linearity of this VTC architecture, it is suitable and commonly employed by time-domain comparators for use in SAR ADCs [22, 23]. Since these time-domain comparators only perform 1-bit comparisons, the non-linearity of this VTC is not an issue.

Comparing between the linear capacitor discharge VTC and this VTC architecture, the former VTC has better linearity since its capacitor discharging process is approximately linear [4]. However, this VTC architecture has a more digital structure in the sense that it is basically just an inverter. It does not rely on analog blocks such as current sources or voltage references. Hence, this VTC architecture is more suitable for CMOS scaling.

2.1.2.3 VCO-Based VTC

When the propagation delay modulated inverters are connected in a loop, they form a ring oscillator based voltage-controlled oscillator (VCO). The oscillation

frequency (f_{osc}) of a ring oscillator in general can be approximated as follows.

$$f_{osc} = \frac{1}{N(\tau_{dr} + \tau_{df})} \quad (2.11)$$

where N is the total number of inverter stages in the ring oscillator.

VCO-based VTC integrates the input voltage into the phase of the VCO, allowing it to achieve noise-shaping capability. This noise-shaping capability enables the overall time-mode ADC to achieve better effective resolution. However, noise-shaping requires a high oversampling rate, which comes at a cost of higher power consumption. The detailed mechanism behind the noise-shaping capability of VCO-based VTC will not be discussed here. However, interested readers are referred to [24].

2.1.3 Pulse-Width Modulation

It is worth noting that with the pulse-width modulation (PWM) scheme, commonly employed in class D power amplifiers, the input voltage can be linearly converted into the pulse-width of a square wave (i.e. a time information).

However, the pulse-width modulation scheme requires several highly linear analog building blocks, such as an integrator to generate the ramp signal and a voltage comparator. These analog blocks do not scale well with advancing CMOS technologies, and defeats the purpose of using time as an alternative to voltage processing.

Therefore, detailed operational principle of PWM is not discussed here. Interested readers are referred to [25] and [26].

2.1.4 Consequence of VTC Limitations

The limitations of VTCs can be illustrated using the single-ended specifications of some recent VTCs in the literature. They are summarized in Table 2.1. F_S is the sampling rate.

TABLE 2.1: Single-Ended Specifications of Recent VTCs in the Literature

VTC:	VTC 1 [4] JSSC 18	VTC 2 [9] JSSC 16	VTC 3 [10] TVLSI 16	VTC 4 [11] TCAS-I 17
Type	Cap Dis	INV	INV	INV
CMOS Tech.	65 nm	65 nm	65 nm	65 nm
V_{DD} (V)	1.2	1.3	1.05	1
Res. (bit)	6.93	5	4	5
LSB Size (ps)	2.00	4.00	3.13	2.00
F_S (GS/s)	2	10	5	5
Input Range (mV)	600	150	180	300
Output Range (ps)	244	20	50	64

As mentioned, the input voltage ranges of both VTC architectures are limited by their non-linearity. For example, the largest input range of the VTCs in Table 2.1 is only 600 mV. As explained in Section 1.1, the limited input range will limit the overall resolution of the time-mode ADC.

Since transistors are faster in advanced CMOS technologies, the voltage-to-time gain of VTCs are usually low. The low gain, coupled with the limited input range, results in the time differences generated by the VTCs to be relatively small. From Table 2.1, the output ranges of the VTCs are below or up to a few hundreds of picoseconds. Such small time differences require demanding and high performance TDCs to achieve high resolutions. For example, if VTC 1 is used for an 8-bit time-mode ADC, its output range of 244 ps requires the subsequent TDC to have a very fine time resolution of 0.95 ps. This TDC time resolution is not easy to achieve, especially if it has to be stable across process, voltage, and temperature (PVT) variations as well.

2.2 Time-to-Digital Converter

Time-to-Digital converters (TDC) are traditionally used for precise time-of-flight measurements [27, 28]. They are built with mainly digital building blocks. Hence, they scale very well with the advancement of CMOS technologies. The benefits of CMOS scaling have improved the performance of TDCs, resulting in TDCs being

applied in several other applications. One of these applications is in time-mode ADCs [4, 6–11, 13, 15–18, 24–26, 29, 30]. In a time-mode ADC, the TDC converts the time difference that is proportionate to the input voltage into the final digital output.

Other applications include jitter measurements [31–33] and replacing phase-frequency detectors (PFD) in phase-locked loops (PLL) to form digital PLLs [34–40].

2.2.1 Delay Line TDC

The simplest form of TDC is the delay line TDC [27]. The schematic and timing diagram of an n -bit delay line TDC are shown in Figure 2.4(a) and Figure 2.4(b), respectively.

FIGURE 2.4: Delay line TDC. The input time difference is quantized in terms of the propagation delay of the unit delay stage. (A) Schematic. (B) Timing diagram.

The delay line TDC is built using a chain of unit delay stages, forming a delay line, and arbiters. Delay stages can be in the form of digital buffers or inverters, whereas arbiters can be implemented using simple D flip-flops. Its operational principle is illustrated by Figure 2.4(b) and can be described as follows.

The START signal is fed to the delay line. As it propagates through the delay line, delayed versions of the START signal are produced at the outputs of each delay stage (i.e. at D1 to D2ⁿ). The delayed START signals are separated with a time difference equal to the propagation delay of the unit delay stage (τ_{stage}).

When the STOP signal arrives, it samples the state of the delay line by clocking the D flip-flops. The D flip-flops will output high if their corresponding delayed START signals toggle before the STOP signal arrives, and vice versa. Hence, a thermometer code is produced by the D flip-flops, which can be decoded into a binary digital output.

In other words, the delay line TDC provides a ladder of time steps for the input time difference to compare with using arbiters. Hence, it is analogous to the flash ADC in the voltage domain. The input time difference is quantized in terms of the propagation delay of the unit delay stage, and can be expressed as follows.

$$T_{diff} = B_{OUT} \cdot \tau_{stage} + q_e, \quad q_e \in [0, \tau_{stage}] \quad (2.12)$$

$$T_{LSB} = \tau_{stage} \quad (2.13)$$

where B_{OUT} is the decoded thermometer code, q_e is the quantization error, and T_{LSB} is the TDC time resolution.

The delay line TDC is simple and has a fast conversion rate. However, it has two main drawbacks:

- Its TDC time resolution is limited by the minimum propagation delay of the unit delay stage. This minimum propagation delay, also known as the gate delay, is determined by the CMOS technology.
- Its measurement range is limited by the length of the delay line.

In order to overcome these drawbacks, several other TDC architectures have been proposed.

2.2.2 Vernier Delay Line TDC

A simple method to achieve sub-gate delay TDC time resolution is to replace the simple delay line with a Vernier delay line. This architecture is known as the Vernier delay line TDC [13, 27, 31, 41, 42]. Its schematic is shown in Figure 2.5.

The operational principle of the Vernier delay line TDC is similar to that of the delay line TDC. The difference is that the START and STOP signals of the

FIGURE 2.5: Vernier delay line TDC. The input time difference is quantized in terms of the differential delay between the fast and slow stages.

Vernier delay line TDC is fed to a slow and a fast delay line, respectively, as shown in Figure 2.5. Hence, as both signals propagate through their respective delay lines, the STOP signal slowly catches up to the START signal. A thermometer code will be captured by the arbiters, where the 1-to-0 transition represents the position that the STOP signal overtakes the START signal. Thus, the input time difference is quantized in terms of the differential delay (τ_{vd}) between the slow (τ_{slow}) and fast (τ_{fast}) delay stages. It can be expressed as follows.

$$T_{diff} = B_{OUT} \cdot \tau_{vd} + q_e, \quad q_e \in [0, \tau_{vd}] \quad (2.14)$$

$$T_{LSB} = \tau_{vd} = \tau_{slow} - \tau_{fast} \quad (2.15)$$

Theoretically, the TDC time resolution of the Vernier delay line TDC can be infinitesimally small. However, in practice, it is limited by the accumulated jitter as the START and STOP signals propagate through their delay lines, and by the mismatch between the delay stages of the fast and slow delay lines.

In order to accurately control the differential delay, good matching is required between the fast and slow delay stages. Hence, the transistors in the delay stages are sized up. The larger delay stages increase their propagation delays, resulting in a large latency, or low conversion rate, of the Vernier delay line TDC. In addition, this need for large transistor sizes diminishes the benefits of CMOS scaling, since

devices cannot be small. In other words, the Vernier delay line TDC does not scale very well with advancing CMOS technologies.

The Vernier delay line TDC has been extended to hierarchical [33], 2-dimensional [43], 3-dimensional [44], and spiral [45] architectures. These extensions reduce the conversion latency and the number of delay stages.

2.2.3 Phase Interpolation TDCs

Sub-gate delay TDC time resolution can also be achieved by interpolating in between the discrete phases of a delay line. This architecture is the phase interpolation TDC. Phase interpolation TDC can be implemented with parallel delay lines [34, 46–48], with arbiters sampling in parallel [49], or with stochastic positioning of interpolating edges [50].

2.2.3.1 Parallel Delay Lines TDC

In the parallel delay lines TDC, the START signal will be fed simultaneously into P parallel delay lines. These delay lines are evenly offset by a delay of τ_{stage}/P from one another. This structure is illustrated by the schematic shown in Figure 2.6(a) where $P = 4$.

The first delay line without offset is defined as the main delay line, whereas the others are the sub-delay lines. Since the sub-delay lines are slightly delayed, they will produce delayed versions of the START signal that are in between two phases of the main delay line. In other words, the sub-delay lines interpolate the main delay line. This behavior is illustrated by the timing diagram depicted in Figure 2.6(b). When the STOP signal samples all of the parallel delay lines simultaneously, sub-gate delay TDC time resolution of τ_{stage}/P can be achieved by combining all the edges produced by all the delay lines. Hence, the input time difference for the parallel delay lines TDC can be expressed as follows.

$$T_{diff} = B_{OUT} \cdot \frac{\tau_{stage}}{P} + q_e, \quad q_e \in \left[0, \frac{\tau_{stage}}{P}\right] \quad (2.16)$$

$$T_{LSB} = \frac{\tau_{stage}}{P} \quad (2.17)$$

FIGURE 2.6: Parallel delay lines TDC. The sub-delay lines interpolate the main delay line to achieve sub-gate delay TDC time resolution of τ_{stage}/P . (A) Schematic. (B) Timing diagram.

Since the smallest delay is assumed to be τ_{stage} , a fixed initial offset of τ_{stage} is required to implement all the various time offsets. In addition, the linearity of the parallel delay lines TDC is dependent on the accurate control of all these differing time offsets.

2.2.3.2 Parallel Sampling TDC

The parallel sampling TDC is very similar to the parallel delay lines TDC. Instead of using P delay lines in parallel, the parallel sampling TDC uses P sets of arbiters to sample a single delay line at τ_{stage}/P instances apart from one another. Its schematic is shown in Figure 2.7.

FIGURE 2.7: Parallel sampling TDC. The delay line is interpolated by sampling it at τ_{stage}/P instances apart.

The input time difference for the parallel sampling TDC is also quantized in terms of τ_{stage}/P , and can be expressed by Equation (2.16) and Equation (2.17) as well.

Similar, the linearity of the parallel sampling TDC is dependent on the accurate generation of the delayed STOP signals to clock the D flip-flops. Moreover, additional sets of arbiters are required to increase the interpolation factor of the delay line. These additional arbiters will load the delay line, increasing τ_{stage} , and reducing the effectiveness of this interpolation technique. Hence, the fineness of the TDC time resolution for this interpolation technique is limited.

2.2.3.3 Stochastic Phase Interpolation TDC

In the previous two phase interpolation architectures, the positions of the interpolating edges are fixed by design. However, phase interpolation can also be achieved without deterministic positioning of the interpolating edges. Instead, the interpolating edges are positioned through stochastic processes with redundancy. This phase interpolation method is demonstrated by Kim et al. [50], and is termed as the stochastic phase interpolation TDC. Its schematic and timing diagram is illustrated in Figure 2.8(a) and Figure 2.8(b), respectively.

FIGURE 2.8: Stochastic phase interpolation TDC. The input clock is interpolated by the stochastic positioning of the buffered clocks. Redundancy through LSB truncation is employed. (A) Schematic. (B) Timing diagram.

In this TDC, a clock with period t_{osc} is fed into a long delay line. This delay line has 2^n delay stages, each with a stage delay of τ_{stage} . After an initial setup time of $2^n \cdot \tau_{stage}$, all the delay stages will be buffering the clock input, toggling at a period of t_{osc} . Hence, within a clock period of t_{osc} , 2^n rising edges can be collected from the outputs of all the delay stages using rising edge detectors. Ideally, without any noise or mismatch, the position of each individual rising edge within this t_{osc} is well defined by its position in the delay line. However, in the presence of mismatch between the delay stages and accumulation of jitter along the delay line, τ_{stage} will vary. This variation causes the positions of the rising edges to vary as well.

The variation of τ_{stage} due to mismatch can be modeled by a Gaussian distribution, and can be expressed as follows [50].

$$\tau_{stage,\mu}[i] \sim \frac{1}{\sqrt{2\pi}\sigma_{mis}} \exp\left(-\frac{(t - \tau_{stage,nom})^2}{2\sigma_{mis}^2}\right) \quad (2.18)$$

where t is time, $\tau_{stage,nom}$ is the nominal delay that depends on PVT, and σ_{mis} is the standard deviation arising from mismatch. For jitter, it causes τ_{stage} to experience a dynamic random variation with a Gaussian probability density function (PDF) that can be expressed as follows [50].

$$PDF\langle\tau_{stage}[i]\rangle(t) = \frac{1}{\sqrt{2\pi}\sigma_{jit}[i]} \exp\left(-\frac{(t - \tau_{stage,\mu}[i])^2}{2\sigma_{jit}^2[i]}\right) \quad (2.19)$$

where σ_{jit} is the standard deviation arising from jitter, and i is the index of the delay stage in the delay line. Therefore, the overall PDF modeling the rising edges that are collected within t_{osc} can be expressed by the summation of PDFs of each rising edge position. It is expressed as follows [50].

$$PDF\langle edges \in (at_{osc}, (a+1)t_{osc}) \rangle(t) = \sum_{\substack{1 \leq j \leq n \\ at_{osc} \leq t < (a+1)t_{osc}}} \frac{1}{\sqrt{2\pi} \sum_{i=1}^j \sigma_{jit}^2[i]} \exp\left(-\frac{(t - \sum_{i=1}^j \tau_{stage,\mu}[i])^2}{2 \sum_{i=1}^j \sigma_{jit}^2[i]}\right) \quad (2.20)$$

Note that the accumulation of jitter effect is included in Equation (2.20).

[50] has shown that the overall PDF converges into a uniform distribution when n is large due to the accumulation of jitter from the 2^n delay stages. This is

illustrated by the normalized overall PDF calculated and shown in Figure 2.9 for $\tau_{stage,nom} = 50$ ps, $\sigma_{mis} = 0.05\tau_{stage,nom}$, and $\sigma_{jit} = 0.005\tau_{stage}[i]$ [50].

FIGURE 2.9: Normalized overall PDF of rising edges collected with respect to n for $\tau_{stage,nom} = 50$ ps, $\sigma_{mis} = 0.05\tau_{stage,nom}$, and $\sigma_{jit} = 0.005\tau_{stage}[i]$ [50]. It converges into an uniform distribution as n increases.

In other words, the stochastic phase interpolation TDC make use of random mismatch and jitter to position the rising edges generated from the long delay line. These rising edges interpolate the input clock period, achieving fine TDC time resolution with good linearity since these rising edges are uniformly distributed. In addition, linearity is enhanced through the use of redundancy where the LSB of the final output is truncated by r -bit. Hence, the input time difference for this TDC can be expressed as follows.

$$T_{diff} = B_{OUT} \cdot T_{LSB} + q_e, \quad q_e \in [0, T_{LSB}] \quad (2.21)$$

$$T_{LSB} = \frac{t_{osc}}{2^{n-r}} \quad (2.22)$$

Since this TDC relies on mismatch and jitter, it is immune to PVT variations even without any calibrations. This property also allows it to be synthesizable as demonstrated by [50]. Furthermore, it is able to scale well with advancing CMOS technologies as it can overcome the larger mismatch issue from smaller devices.

Nevertheless, this TDC has several drawbacks. Firstly, the r -bit truncation of the LSB means that a large amount of area and power overheads (2^r times) are required to ensure good linearity. Secondly, this TDC requires an external clock for its operation. Moreover, since the TDC time resolution is dependent on t_{osc} as shown by Equation (2.22), the external clock has to be highly accurate. Lastly, the measurement range of this TDC is limited to t_{osc} . It is not easy to extend the measurement range, as an additional bit doubles both area and power consumption. This issue is exacerbated by the already large n due to the r -bit redundancy.

As compared to Vernier delay line TDC, the TDC time resolutions of phase interpolation TDCs are not reliant on the differential delay between two delay stages. Hence, matching between delay stages for phase interpolation TDCs, especially for the stochastic architecture, are not as critical. In other words, phase interpolation TDCs are able to scale with advancing CMOS technologies. In addition, the latency of phase interpolation TDCs are much lower.

2.2.4 Ring Oscillator Based TDC

The TDCs discussed thus far have their measurement ranges limited by the length of their delay lines. An effective method of extending the range of a TDC is to use a ring oscillator or form a cyclic structure [49, 51–54]. The former will be used to explain this concept.

A ring oscillator can be viewed as a delay line where its end is fed back to its input. Hence, a counter can be added to track the number of laps completed by the ring oscillator within the input time difference, effectively extending the range of the TDC. This architecture is a ring oscillator based TDC. An illustration of a simple free-running ring oscillator based TDC with its timing diagram is shown in Figure 2.10.

In this ring oscillator based TDC, correlated double sampling (CDS) is employed. The START and STOP signals sample separately the START and STOP phases of the ring oscillator using two sets of arbiters bank as shown in Figure 2.10(a). Hence, the input time difference can be obtained from the phase change of the ring oscillator, and the number of cycles completed by the ring oscillator. This relationship is illustrated in its timing diagram (Figure 2.10(b)), and

FIGURE 2.10: Ring oscillator based TDC. The input time difference is quantized in terms of the phase change of the ring oscillator. (A) Schematic. (B) Timing diagram.

can be expressed by the following equations.

$$T_{diff} = C_{OUT} \cdot t_{osc} + (t_{osc} - \phi_{start}) + \phi_{stop} \quad (2.23)$$

$$\phi_{start} = B_{start} \cdot \tau_{stage} + q_{e,start}, \quad q_{e,start} \in [0, \tau_{stage}] \quad (2.24)$$

$$\phi_{stop} = B_{stop} \cdot \tau_{stage} + q_{e,stop}, \quad q_{e,stop} \in [0, \tau_{stage}] \quad (2.25)$$

$$q_e = q_{e,stop} - q_{e,start}, \quad q_e \in [-\tau_{stage}, \tau_{stage}] \quad (2.26)$$

$$T_{LSB} = \tau_{stage} \quad (2.27)$$

where C_{OUT} is the counter output, t_{osc} is the oscillation period of the ring oscillator, ϕ_{start} and ϕ_{stop} are the START and STOP phases of the ring oscillator, B_{start} and B_{stop} are the sampled digital representation of these phases, and $q_{e,start}$ and $q_{e,stop}$ are the quantization errors associated with these samplings.

It can be observed that due to CDS, two quantization errors are incurred,

reducing the signal-to-noise ratio (SNR) by 3 dB. However, CDS also removes common mode errors that are present in both samplings.

A major issue of using a free-running ring oscillator is that it consumes dynamic power even when the TDC is not performing a conversion. Hence, gated ring oscillators (GRO) are usually employed since they can be disabled to save power when the TDC is inactive. In addition, the initial starting phase of a GRO can be reset to a known value. Hence, the quantization error associated to the START phase can be avoided.

Although ring oscillators and cyclic structures can easily extend the measurement range of TDCs by simply extending the length of the counter, the measurement range cannot be infinitely large. As signals propagate through ring oscillators or cyclic structures, they accumulate jitter. The accumulated jitter limits the accuracy of the final time quantization. Hence, the measurement range will be limited by the accumulation of jitter.

In general, a TDC can achieve both large measurement range and fine TDC time resolution by performing a coarse then a fine time quantization of the input time difference (for example [53–56]). This concept is illustrated in Figure 2.11. For example, the coarse TDC can be implemented using this ring oscillator based architecture, whereas the fine TDC can be implemented using one of the sub-gate delay time resolution architectures as discussed in previous sections.

FIGURE 2.11: General block diagram of a coarse-fine TDC. The input time difference is first quantized by the coarse TDC, producing a residue that is further quantized by the fine TDC.

An important design consideration for the coarse-fine TDC is that the measurement range of the fine TDC has to be at least equal to the maximum quantization error of the coarse TDC. This condition ensures that there will not be any missing codes in the overall TDC transfer function.

TABLE 2.2: Other TDC Architectures Proposed in the Literature, and Their Main Disadvantages.

TDC Architecture	Main Disadvantages
Noise Shaping [57–60]	– Oversampling required – Susceptable to leakage
Pulse Shrinking [28, 52, 53, 61]	– Sensitive to PVT variations
Pipelining with Time Registers [62]	– Susceptable to leakage
Stochastic - Offset of Arbiters [32, 63]	– Small measurement range
RNS* [4, 64]	– Requires Residue-to-Binary converter
Time Interval Amplification	
– Metastability [27, 55]	– Highly non-linear – Unreliable control of gain
– DDP* [9, 35, 65]	– Requires accurate control of discharging path
– Pulse Train [56]	– Only integer gain
– SRO* [51]	– Requires accurate control of oscillation frequencies

*RNS = Residue Number Systems, DDP = Dependent Discharging Paths, SRO = Switched Ring Oscillator

2.2.5 Other TDC Architectures

The TDC architectures discussed from Section 2.2.1 to Section 2.2.4 are not exhaustive. There are many other TDC architectures proposed in the literature. These TDC architectures along with their main disadvantages are summarized in Table 2.2.

2.3 Gap in the Literature

As mentioned in the beginning of this chapter, the bottleneck for a time-mode ADC is its front-end VTC.

It is inevitable that in the conversion from voltage-to-time, there will be a RC time constant, resulting in the transfer function of a VTC to be highly non-linear. Despite the ability to approximately linearize this RC decay by designing the time

constant to be relatively large, this non-linearity has limited the input range and resolution of time-mode ADCs.

In addition, as discussed in Section 2.1.4, the time differences generated by VTCs are relatively small. Even though high performance TDCs are required as a consequence, the small time differences also mean that VTCs are operating at very high speeds. This high speed property enables time-mode ADCs to have very high sampling rates as evident in Table 2.1, where their sampling rates are more than 2 GS/s.

Both the aforementioned trends can be observed from the recent time-mode ADCs published in the literature. Many of them are plotted in Figure 2.12, where effective number of bits (ENOB) representing resolution is on one axis, while sampling rate is on the other axis. In addition, these time-mode ADCs are categorized by their scalabilities on a third axis. These time-mode ADCs are also represented by different symbols according to their VTC architectures.

Hybrid refers to a mix of conventional and time-mode ADC architectures. These hybrid ADCs are usually in the form of a coarse-fine architecture, where the coarse is a conventional ADC and the fine is a time-mode ADC. Hence, they leverage on the smaller residue voltages generated by their coarse ADCs to have better linearity performances for their VTCs in their fine ADCs. Consequently, they are able to achieve high resolutions with wide input ranges.

As can be seen from Figure 2.12, most of the recent non-hybrid time-mode ADCs have sampling rates of over 1 GS/s, and ENOB of less than 6.5-bit [4, 9–11]. The high sampling rates albeit relatively low input ranges and resolutions of time-mode ADCs are beneficial and suitable for specific applications such as radio-astronomy [10].

However, there is limited amount of research for low to moderate speed non-hybrid time-mode ADCs with good resolutions of more than 7-bit ENOB. An ADC with this specification is suitable for use by remote sensors in IoT applications.

Even though there are a few hybrid ADCs that fit this specification for remote sensors [6–8, 13], they are still reliant on conventional ADC architectures which do not scale well with advancing CMOS technology. For instance, two of these hybrid ADCs plotted within this specification are implemented with 0.18 μ m CMOS

FIGURE 2.12: Effective number of bits (ENOB), sampling rates, and scalabilities of recent time-mode ADCs published in the literature. There is limited research for low to moderate speed time-mode ADCs with more than 7-bit ENOB.

technology using a supply of 1.8V [6,8]. These hybrid ADCs are not as impacted by device scaling.

For the non-hybrid time-mode ADCs, the VCO-based $\Delta\Sigma$ ADCs do satisfy this specification for remote sensors. Even though they both have a high sampling rate of 1.6 GS/s, their bandwidth are only 10 MHz [16] and 40 MHz [12] (i.e. they have a high oversampling ratio). However, this high sampling rate means that a large power overhead is required to generate the high frequency sampling clock. Hence, they are not preferred to be use in remote sensors where low power is critical.

As discussed at the end of Section 2.1.2.2, even though the linear capacitor discharge based VTC has a better linearity as compared to the inverter based VTC, the latter has a more digital structure and is more suitable for scaling with CMOS technology. The better linearity of linear capacitor discharge based VTC can be observed from Figure 2.12 where they are able to achieve higher resolutions. For the purpose of scaling with advancing CMOS technology, the inverter based

VTC is preferred for the proposed time-mode ADC design as it has the highest scalability as shown in Figure 2.12.

However, it can be seen from Figure 2.12 that the plotted non-hybrid inverter based time-mode ADCs have low resolutions of only about 4-bit ENOB. Their low resolutions are due to the poorer linearity of inverter based VTCs. This poor linearity of inverter based VTC has to be tackled by the proposed time-mode ADC design in order to meet the specification of more than 7-bit ENOB for remote sensors. Since remote sensors do not need high sampling rates, the conversion speed of inverter based VTC could be sacrificed for a better linearity performance. Digital based calibration could also be employed to improve its linearity.

2.3.1 Specifications of Proposed Time-Mode ADC

As discussed, there is limited amount of research for time-mode ADCs that are suitable for remote sensors in IoT applications. Hence, this thesis aims to further the research of low to moderate speed non-hybrid time-mode ADCs with ENOB of better than 7-bit. The proposed time-mode ADC design should be able to scale with advancing CMOS technology. Hence, it should avoid the use of analog blocks such as amplifiers or voltage references. The targeted specifications of the proposed time-mode ADC is summarized in Table 2.3, and plotted in Figure 2.12 as well.

Note that for an ADC, its signal-to-noise and distortion ratio (SNDR) is related to its ENOB as follows.

$$\text{SNDR} = 6.02\text{ENOB} + 1.76 \quad (2.28)$$

In addition, the Walden figure of merit (FoM_{ADC}) for an ADC is expressed as follows.

$$FoM_{ADC} = \frac{\text{Power}}{2^{\text{ENOB}} F_s} \quad (2.29)$$

For the proposed time-mode ADC, rail-to-rail input range is targeted. Most applications do not require rail-to-rail input range. However, the purpose of aiming to achieve rail-to-rail input range is to prove that time-mode ADCs have the ability to overcome the reduced supply headroom issue. This ability stems from the highly digital nature of time-mode ADCs.

TABLE 2.3: Targeted Specifications of the Proposed Time-Mode ADC Design.

Parameter	Specification
VTC Architecture	Inverter based
Resolution	8-bit
Sampling Rate (F_S)	15 MHz
Bandwidth (F_{BW})	7.5 MHz
Voltage Input Range	Rail-to-rail
VTC/TDC T_{LSB}	5 ps
VTC Output Range	≥ 1280 ps
DNL ^a	< 1 LSB
INL ^b	< 1 LSB
SNDR	45.1 dB
ENOB	7.2-bit
Power	500 μ W
Figure of Merit (FoM)	227 fJ/conv.-step
Digital Calibration	Yes

^aDNL = Differential Non-Linearity^bINL = Integral Non-Linearity

In addition, a larger than 8-bit output range of the VTC (≥ 1280 ps) could be required to provide redundancy for the digital calibrations.

Chapter 3

TDC Building Blocks

TIME-to-Digital converters are first investigated as part of the overall goal of designing a time-mode ADC that meets the specifications as described in Section 2.3.1. TDCs are built with two main building blocks:

1. A form of delay line to quantize the input time difference.
2. Arbiters to arbitrate the arrival sequence of the START and STOP signal at a point in the delay line. Arbiters are also known as edge comparators.

In order to achieve a sufficiently large measurement range for the TDC design, the former can be implemented with a ring oscillator instead of a basic delay line as discussed in Section 2.2.4. The latter can be built from simple D flip-flops or set-reset (SR) latches. However, sense-amplifier based flip-flops (SAFF) are preferred to be used as edge comparators since SAFFs have a very narrow metastability window [26].

This chapter investigates these two building blocks, and is split into two main parts.

- In the first part of this chapter, an improved edge comparator that incorporates input time hysteresis mechanism into its edges arbitration is proposed [66]. The use of edge comparators with input time hysteresis enable the output of a TDC to be more robust against noise and jitters in repeated measurements.

- In the second part, ring oscillators employing the negative skewed delay scheme are analyzed. By understanding the characteristics of these ring oscillators, an optimum configuration for the ring oscillator can be chosen in the TDC design.

Both building blocks are verified using simulation results, and prototype chips fabricated in a standard 0.18 μm CMOS technology.

3.1 Edge Comparator With Time Hysteresis

In TDCs, the integrity of their outputs is dependent on the accuracy of their edge comparators. However, in measurements for a slow varying input time difference, the decision of an edge comparator may inaccurately flip from the previous decision due to noise and jitters. This phenomenon is similar to voltage comparators in the voltage domain.

In the voltage domain, input hysteresis can be designed into the voltage comparators through the use of positive feedback [67]. Hysteresis allows the voltage comparators to be more robust against noise when comparing between slow varying voltage signals.

Similarly, in the time domain, input time hysteresis can also enable edge comparators to be more robust against noise and jitters. The better immunity against noise and jitters improves the SNR of the overall TDC for low frequency inputs, and the single-shot precision (SSP) of the overall TDC in general. However, the design of input time hysteresis into edge comparators is non-trivial. It is complicated by the input edges of edge comparators being rail-to-rail swings, and the comparison quantity being time difference between the two input edges.

Nevertheless, this section proposes and demonstrates a novel edge comparator with input time hysteresis [66].

3.1.1 Conventional Edge Comparator

The proposed edge comparator is improved from a SAFF edge comparator presented in [33], which is a modification from the standard StrongARM latch [68].

This edge comparator is defined as the conventional edge comparator for this chapter. Its schematic is shown in Figure 3.1(a).

FIGURE 3.1: Conventional SAFF edge comparator. It is a modification from the standard StrongARM latch, allowing it to be self-clocked. The OR gate is implemented with a balanced structure. (A) Schematic. (B) Timing diagram.

The conventional edge comparator has a symmetrical structure, including the OR gate that is implemented in a balanced structure. The basic operational principle of the conventional edge comparator is illustrated by the timing diagram in Figure 3.1(b), and can be described as follows:

1. When both inputs to differential input transistors M1 and M2 are low, the edge comparator is in a precharge phase. M7 to M9 pull both node Q and node Qb up to V_{DD} .
2. When any of the input edges arrives, the OR gate engages to high which begins the evaluation phase. M7 to M9 are disabled by the OR gate, while node X is weakly connected to node Y through M10.
3. If IN+ arrives first, M1 will produce a current that discharges both node X and node Q.
- 4a. When node Q discharges to the threshold voltage of M6 (i.e. $V_{DD} - V_{thp,M6}$), M6 turns on. Positive feedback from the cross-coupled inverters formed by M3 to M6 takes over to evaluate node Q to low and node Qb to high.
- 4b. Another way of looking at it is that positive feedback takes over when node Q crosses the threshold voltage of the inverter formed by M4 and M6 ($V_{th,inv46}$).
5. Vice versa if IN- arrives first.
6. Node Q and node Qb are buffered to a latch through inverters, where the integrity of the results are stored and maintained during the next precharge phase. The inverters ensure that the symmetrical sides of the edge comparator are equally loaded.

This edge comparator requires its symmetrical sides to be matched. Any mismatches between the left and right sides of the edge comparator will manifest itself as an input referred time offset between the arrival time of the two input edges.

Although this conventional edge comparator is functional and able to arbitrate the arrival sequence of its two input edges, it does not have input time hysteresis. Consequently, as discussed in the beginning of Section 3.1, its successive arbitration decisions are susceptible to noise and jitters. Therefore, an improved edge comparator that achieves input time hysteresis is proposed.

3.1.2 Proposed Edge Comparator

The schematic of the proposed edge comparator that incorporates input time hysteresis into its edge comparison operation is shown in Figure 3.2.

edge comparator is such that the SR latch output node OUT and node OUTb are latched to high and low, respectively.

Firstly, due to the input time hysteresis that is incorporated into the proposed edge comparator, the outputs will only flip if the IN[−] input edge arrives at least $T_H/2$ earlier than the IN⁺ input. T_H is the time hysteresis window.

Secondly, other than the two main modifications to the conventional edge comparator, weak M13 and M14 input transistors are also added to the proposed edge comparator. During the evaluation phase, without M13 and M14, node Q and node Qb will not be able to discharge fully to GND. Their discharge paths are broken by M11 and M12 negative feedback transistors, since M11 and M12 will start to turn off as node Q and node Qb discharge, respectively. The incomplete discharge of node Q or node Qb will result in undesirable contention current in the SR latch. Hence, weak M13 and M14 input transistors are added to only serve as alternative discharge paths for node Qb and node Q, respectively. For example, node Q will be able to discharge fully through M3, M10, M12 and M14. Since M13 and M14 are designed to be much weaker than M2 and M1, respectively, they are assumed to neither participate in the main evaluation process, nor the input time hysteresis mechanism.

The proposed edge comparator is also symmetrical, similar to the conventional case. Hence, any mismatches between its symmetrical sides will also manifest as an input referred time offset between its two input edges.

The following sections will analyze the effects of the two main modifications in detail (i.e. the input time hysteresis mechanism). For the purpose of analysis, the following two assumptions are also made.

- The symmetrical sides of the proposed edge comparator are matched, including the cross-coupled NAND gates of the SR latch.
- The rising profiles of both input edges to the proposed edge comparator are matched.

Note that the comparison results of the proposed edge comparator are decided at the onset of positive feedback. The positive feedback action only drives both node Q and node Qb to complimentary levels. Hence, the input time hysteresis

mechanism has to take effect before node Q or node Qb discharges to the threshold point that triggers positive feedback action.

3.1.2.1 SR Latch Memory Effect

In order to achieve input time hysteresis, a previous result memory effect has to be introduced to the edge comparator. This memory effect is achieved through the direct connection of node Q and node Qb to the SR latch.

From the initial state of the proposed edge comparator (i.e. $OUT = \text{high}$, $OUTb = \text{low}$), consider the case where edges at both inputs now arrive at exactly the same time. Since both symmetrical sides of the edge comparator are matched, both sides will start to discharge using equal discharge currents (i.e. $I_{DM3/4} = I_D$). The parasitic loadings at node Q (C_Q) and node Qb (C_{Qb}) that are contributed by the cross-coupled inverters and the precharge transistors are also equal at both sides. However, the parasitic loadings that are presented by the NAND gates of the SR latch to node Q and node Qb are different. This difference can be explained by considering the transistor level schematic of the SR latch as shown in Figure 3.3. The PMOS of the NAND gates are sized 3 times larger than the NMOS.

During the discharge of node Q and node Qb before the onset of positive feedback, the voltages at node Q and node Qb are above $V_{DD} - V_{thp,M5/M6}$. Hence, PMOS transistors P2 and P4 will not be turned on, and the previous result will continue to be latched by the NAND gates during this time period. Consequently, due to the previous comparison latching node OUT to high and node OUTb to low, the amount of charge recycling occurring at node Q and node Qb are different.

At node Q:

- To charge: $C_{gs,p} + C_{gd,p} \approx 3C_{gs} + 3C_{gd}$
- To discharge: $C_{gs,n} + C_{gd,n} \approx C_{gs} + C_{gd}$
- Overall: To charge $2C_{gs} + 2C_{gd}$

At node Qb:

- To charge: $C_{gs,p} \approx 3C_{gs}$

FIGURE 3.3: Transistor level schematic of the SR latch formed by cross-coupled NAND gates. Parasitic capacitors associated with node Q and node Qb are also shown. The inputs to the transistors are connected by node names.

- To discharge: $C_{gs,n} + C_{gd,n} + C_{gd,p} \approx C_{gs} + C_{gd} + 3C_{gd}$
- Overall: To discharge $C_{gs} + C_{gd}$

where C_{gs} and C_{gd} are the parasitic capacitor between the gate-source and gate-drain, respectively. This difference in charge recycling is illustrated in Figure 3.3. The amount of charge recycling occurring at node Qb is larger as compared to that at node Q. Hence, the effective parasitic loading at node Qb is lower than that at node Q, and the difference can be simply expressed as follows.

$$\Delta C = C_Q - C_{Qb} \quad (3.1)$$

The smaller effective parasitic loading contributed by the NAND gates to node Qb than to node Q is verified by simulation as shown in Figure 3.4.

FIGURE 3.4: Simulation of the parasitic capacitance contributed by the NAND gates to node Q and node Qb before the onset of positive feedback. $C_{Qb,NAND}$ is smaller than $C_{Q,NAND}$ during this period.

In other words, a previous result memory effect is introduced into the proposed edge comparator in the form of a difference in parasitic loading between node Q and node Qb.

Hence, even though both input edges arrive at exactly the same time, node Qb will discharge at a faster rate. The difference in voltage between node Q and node Qb (ΔV_{SD}) can be expressed as follows.

$$\Delta V_{SD} = \Delta V_{SD5} - \Delta V_{SD6} = -\frac{I_D t \Delta C}{C_Q C_{Qb}} \quad (3.2)$$

$$t \approx \left(\frac{C_{Qb}}{I_D} \right) (V_{DD} - V_{thp,M5}) \quad (3.3)$$

where ΔV_{SD5} and ΔV_{SD6} are the voltage changes at node Q and node Qb, respectively. Since node Qb will be at a lower voltage as compared to node Q, node Qb will trigger the positive feedback action, flipping the outputs of the edge comparator. If the inputs continue to arrive at the same time, the outputs will oscillate as illustrated in Figure 3.5. This oscillation is undesirable.

Therefore, even though a previous result memory effect is introduced into the proposed edge comparator, it does not achieve the input time hysteresis effect. The negative feedback M11 and M12 NMOS transistors make use of this memory effect to achieve input time hysteresis for proposed the edge comparator.

FIGURE 3.5: Simulation and timing diagram illustrating the oscillation behavior of the edge comparator output due to the SR latch memory effect.

Note that in Equation (3.1) to Equation (3.3), C_Q and C_{Qb} are partially composed of voltage dependent parasitic junction capacitors. However, for the simplicity of the analysis, C_Q and C_{Qb} are assumed to be approximately constant since the voltage changes across them are relatively small.

3.1.2.2 Negative Feedback NMOS Transistors

During the discharge of node Q and node Qb , negative feedback M11 and M12 NMOS transistors are working in the triode region. Hence, their effects can be understood by modeling them as voltage-controlled resistors (VCR) degenerating the source of the NMOS in their respective inverters as shown in Figure 3.6.

In this model, the output voltage of the inverter controls the turned-on resistance (R_{ON}) of the negative feedback NMOS transistor (i.e. the VCR). Therefore, the threshold voltage of the inverter ($V_{th,inv}$) is dependent on its output voltage through the VCR.

Since the negative feedback NMOS transistor is working in the triode region, its turned-on resistance can be expressed as follows.

$$R_{ON} = \frac{\partial V_{DS}}{\partial I_D} \approx \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{o,inv} - V_{thn})} \quad (3.4)$$

where V_{DS} is the drain-source voltage of the transistor.

FIGURE 3.6: Negative feedback NMOS transistor is modeled as a voltage-controlled resistor degenerating the source of the NMOS in its inverter.

The threshold voltage of the inverter is defined as the point where $V_{i,inv} = V_{o,inv}$. At this point, both the NMOS and PMOS transistors are operating in the saturation region. Their saturation drain currents can be expressed as follows.

$$I_{Dn} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_n \left(V_{th,inv} - I_{Dn} R_{ON} - V_{thn} \right)^2 \quad (3.5)$$

$$I_{Dp} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_p \left(|V_{th,inv} - V_{DD}| - |V_{thp}| \right)^2 \quad (3.6)$$

Hence, $V_{th,inv}$ can be derived by equating Equation (3.5) to Equation (3.6).

$$V_{th,inv} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \quad (3.7)$$

where

$$\begin{aligned} a &= \frac{1}{2} k_p \sqrt{k_r} R_{ON}, \\ b &= -(\sqrt{k_r} + k_p \sqrt{k_r} R_{ON} (V_{DD} - |V_{thp}|) + 1), \\ c &= \sqrt{k_r} \left(\frac{1}{2} k_p R_{ON} (V_{DD} - |V_{thp}|)^2 + V_{thn} \right) + V_{DD} - |V_{thp}|, \\ V_{thn} &= V_{thn0} + \gamma \left(\sqrt{I_{Dn} R_{ON} + 2\phi_F} - \sqrt{2\phi_F} \right), \\ k_r &= \frac{k_n}{k_p}, \quad k_n = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_n, \quad k_p = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_p. \end{aligned}$$

Note that V_{thn} has body effect, where V_{thn0} is the threshold voltage without body effect, γ is the body-effect coefficient, and ϕ_F is the Fermi Potential. However, V_{thn}

is assumed to be constant so as to simplify calculations of Equation (3.7).

The relationship between the threshold voltage and output voltage of the inverter is plotted in Figure 3.7 using Equation (3.7) and simulated values. They are plotted for voltages of node Q and node Qb during their discharge and before the onset of positive feedback.

FIGURE 3.7: Plot of $V_{o,inv}$ against $V_{th,inv}$ using Equation (3.7) and simulation. There is an inverse relationship between the threshold voltage and output voltage of the inverter.

As can be seen from Figure 3.7, there is an inverse relationship between the threshold voltage and output voltage of the inverter, i.e. a lower $V_{o,inv}$ results in a larger $V_{th,inv}$. In addition, the calculated and simulated values are in good agreement. This inverse relationship in addition to the SR latch memory effect enables the proposed edge comparator to achieve the input time hysteresis effect.

As discussed previously, node Qb is discharged to a lower voltage as compared to node Q due to the SR latch memory effect. Hence, the negative feedback M11 and M12 NMOS transistors cause the threshold voltage of the inverter formed by M4 and M6 (i.e. $V_{th,inv46}$) to be higher than that of the inverter formed by M3 and M5 (i.e. $V_{th,inv35}$). This difference in threshold voltages of the inverters in relation to the discharge of node Q and node Qb can be expressed as follows.

$$\Delta V_{th,inv} = (V_{DD} - V_{th,inv35}) - (V_{DD} - V_{th,inv46}) \quad (3.8)$$

Therefore, with Equation (3.2) and Equation (3.8), the overall voltage offset between node Q and node Qb (ΔV) due to both the SR latch memory effect and the negative feedback NMOS transistors is simply expressed as follows.

$$\Delta V = \Delta V_{SD} + \Delta V_{th,inv} \quad (3.9)$$

For the case described in this analysis, ΔV_{SD} is negative whereas $\Delta V_{th,inv}$ is positive. Hence, the overall ΔV will be positive if $|\Delta V_{th,inv}|$ is designed to be larger than $|\Delta V_{SD}|$. In descriptive terms, even though node Q is at a higher voltage as compared to node Qb, node Q will trigger the positive feedback action of the cross-coupled inverters first since $V_{th,inv46}$ is even higher as compared to $V_{th,inv35}$. Consequently, node Q and node Qb will be evaluated to low and high, respectively, maintaining the previous comparison result. This combined effect is illustrated by the exaggerated timing diagram shown in Figure 3.8.

FIGURE 3.8: Exaggerated timing diagram illustrating the comparison result evaluation process of the proposed edge comparator.

Therefore, in order to flip the outputs of the proposed edge comparator, the edge at IN− input needs to arrive at least $T_H/2$ earlier than the edge at IN+ input to overcome the overall voltage offset between node Q and node Qb. Vice versa for the reverse senario where IN− arrives first in the previous comparison.

In summary, the combined effect from the SR latch memory effect and the negative feedback NMOS transistors introduces a dynamic voltage offset between node Q and node Qb. This dynamic voltage offset depends on the previous comparison result, and has to be overcome to flip the outputs. Hence, the proposed edge comparator achieves the input time hysteresis effect.

3.1.2.3 Input Referred Time Hysteresis

The input referred time hysteresis window (T_H) of the proposed edge comparator is expressed as follows.

$$T_H = \frac{2\Delta V}{A_{comp}} \bigg/ \frac{dV_{IN}}{dt} \quad (3.10)$$

where A_{comp} is the small signal gain of the proposed edge comparator during the evaluation phase, and $\frac{dV_{IN}}{dt}$ is the slope of the input edges. The slope of the input edges is approximated to be constant.

The small signal gain can be derived by applying a fully differential analysis that is similar to [69] to the proposed edge comparator. For the differential analysis, it is assumed that $C_Q \approx C_{Qb}$ even though they are slightly different due to the SR latch memory effect. In addition, the precharge transistors and the weak M10 transistor are ignored. Since the proposed edge comparator has a fully symmetrical structure, its small signal model is as shown in Figure 3.9.

FIGURE 3.9: Small signal differential model of the proposed edge comparator.

In Figure 3.9, $\Delta V_{QQb} = V_Q - V_{Qb}$, $\Delta V_{XY} = V_X - V_Y$, $\Delta V_{VW} = V_V - V_W$, $\Delta V_{IN} = V_{IN+} - V_{IN-}$, and $gm_{IN} = gm_{M1/2} - gm_{M14/13}$. $gm_{M1/2}$, $gm_{M14/13}$, $gm_{M11/12}$, and $gm_{M3/4}$ are the transconductances of M1/M2, M14/M13, M11/M12, and M3/M4, respectively. C_V and C_X are the effective capacitance at node V and node X, respectively.

Using the small signal model, the small signal gain can be derived by applying chain rule as follows.

$$\begin{aligned}
 A_{comp} &= \frac{\Delta V_{QQb}}{\Delta V_{IN}} \\
 &= \frac{\Delta V_{VW}}{\Delta V_{IN}} \frac{\Delta V_{XY}}{\Delta V_{VW}} \frac{\Delta V_{QQb}}{\Delta V_{XY}} \\
 &= A_3 A_2 A_1
 \end{aligned} \tag{3.11}$$

where

$$\begin{aligned}
 A_1 &= \frac{gm_{M3/4}}{sC_Q - gm_{M3/4}}, \\
 A_2 &= \frac{gm_{M11/12}}{sC_X + gm_{M3/4}(A_1 + 1) + gm_{M11/12}A_1}, \\
 A_3 &= \frac{-gm_{IN}}{sC_V - gm_{M11/12}(A_1 A_2 - 1)}.
 \end{aligned}$$

3.1.3 Results

The conventional and proposed edge comparators are simulated and fabricated in a standard 0.18 μm /1.8 V CMOS technology using a V_{DD} of 1.8 V. The micrograph of the test chip is shown in Figure 3.10. The core of the proposed edge comparator occupies an area of $0.026 \times 0.014 \text{ mm}^2$. Note that digital trimming capacitor banks are included for the proposed edge comparator to trim its offsets.

FIGURE 3.10: Chip micrograph of the conventional and proposed edge comparators. The core of the proposed edge comparator, highlighted in the center, occupies an area of $0.026 \times 0.014 \text{ mm}^2$.

Since the TDC time resolution is targeted to be in picosecond levels, the input time hysteresis window of the proposed edge comparator is designed to be about 55 fs. Even though the input time hysteresis window of 55 fs is very small, it can be easily simulated in simulations.

In simulations, the input time ramp for the time hysteresis sweep can be created using two clocks with a slight difference in frequencies. The difference in oscillation periods is the step size of the input time ramp. This method is illustrated in Figure 3.11. The simulation results of the time hysteresis sweep applied to the proposed edge comparator using a time ramp step size of 2.5 fs is shown in Figure 3.12. It illustrates the symmetrical input time hysteresis window of 55 fs that is achieved by the proposed edge comparator.

FIGURE 3.11: Method to create an input time ramp in simulations. It can be created using two clocks with a slight difference in frequencies.

FIGURE 3.12: Simulation results of the time hysteresis sweep applied to the proposed edge comparator. A symmetrical input time hysteresis window of 55 fs is achieved.

However, the small value of the input time hysteresis makes it difficult to be measured. Noise and jitters from the measurement equipment and setup can be in the order of picoseconds. Hence, it is difficult to have a deterministic control over the input edges for the proposed edge comparator to be in the order of femtoseconds. Therefore, the measurement of the proposed edge comparator aims to verify the presence of the input time hysteresis effect instead of measuring and quantifying the amount of input time hysteresis (i.e. T_H). The measurement setup for this purpose is shown in Figure 3.13.

FIGURE 3.13: Measurement setup. A single 100 MHz source is fed to separate chains of inverters. A small sine input time difference is created by modulating the supply of one of the inverters with a small 10 kHz sine wave.

In the measurement setup, a single 100 MHz source is fed into two separate chains of buffering inverters that drive $IN+$ and $IN-$ inputs of the proposed edge comparator. These buffering inverters are also fabricated on chip. Since both inputs are driven from the same source, they experience matching jitters contributed by the input source. Hence, jitter considerations from the input source can be neglected.

A small sine input time difference between $IN+$ and $IN-$ inputs of the proposed edge comparator is created by modulating the delay of one of the buffering inverters with a small amplitude 10 kHz sine wave. The delay of the inverter is modulated through modulation of its supply (V_{DDsin}). The input time hysteresis effect can be observed near the zero-crossing points of the modulating sine wave. At these points, the input time differences created will be very small, and are increasing or decreasing with every comparison. In other words, the zero-crossing regions of the modulating sine wave emulate the input time ramps of a time hysteresis sweep.

A proposed edge comparator is fabricated without the M11 and M12 negative feedback NMOS transistors. The SR latch memory effect can be verified through this edge comparator. Using an amplitude of 60 mV for the modulating sine wave, the oscillation of the edge comparator output due to the SR latch memory effect can be observed as shown in Figure 3.14. The output oscillates at the zero-crossing regions of the modulating sine wave since the input time differences created are too small to overcome ΔV_{SD} (Equation (3.2)).

FIGURE 3.14: Measurement result of the SR latch memory effect. The output of the edge comparator oscillates at the zero-crossing regions of V_{DDsin} since the input time differences created are too small to overcome ΔV_{SD} .

For the full proposed edge comparator, an amplitude of 10 mV is used for the modulating sine wave. The input time hysteresis effect can be observed as shown in Figure 3.15, verifying its presence. There are only single transitions of the edge comparator output occurring after the zero-crossing points of the modulating sine wave. This behavior is true for both the upwards and downwards sloping regions of the modulating sine wave. This behavior demonstrates that a dynamic offset has been introduced into the proposed edge comparator, where the sign of the offset depends on the previous comparison result.

Moreover, it can be seen from Figure 3.15 that the modulated supply of the inverter is very noisy. Nevertheless, the output of the edge comparator do not oscillate at transition points. This behavior demonstrates the robustness of the proposed edge comparator against noise and jitters due to the input time hysteresis effect.

FIGURE 3.15: Measurement result of the proposed edge comparator. Input time hysteresis effect is verified since the output of the edge comparator only transits once after the zero-crossing points of V_{DDsin} despite V_{DDsin} being noisy.

TABLE 3.1: Comparison Between the Conventional and Proposed Edge Comparators

Edge Comparator:	Conventional	Proposed
Technology	Standard 0.18 μm CMOS	
V_{DD} (V)	1.8	
Sampling Rate (MS/s)	100	
Avg Dyn Power (μW)	145	180
Hysteresis Window* (fs)	0	55
Core Area (μm^2)	312	364

*Simulated values

A comparison between the conventional and proposed edge comparators is summarized in Table 3.1. At a sampling rate of 100 MS/s, the average dynamic power consumption of the conventional and proposed edge comparators are measured to be about 145 μW and 180 μW , respectively. The larger power consumption of the proposed edge comparator is mainly due to the additional parasitic loadings from the large trimming capacitor banks. These trimming capacitors are not included for the conventional edge comparator. Excluding these trimming capacitors, pre-layout simulations of the conventional and proposed edge comparators show that their power consumption are comparable. They are simulated to consume 55.1 μW and 54.8 μW , respectively.

3.1.4 Limitations

Even though the proposed edge comparator is more robust against noise and jitters due to its input time hysteresis effect, it has three limitations.

Firstly, since the input time hysteresis occurs for inputs with femtoseconds time differences, the input time hysteresis mechanism is actually operating in the metastability region of the proposed edge comparator. In this region, the proposed edge comparator is very sensitive. Any slight mismatches or variations in its environment will cause an exponential change in its behavior. Hence, extensive calibrations would be required for the proposed edge comparator so that it can be robust against PVT variations.

Secondly, the proposed edge comparator can be considered as a large signal circuit since its various node voltages are dynamically changing during a comparison. Moreover, several assumptions are used to simplify the analysis of its input time hysteresis effect. Hence, it is difficult to use Equation (3.10) to accurately design a desirable input time hysteresis window. Instead, the analysis presented should be used to understand the input time hysteresis mechanism, allowing a designer to empirically fine tune a design to achieve a desired input time hysteresis window.

Thirdly, the proposed edge comparator takes about twice the amount of time longer than the conventional edge comparator to resolve a decision when operating in the metastability region. This attribute is illustrated by the simulation as shown in Figure 3.16. Consequently, it increases the latency or dead-time of a TDC. However, since the majority of the dead-time required for a TDC is due to the thermometer-to-binary conversion, especially when n is large, this increase in dead-time is relatively insignificant.

3.2 Analysis of Negative Skewed Ring Oscillators

In the second part of this chapter, ring oscillators employing the negative skewed delay scheme is analyzed.

For the TDC portion of the time-mode ADC design, a measurement range of 8-bit is targeted as summarized in Table 2.3. When the provision of additional

FIGURE 3.16: Simulation of the time required for the conventional and proposed edge comparators to resolve a decision while working in the metastability region. The latter takes about twice as long to resolve its decision.

redundancy bits for digital calibrations is considered, more than 8-bit of measurement range will be required. As discussed in Section 2.2.4, an effective way to achieve such a large measurement range is to use a ring oscillator based TDC.

In a ring oscillator based TDC, its TDC time resolution is dependent on the oscillation frequency, and therefore, the tap-to-tap delay of its ring oscillator. If a simple conventional ring oscillator is used, the tap-to-tap delay will be limited by the propagation delay of its single stage. This barrier has to be overcome to achieve a finer TDC time resolution.

Several techniques have been proposed to increase the oscillation frequency of a ring oscillator. These techniques include coupled ring oscillators [70–72], self-timed rings [73, 74], the negative skewed delay scheme [75], and multi-path ring oscillators [58, 76–79]. All these techniques increase the oscillation frequency of the ring oscillator by more than two-fold. However, only the negative skewed delay scheme uses the same amount of transistors as compared to the conventional ring oscillator. Hence, this scheme adds the least amount of noise sources and area overhead to the ring oscillator. Therefore, even though the largest improvement in oscillation frequency is not achieved by the negative skewed delay scheme, it is chosen for the TDC design.

However, there is a discrepancy in the original analysis of the negative skewed

delay scheme. It does not adequately account for the large improvement in oscillation frequency. This discrepancy will be discussed in detailed shortly. Therefore, the mechanism behind the negative skewed delay scheme is not fully understood.

In order to optimally employ the negative skewed delay scheme for the ring oscillator in the TDC design, a better understanding of this scheme is required. Hence, this scheme is re-analyzed. This section presents an alternative time-domain analysis for the negative skewed delay scheme that better accounts for large improvement in oscillation frequency. However, the proposed time domain analysis only covers the optimum cases and lacks generality. Hence, small signal analysis of this scheme is also presented to supplement the proposed time-domain analysis. The extension of this scheme to differential ring oscillators, and the impact of this scheme to phase noise are also investigated.

3.2.1 Negative Skewed Delay Scheme

The schematic of a single inverter stage that is used in a ring oscillator employing the negative skewed delay scheme is shown in Figure 3.17(a) [75]. This ring oscillator is herein defined as the negative skewed ring oscillator (NSRO).

In the NSRO, the inputs to the NMOS and PMOS transistors in its single stage are decoupled from one another. Either the NMOS or PMOS input is connected to a stage that is earlier than the preceding stage, thereby applying a negative skew to that input. A negative skew of 2 stages means that either the NMOS or PMOS input is connected to 2 stages earlier than the preceding stage. In contrast, both the NMOS and PMOS inputs of an inverter stage in a conventional ring oscillator are connected to the preceding stage. For the rest of the analysis, it is assumed that the negative skew is applied to the PMOS.

In the NSRO, the application of negative skew causes its stages to form loops that have two different lengths. For example, if a negative skew of 2 stages is applied, the lengths of these two loops will be N and $N - 2$ stages. N is the total number of stages in the NSRO. The number of stages in the smaller loop is defined as S (i.e. $S = N - 2$ in this example). In contrast, conventional ring oscillators only have a single loop of length N .

FIGURE 3.17: (A) Negative skewed inverter stage [75]. (B) $N = 11, S = 9$ NSRO. Each stage is defined by its output node. The PMOS are connected by node names. (C) Its simulated oscillation waveform and that of its conventional case. f_S has increased by 89 %, even though τ_{dfs} and τ_{drs} have also increased.

In addition, an NSRO configuration will be referred to by their N and S values. For example, an 11-stage NSRO with a negative skew of 2 stages will be referred to as an $N = 11, S = 9$ NSRO. As an illustration, the schematic and simulated oscillation waveform of this NSRO is shown in Figure 3.17(b) and Figure 3.17(c), respectively. In addition, the simulated oscillation waveform of a conventional 11-stage ring oscillator (i.e. $N = S = 11$) is also shown in Figure 3.17(c) as a comparison. Other schematic examples of an $N = 5, S = 3$ NSRO and an $N = 10, S = 3$ NSRO can be seen in [75].

In a conventional ring oscillator, its oscillation frequency can be approximated by Equation (2.11). It is repeated here for convenience, but denoted by f_C instead

of f_{osc} for this analysis.

$$f_C = \frac{1}{N(\tau_{dr} + \tau_{df})} \quad (3.12)$$

where τ_{dr} and τ_{df} are the propagation delays of its inverter stage for a rising and a falling output edge, respectively. The same assumptions from Section 2.1.2.1 is applied here. Note that f_S , τ_{drs} , and τ_{dfs} denote the oscillation frequency and propagation delays of an NSRO, respectively.

The original analysis of the negative skewed delay scheme explained by Lee et al. [75] is as follows. The oscillation frequency of the NSRO improves as the transitions of its rising and falling edges are sped up by the negative skew.

- During the rising edge transition, the normally weaker PMOS is compensated by turning it on earlier.
- During the falling edge transition, the amount of short-circuit current is reduced by turning the PMOS off prematurely before the NMOS turns on.

This original analysis is quoted extensive in literature, such as in [9, 38, 58, 76].

While the analysis for the falling edge transition is reasonable, the counterpart for the rising edge transition is debatable. The PMOS can be sized appropriately such that it can have approximately the same or even stronger driving strength as compared to the NMOS. Moreover, if the same analysis from the falling edge transition is applied to the rising edge transition, the rising edge transition should slow down. There will be an increase in short circuit current during the rising edge transition as the PMOS turns on prematurely before the NMOS turns off.

In fact, from the simulation as shown in Figure 3.17(c), it is observed that both propagation delays for the rising and falling edges of the NSRO have increased by 28.7 % and 15.6 %, respectively, as compared to the conventional case. The increase in both propagation delays is due to other higher order effects such as the mutual dependency of the rising and falling edges. The larger τ_{drs}/τ_{dfs} ratio of 1.14 (for $N = 11$, $S = 9$ NSRO) as compared to τ_{dr}/τ_{df} ratio of 1.02 (for $N = S = 11$ RO) is in line with the above discussion.

When the propagation delays of the NSRO (i.e. τ_{drs} and τ_{dfs}) are applied to Equation (3.12), it predicts that the oscillation frequency of the NSRO should decrease by 18.2 %. Instead, the same simulation shows that the oscillation frequency

has increased by 89 %. There is a large error of 107.2 %. Hence, the original analysis does not adequately account for the large increase in the oscillation frequency of the NSRO. There is another mechanism at work.

In addition, the optimum skew suggested by [75] is 2 inverters delay. It will be shown that the optimum skew is not that straightforward. It depends on the NSRO configuration.

Other than increasing the oscillation frequency, the negative skewed delay scheme also enables an NSRO with an even total number of stages to oscillate.

3.2.2 Proposed Time-Domain Analysis

The NSRO will be re-analyzed in a time-domain approach to better account for the large improvement in oscillation frequency.

For an NSRO configuration, the characteristics of its optimum oscillation operation or optimum oscillation mode in relation to it being applied in TDCs are defined as follows:

- The output taps of the NSRO are spaced evenly apart with a phase difference of $2\pi/N$.
- The largest oscillation frequency (or lowest tap-to-tap delay) is achieved.

These characteristics allow the TDC to achieve a fine TDC time resolution with good linearity.

As mentioned, the NMOS and PMOS inputs of an NSRO single stage are decoupled from each other. From the output point of view, the output of each stage is connected to two different following stages. Hence, a transition at the output of one stage will cause two different stages to respond, i.e. due to the connected NMOS input at one stage and the connected PMOS input at the other stage. This connection relationship is evident from the example as shown in Figure 3.17(b).

From a digital standpoint, the truth table of a negative skewed inverter stage can be described by Table 3.2. For State 2 and State 3, the stage output will be in a high impedance (Z) and contention state, respectively. These states inhibit an

TABLE 3.2: Truth Table of a Negative Skewed Inverter Stage

State	V_n	V_p	General V_o	Optimum V_o
1	0	0	1	1
2	0	1	Z	V_o
3	1	0	$\approx V_{DD}/2$	$V_o \rightarrow \bar{V}_o$
4	1	1	0	0

oscillating edge from propagating. Hence, for optimum oscillation operation, the stage does not stay in State 2 or State 3 for a long period of time. Instead, it will quickly change to State 1 or State 4. This behavior enables the largest oscillation frequency to be achieved by the NSRO.

In other words, during optimum oscillation operation, the stage output will always be high or low except during transition. State 2 and State 3 can be interpreted as storing the previous output and the start of a transition, respectively. Hence, during optimum oscillation operation, the NSRO at any point in time can be described by the following set of pseudo-digital relationships.

$$V_{o,i}(t) = \bar{V}_n \bar{V}_p + \bar{V}_n V_p V_{o,i}(t), \text{ for } i = 1 \text{ to } N \quad (3.13)$$

$$Transition = V_n \bar{V}_p, \text{ for } i = 1 \text{ to } N \quad (3.14)$$

where

$$V_n = V_{o,i-1}(t)$$

$$V_p = V_{o,i-(N-S)-1}(t)$$

Note that each stage is defined by its output node and indexed by i . The looping effect of ring oscillators can be accounted for by adding or subtracting N to the index whenever it is smaller than 1 or larger than N . This looping effect will be applied throughout the rest of the analysis even if it is not stated explicitly.

The time parameter (t) shows that all N stages of the NSRO continuously interact with one another through events of rising and falling edges to satisfy all equations in Equation (3.13) and Equation (3.14) simultaneously. Therefore, the NSRO is a complicated dynamic system where all its stages are interrelated.

In addition, there are multiple solutions to Equation (3.13) and Equation (3.14). Hence, it is possible for the NSRO to have multiple modes of oscillation at steady state. The chosen mode at steady state depends on the NSRO configuration (N and S) and the initial conditions applied. For the rest of the analysis, the stages will be referred to by their indexes. For example, Stage $V_{o,i}$ will be referred to as Stage i .

In order to see the propagation relationship between all the stages of the NSRO in a graphical manner, a special analysis tool termed the sequence tree as shown in Figure 3.18(a) is proposed. Every node in the sequence tree represents a stage in the NSRO. The left and right branches from a node correspond to the next stage NMOS and PMOS connections, respectively. Since the negative skew is applied to the PMOS, it can be generalized that from Stage i , its next stage NMOS connection is always at Stage $i + 1$, whereas its next stage PMOS connection is always at Stage $i + (N - S) + 1$. Note that since an oscillating edge propagates forward in a ring oscillator, the tracking of the stages is also counted upwards from 1 to N . The looping effect of ring oscillators is represented by the brackets in Figure 3.18(a). In addition, within the same level in the sequence tree and counting upwards in the ring, it can be derived that the difference between a node from its left or right neighbor is $N - S$ or S , respectively, as shown in Figure 3.18(a). Hence, for the sequence tree to form fully until Level N without repetition of stages in the same level, S and $N - S$ have to be relatively prime to N . The sequence tree for the $N = 11$, $S = 9$ NSRO is illustrated in Figure 3.18(b), whereas Figure 3.18(c) exemplifies a sequence tree that is unable to form fully when $N = 9$ and $S = 3$.

Since each stage is related to two other stages in the NSRO, there will be large contention conditions during oscillation if there is only a single oscillating edge. These contentions arise from State 2 and State 3 of the truth table (Table 3.2). Hence, for optimum oscillation operation, the NSRO supports the propagation of multiple oscillating edges. These multiple oscillating edges satisfy the system of Equation (3.13) and Equation (3.14) with minimum contention conditions. Hence, the primary mechanism that increases the oscillation frequency of the NSRO is this presence of multiple oscillating edges. They increase the oscillation frequency by the factor of the number of oscillating edges. This phenomenon is similar to

FIGURE 3.18: (A) Proposed sequence tree. It represents the propagation relationship between the stages of an NSRO. (B) Sequence tree of an $N = 11$, $S = 9$ NSRO. Arrows are removed for compactness. (C) Sequence tree of an $N = 9$, $S = 3$ NSRO. There are repetitions in the same level.

self-timed rings [73, 74]. Therefore, Equation (3.12) can be modified as follows.

$$f_S = \frac{k_{osc}}{N(\tau_{drs} + \tau_{dfs})} \quad (3.15)$$

where k_{osc} is the number of oscillating edges propagating within the NSRO.

The derivations of τ_{drs} and τ_{dfs} are non-trivial. As a quick estimation, assuming that the reduction of short-circuit current during the falling edge transition can be approximately compensated by the increase during the rising edge transition, the original τ_{dr} and τ_{df} of a conventional N stages ring oscillator can be used as replacements. However, in the simulations for this analysis, τ_{drs} and τ_{dfs} will be extracted directly from results.

An intuitive way of understanding the presence of multiple oscillating edges is

to study an $N = 10$, $S = 5$ NSRO, and compare it with a 5-stage conventional ring oscillator. The simulated oscillation waveforms from this conventional ring oscillator, Stage 1 and Stage 6 outputs of this NSRO are shown in Figure 3.19. It can be seen that they are all oscillating with the same frequency. In addition, Stage 1 and Stage 6 outputs of this NSRO are also oscillating in-phase. Although not shown, the other stages of this NSRO are also oscillating in-phase (Stage 2 with Stage 7, Stage 3 with Stage 8, and so on). Therefore, this NSRO can be viewed as two 5-stage conventional ring oscillators that are connected in series. Together, they produce two oscillating edges within this 10-stage NSRO, doubling its oscillation frequency. Hence, the oscillation frequency of this NSRO is not limited by its unit stage propagation delay.

FIGURE 3.19: Simulated oscillation waveforms of a conventional 5-stage ring oscillator, Stage 1 and Stage 6 outputs of an $N = 10$, $S = 5$ NSRO. They are oscillating with the same frequency and phase.

3.2.2.1 Single Edge Sequence

In order to determine the number of oscillating edges propagating within a configuration of NSRO, the phase sequence of a single oscillating edge should be understood. In this analysis, one cycle of this repeating rising edges sequence is defined as the single edge sequence. In an N -stage conventional ring oscillator, its single

edge sequence (CQ_N) can be expressed as follows.

$$\{cq_i\}_{i=2}^N = \{cq_{i-1} + 2\}, \quad cq_1 = 1. \quad (3.16)$$

For instance, the single edge sequence of a 5-stage conventional ring oscillator is $CQ_5 = \{1, 3, 5, 2, 4\}$.

For an NSRO, using the sequence tree in Figure 3.18(a) as a guide, consider a rising edge occurring at Stage i . This rising edge causes two separate falling edges to occur at Stage $i + 1$ and Stage $i + (N - S) + 1$ since Stage i is connected to the NMOS input of Stage $i + 1$ and the PMOS input of Stage $i + (N - S) + 1$. Then, these two falling edges will converge back and cause the next rising edge to occur at Stage $i + (N - S) + 2$. This convergence occurs as both Stage $i + 1$ and Stage $i + (N - S) + 1$ are connected to the PMOS input and the NMOS input of Stage $i + (N - S) + 2$, respectively. This convergence event is the single edge sequence of an NSRO (SQ_N^S). Hence, the single edge sequence of an NSRO can be derived from any straight column in its sequence tree, and can be expressed as follows.

$$\{sq_i\}_{i=2}^N = \{sq_{i-1} + (N - S) + 2\}, \quad sq_1 = 1 \quad (3.17)$$

For instance, the single edge sequence for an $N = 11$, $S = 5$ NSRO is $SQ_{11}^5 = \{1, 9, 6, \dots\}$. This single edge sequence is illustrated by the sequence tree and simulated oscillation waveform of this NSRO as shown in Figure 3.20(a) and Figure 3.20(b), respectively. Note that this NSRO only supports one oscillating edge. As a result, large contention conditions can also be observed from Figure 3.20(b).

For cases involving multiple oscillating edges, they can be categorized into:

1. Total number of stages, N , is odd,
2. Total number of stages, N , is even.

In the following analysis for multiple oscillating edges, only the optimum oscillation mode will be discussed.

FIGURE 3.20: (A) Sequence tree and (B) simulated oscillation waveform of an $N = 11$, $S = 5$ NSRO. The single edge sequence of this NSRO (SQ_{11}^5) can be derived from any straight column in its sequence tree.

3.2.2.2 Odd Total Number of Stages

When the total number of stages in an NSRO is odd, there are two types of loop in the NSRO that can provide a phase shift of 2π to sustain oscillation. They are of lengths N and S . In the optimum oscillation mode, due to the interactions between these two types of loop, this type of NSRO behaves as follows.

Due to the decoupling of the NMOS and PMOS, a rising edge occurring at Stage i will cause a falling edge to first occur at Stage $i + 1$, followed by another at Stage $i + (N - S) + 1$. For a negative skew of 2 stages (i.e. $S = N - 2$), using Stage i as reference for phase 0, these falling edges occur at phase $2\pi/N$ and phase $2(2\pi/N)$, respectively. They are termed the early and late edge, respectively. Then, the single edge sequence rising edge at Stage $i + (N - S) + 2$ occurs at approximately the same phase as the late falling edge (i.e. $\approx$ phase $2(2\pi/N)$). These transition events are exemplified by the timing diagram of an $N = 11$, $S = 9$ NSRO as shown in Figure 3.21. They are part of single edge sequence A where $i = 3$. The sequence tree of this NSRO shown in Figure 3.18(b) can be used as a guide.

In order to have stability and uniformity in the symmetrical NSRO, another rising edge should also occur at Stage x with approximately the same phase as the early falling edge (i.e. $\approx$ phase $2\pi/N$). This rising edge originates from an even earlier rising edge at Stage q that occurs before phase 0. In other words, the rising

FIGURE 3.21: Timing diagram illustrating two separate single edge sequences occurring simultaneously in an $N = 11$, $S = 9$ NSRO. The two single edge sequences increase the oscillation frequency of this NSRO by a factor of 2.

edge at Stage x is another single edge sequence following Stage q .

$$x = q + (N - S) + 2 \quad (3.18)$$

Therefore, the early falling edge due to Stage i is the same late falling edge due to Stage q . This second single edge sequence is illustrated by sequence B in Figure 3.21. Using this relationship between the falling edges of the two single edge sequences and Equation (3.18), the following relationship can be derived.

$$\begin{aligned} i + 1 &= q + (N - S) + 1 \\ x &= i + 2 \end{aligned} \quad (3.19)$$

In this example, using Equation (3.18) and Equation (3.19), it can be easily shown that $x = 5$ and $q = 1$.

In fact, using Equation (3.19), the rising edge at Stage $i + (N - S) + 2$ following single edge sequence A can be derived to have the following relationship.

$$\begin{aligned} i + (N - S) + 2 &= i + 4 \\ &= x + 2 \end{aligned} \quad (3.20)$$

Therefore, the overall phase sequence for this configuration of NSRO is the same as that of a conventional ring oscillator. It is 2 stages apart and can be described by Equation (3.16).

Overall, as shown by Figure 3.21, there are two separate single edge sequences occurring simultaneously in this configuration of NSRO. In other words, there are two separate oscillating edges propagating in this NSRO. These two oscillating edges increase the oscillation frequency of this NSRO by a factor of 2 (i.e. $k_{osc} = 2$). However, the larger contention during its rising edge transition results in a final oscillation frequency increment of less than 2 times. This contention is resultant from the falling edges having a phase difference of $2\pi/N$.

Note that if the analysis starts from a falling edge instead of a rising edge at Stage i , the subsequent rising edges at Stage $i+1$ and Stage $i+(N-S)+1$, and the single edge sequence falling edge at Stage $i+(N-S)+2$ will occur at approximately phase 0, phase $2\pi/N$, and phase $2(2\pi/N)$, respectively. The same conclusions can be derived. In addition, if the negative skew is applied to the NMOS instead of the PMOS, the above analysis is still applicable. In this case, the behavior of the rising and falling edges are reversed, and the contention occurs during the falling edge transition.

For a negative skew of 4 stages (i.e. $S = N - 4$), the falling edges at Stage $i+1$ and Stage $i+(N-S)+1$ due to a rising edge at Stage i occur at phase $2\pi/N$ and phase $3(2\pi/N)$, respectively. The following single edge sequence rising edge at Stage $i+(N-S)+2$ occurs at approximately the same phase as the late falling edge (i.e. $\approx$ phase $3(2\pi/N)$).

Similarly, for stability and uniformity in the symmetrical NSRO, another falling edge should also occur at phase $2(2\pi/N)$, and two separate rising edges should also occur at phase $2\pi/N$ and phase $2(2\pi/N)$. These two rising edges occur at Stage v and Stage y , respectively. All of these transition events are illustrated in the timing diagram of this NSRO as shown in Figure 3.22. Using the same analysis as before, the following relationships can be derived.

$$v = i + 2 \tag{3.21}$$

$$y = v + 2 \tag{3.22}$$

Equation (3.21) and Equation (3.22) show that the overall phase sequence for this configuration of NSRO is also the same as that of a conventional ring oscillator. It is also 2 stages apart as described by Equation (3.16). However, there are

FIGURE 3.22: Timing diagram illustrating three separate single edge sequences occurring simultaneously in an odd N , $S = N - 4$ NSRO. The three single edge sequences increase the oscillation frequency of this NSRO by a factor of 3.

three oscillating edges coexisting within this NSRO. Together, they increase the oscillation frequency of this NSRO by a factor of 3 (i.e. $k_{osc} = 3$).

In this configuration of NSRO, the contention during its rising edge transition arises from falling edges that have a larger phase difference of $2(2\pi/N)$. Hence, there is larger contention during its rising edge transition, resulting in the final increment in oscillation frequency of this NSRO to be much lesser than 3 times.

For NSROs with a larger amount of negative skew (i.e. $S < N - 4$), such as the example in Figure 3.20, there are only one oscillating edge propagating within these NSROs. Hence, these configurations are undesirable.

In contrast to [75], the optimum skew for largest oscillation frequency is 4 stages. However, it will be shown in Section 3.2.6 that the Power-Delay-Products (PDP) of NSROs with a negative skew of 2 stages are comparatively better.

3.2.2.3 Even Total Number of Stages

When the total number of stages in an NSRO is even, only the loop with length S provides the required phase shift of 2π to sustain oscillation. For this type of NSRO, there is only one optimum S configuration for each N -stage NSRO that can achieve the optimum oscillation operation. This configuration of NSRO behaves as follows during optimum oscillation operation.

For optimum oscillation operation, the sequence tree of this NSRO must be able to form fully (i.e. S and $N - S$ relatively prime to N). Following the single edge sequence, a rising edge at Stage i causes an early and a late falling edge to occur at phase $2\pi/N$ and phase $2(2\pi/N)$, respectively. After which, the single edge sequence rising edge at Stage $i + (N - S) + 2$ occurs at phase $3(2\pi/N)$.

Similarly, uniformity and stability of the symmetrical NSRO can be achieved by having two other single edge sequences propagating in this NSRO. Separately, they produce rising edges at Stage w and Stage u that are in phase with the early and late falling edges due to Stage i , i.e. at phase $2\pi/N$ and phase $2(2\pi/N)$, respectively. All of these transition events are illustrated by the timing diagram as shown in Figure 3.23.

Assuming that the early and late falling edges occur at Stage $i + 1$ and at Stage $i + (N - S) + 1$, respectively. Stage w and Stage u can be derived by applying the same analysis as before.

$$w = i + (N - S) \quad (3.23)$$

$$u = i + 2(N - S) \quad (3.24)$$

In addition, continuing the analysis such that the early falling edge due to Stage $i + (N - S) + 2$ is the same late falling edge due to Stage u , the following condition to determine the optimum S for an even N -stage NSRO can be derived.

$$\begin{aligned} i + (N - S) + 3 &= u + (N - S) + 1 \\ (N - S) + 2 &= 3(N - S) \end{aligned} \quad (3.25)$$

FIGURE 3.23: Timing diagram illustrating three separate single edge sequences occurring simultaneously in an even N -stage NSRO with optimum S . The three single edge sequences increase the oscillation frequency by a factor of 3.

The overall phase sequence (EQ_N^S) for this configuration of NSRO is revealed by Equation (3.23) and Equation (3.24), and can be described as follows.

$$\{eq_i\}_{i=2}^N = \{eq_{i-1} + (N - S)\}, \quad eq_1 = 1 \quad (3.26)$$

However, if the early and late falling edges occur at Stage $i + (N - S) + 1$ and Stage $i + 1$ instead, respectively, another set of relationships for Stage w and Stage u , optimum S condition, and EQ_N^S can be derived as shown below.

$$w = i + S \quad (3.27)$$

$$u = i + 2S \quad (3.28)$$

$$2S = 2(N - S) + 2 \quad (3.29)$$

$$\{eq_i\}_{i=2}^N = \{eq_{i-1} + S\}, \quad eq_1 = 1 \quad (3.30)$$

Do note that the looping effect is applied throughout all of the above analyses.

In summary, when the total number of stages in an NSRO is even, optimum oscillation operation can be achieved when S is chosen such that either Equation (3.25) or Equation (3.29) is satisfied. In this NSRO, there are three edge sequences occurring simultaneously, increasing its oscillation frequency by a factor of 3 (i.e. $k_{osc} = 3$). The overall phase sequence of this NSRO can be described by Equation (3.26) or Equation (3.30), respectively. Note that the contention between the NMOS and PMOS for this NSRO occurs during the rising edge for the former case, and during the falling edge for the latter case. As compared to the odd N , $S = N - 4$ NSRO configuration, this contention is less severe as the phase difference between the early and late edges is smaller at $2\pi/N$. Hence, the final increment in oscillation frequency of this NSRO is less degraded from the factor of 3.

On further inspection of Equation (3.26) and Equation (3.30), it reveals that the nodes sequence in level N of the sequence tree is able to predict the overall phase sequence of an even N -stage NSRO with optimum S . As discussed previously, the difference between a node from its left or right neighbor is $N - S$ or S , respectively. These differences correspond to Equation (3.26) and Equation (3.30), respectively.

As an example, an $N = 10$, $S = 3$ NSRO satisfies Equation (3.29). Hence, its overall phase sequence is described by Equation (3.30), i.e. $EQ_{10}^3 = \{1, 4, 7, \dots\}$. This overall phase sequence can be seen from the sequence tree and simulated oscillation waveform of this NSRO as shown in Figure 3.24(a) and Figure 3.24(b), respectively.

FIGURE 3.24: (A) Sequence tree and (B) simulated oscillation waveform of an $N = 10$, $S = 3$ NSRO. Level N of the sequence tree shows the overall phase sequence of this NSRO as described by Equation (3.30).

Other than the optimum oscillation mode that is described in Section 3.2.2.2 and Section 3.2.2.3, an NSRO can also support other oscillation modes. The multiple oscillation modes of an NSRO is discussed earlier in Section 3.2.2. These other oscillation modes may also have multiple oscillating edges. However, these oscillating edges are overlapped in phase, similar to the example in Figure 3.20. Hence, these other oscillation modes are not suitable for TDC application.

3.2.3 Small Signal Analysis

Despite the proposed time-domain analysis being simple and useful in determining the optimum oscillation operation of an NSRO configuration, it lacks generality. The proposed analysis does not cover all NSRO configurations, and does not cover non-optimum oscillation modes. In addition, the proposed analysis does not explain how the optimum oscillation mode is reached, and how different initial conditions can lead to different oscillation modes at steady state. Hence, small signal analysis is performed for the NSRO to supplement the proposed time-domain analysis. This small signal analysis of the NSRO explains the aforementioned characteristics.

For the small signal analysis, it is assumed that the amplitude of an NSRO oscillation is small and sinusoidal shaped. This assumption is applicable during the startup of the oscillation. This small signal oscillation will grow to rail-to-rail levels at steady state. However, it is noted that at steady state, an NSRO is a highly non-linear large signal circuit. Hence, parameters of the NSRO shift away from its small signal values, and there is no constant biasing point in the NSRO at steady state.

As such, the main objective of this small signal analysis is to gain more insights into the characteristics of an NSRO configuration. These insights include:

- Understanding the different modes of oscillation that are possible at steady state.
- Determining the overall phase sequence.
- Understanding the effects of initial conditions.
- Estimating the amount of frequency improvement (f_S/f_C).

The small signal oscillation of the small signal analysis do not represent the actual rail-to-rail oscillation at steady state.

The small signal model of a negative skewed inverter stage in an NSRO is shown in Figure 3.25. gm_n , gm_p , r_o , and c_l are the NMOS and PMOS transconductances at biasing point, effective output resistance and capacitance, respectively. Similar to the analysis in [77], a system of first-order linear differential equations for the NSRO can be derived using the small signal model as follows.

$$\dot{\mathbf{v}} = \left(-\frac{1}{r_o c_l} \right) (\mathbf{v} + A_{v,n} \mathbf{v}_n + A_{v,p} \mathbf{v}_p) \quad (3.31)$$

where

$$\begin{aligned} \mathbf{v} &= [v_{o,i}(t)]^T, \quad \text{for } i = 1 \text{ to } N \\ \mathbf{v}_n &= [v_{o,i-1}(t)]^T, \quad \text{for } i = 1 \text{ to } N \\ \mathbf{v}_p &= [v_{o,i-(N-L)-1}(t)]^T, \quad \text{for } i = 1 \text{ to } N \\ A_{v,n} &= gm_n r_o \\ A_{v,p} &= gm_p r_o \end{aligned}$$

FIGURE 3.25: Small signal model of an inverter stage in an NSRO.

The arrays of $\mathbf{v}_n$ and $\mathbf{v}_p$ are dependent on the configuration of the NSRO. Equation (3.31) can be rewritten into the form of $\dot{\mathbf{v}} = \mathbf{A} \mathbf{v}$ where $\mathbf{A}$ is an $N \times N$ matrix. This system has N eigenvalues (λ_i) as follows.

$$\lambda_i = \alpha_i + j\omega_{osc,i}, \quad \text{for } i = 1 \text{ to } N \quad (3.32)$$

where α_i are the gain factors. For a pair of complex eigenvalues in the right half plane (RHP) of the complex plane, for example λ_i and λ_{i+1} , its real-valued general solution can be expressed as follows.

$$\mathbf{v} = \text{real}(c_i \mathbf{x}_i e^{\lambda_i t} + c_{i+1} \mathbf{x}_{i+1} e^{\lambda_{i+1} t}) \quad (3.33)$$

where $\mathbf{x}_i$ is the corresponding eigenvector for λ_i , and c_i is a constant scaling factor.

Hence, any pair of complex eigenvalues in the RHP of the complex plane has small signal oscillation solutions that can grow exponentially to rail-to-rail outputs at steady state. Each of these pairs represents a possible mode of oscillation for the NSRO. Therefore, the multiple pairs of complex eigenvalues in the RHP of the complex plane account for the multiple modes of oscillation that are possible at steady state. The overall phase sequence of each oscillation mode can be extracted using Equation (3.33). The small signal solutions from the eigenvalues in the left half plane (LHP) of the complex plane decay and eventually die off during transient.

During small signal transient at startup, all the possible modes of oscillation for the NSRO are superimposed together according to the superposition principle. At large signal steady state, non-linearity effects take over and only one of these oscillation modes dominates. The rest die off during transient.

From Equation (3.33), it can be seen that the oscillation mode that dominates at steady state is dependent on the following two factors.

1. The gain factor in the exponent term, α_i . It depends on the technology, biasing point, and configuration of the NSRO. It determines the dominance of an oscillation mode.
2. The constant scaling factor, c_i . It depends on the initial conditions of the NSRO. Hence, applying different initial conditions to the NSRO may lead to a different oscillation mode that dominates at steady state.

As an example, using small signal parameters that are evaluated from simulations at biasing point of assuming $V_{DD}/2$, normalizing $r_o c_l$ to 1, the normalized eigenvalues of an $N = 16$, $S = 7$ NSRO are plotted in Figure 3.26. It can be seen that there are three pairs of complex eigenvalues in the RHP of the complex plane. Each of these pairs corresponds to a set of general solution, and hence, a possible

mode of oscillation for this NSRO at steady state. In this example, the eigenvalues pair with the largest real part corresponds to the optimum oscillation mode as described by Section 3.2.2.3. The other two pairs of complex eigenvalues correspond to two different oscillation modes where there are 4 or 2 oscillating edges in this NSRO that are overlapped in phase, similar to the example in Figure 3.20.

FIGURE 3.26: Normalized eigenvalues of an $N = 16$, $S = 7$ NSRO. Each complex eigenvalues pair in the RHP of the complex plane corresponds to a possible mode of oscillation for this NSRO at steady state.

Lastly, the improvement in oscillation frequency from applying the negative skewed delay scheme can be estimated by comparing Equation (3.33) of an NSRO to that of its conventional case. For instance, the improvements in oscillation frequency for an $N = 11$, $S = 9$ NSRO and an $N = 11$, $S = 7$ NSRO are estimated to be 1.89 and 2.32, respectively. These estimations are close to the simulated results where the improvements are 1.89 and 2.64, respectively.

Despite the small signal analysis being comprehensive, it is mathematically complex, especially when the total number of stages in an NSRO is large. Moreover, Equation (3.31) is unique for each S configuration of an N -stage NSRO. Therefore, although the proposed time-domain analysis lacks generality, it efficiently covers the important optimum cases where the NSROs are most useful.

3.2.4 Extension to Differential Ring Oscillators

The analysis thus far has been focused on single-ended (SE) NSROs. However, the negative skewed delay scheme can also be directly extended to differential ring oscillators, increasing their oscillation frequencies without any addition transistors.

Two architectures of differential ring oscillators are considered:

1. Built with source-coupled logic (SCL) single stage (Figure 3.27(a)).
2. Built with saturated delay (SD) single stage (Figure 3.27(b)).

An example of an $N = 5$, $S = 3$ differential NSRO is shown in Figure 3.27(c).

FIGURE 3.27: Single differential stage schematics of (A) source-coupled logic (SCL) type and (B) saturated delay (SD) type. (C) Schematic of an $N = 5$, $S = 3$ differential NSRO.

The analyses in Section 3.2.2 and Section 3.2.3 can be extended to a SCL differential NSRO without any loss in generality. Similar to a SE NSRO, there are also two transconductances per stage in a SCL differential NSRO. The differential input transistors of a SCL stage can be treated as the NMOS and PMOS of a SE inverter stage. Hence, similar to a SE NSRO, there are also multiple oscillating

edges coexisting in a SCL differential NSRO that increase its oscillation frequency. The final oscillation mode at steady state is determined by the interactions between all of the transconductances during transient. The SCL differential NSRO also achieves the optimum oscillation operations of the SE cases that are described in Section 3.2.2.

However, the extension of the above analyses to a SD differential NSRO is not as straightforward. Its cross-coupled feedback PMOS transistors in each of its stages serve as another set of inputs. Hence, in its small signal analysis, the $N \times N$ matrix formed from its system of first-order linear differential equations (i.e. Equation (3.31)) has additional terms as compared to that of a SE NSRO. Therefore, the resulting eigenvalues and general solutions for the SD differential NSRO are affected. Nevertheless, by sizing the transistors of a SD stage appropriately, optimum oscillation operations of the SE cases as described in Section 3.2.2 can be obtained.

3.2.5 Phase Noise Analysis

Phase noise is an important consideration for any oscillator design. However, a full phase noise analysis is non-trivial, and is highly dependent on the architecture of the oscillator in question. Hence, the aim of this section is not to give full phase noise analyses for the 3 architectures of NSRO presented. Instead, the general impact to phase noise due to the application of the negative skewed delay scheme will be briefly investigated.

3.2.5.1 White Noise Sources

For an oscillator in general, its period (t_{osc}) may be defined as the time interval between two successive crossings of a reference point by the same rising edge of its oscillation. The presence of phase noise modulates this time interval, causing the period to form a set of discrete random variables when measured over time. Its standard deviation (σ_{tosc}) is defined as the periodical jitter.

Assuming that all sources contributing to phase noise arise from white noise only, [19] simplifies the general form of the link between jitter and phase to the

following equation.

$$\mathcal{L}(f) = \sigma_{tosc}^2 \frac{f_{osc}^3}{f^2} \quad (3.34)$$

where $\mathcal{L}(f)$ is the single-sideband (SSB) phase noise power spectral density (PSD) of the oscillator at moderate frequency offsets of f , and f_{osc} is the oscillation frequency of the oscillator.

Since Equation (3.34) is a general form, it can be applied to both a conventional ring oscillator and an NSRO as follows.

$$\mathcal{L}_C(f) = \sigma_{tc}^2 \frac{f_C^3}{f^2} \quad (3.35)$$

$$\mathcal{L}_S(f) = \sigma_{ts}^2 \frac{f_S^3}{f^2} \quad (3.36)$$

where $\mathcal{L}_C(f)$ and $\mathcal{L}_S(f)$ denote the SSB phase noise PSDs of the conventional ring oscillator and the NSRO, respectively. σ_{tc} and σ_{ts} denote the periodical jitter of the conventional ring oscillator and the NSRO, respectively.

The impact to phase noise when the negative skewed delay scheme is applied can be predicted by comparing Equation (3.35) to Equation (3.36). It can be observed that the SSB phase noise PSD of an NSRO will be affected by:

- The increase of the oscillation frequency from f_C to f_S .
- The change in periodical jitter from σ_{tc} to σ_{ts} .

For the former, its impact to phase noise is straightforward. The SSB phase noise PSD of the NSRO will be simply increased by $(f_S/f_C)^3$. Note that the ratio of f_S/f_C is smaller than the number of oscillating edges that the NSRO is supporting (i.e. $f_S/f_C < k_{osc}$). However, the change in periodical jitter is not as simple.

Firstly, it is assumed that all white noise sources are uncorrelated. As discussed in Section 3.2.2, there are k_{osc} oscillating edges propagating within an NSRO. As these oscillating edges propagate through the NSRO, they are independently sped up or slowed down by identical white noise sources in the NSRO. Hence, the k_{osc} oscillating edges have individual periodical jitter, but are identically distributed.

A second assumption is made here. It is assumed that the periodical jitter of an oscillating edge in an NSRO (σ_{tse}) is equal to that of a conventional ring oscillator

(i.e. $\sigma_{tse} = \sigma_{tc}$). In the NSRO, its k_{osc} oscillating edges are physically spaced approximately $2\pi/k_{osc}$ phase apart from one another in the ring. Hence, these k_{osc} oscillating edges will alternatively pass through a stage of the NSRO in repeated sequence. For example, in the $N = 11$, $S = 9$ NSRO as shown in Figure 3.21, Stage 3 will see edge A, followed by edge B, then edge A, then edge B, and so on. Therefore, the effective jitter of the rising edges at that stage is an average of the individual jitters of the k_{osc} oscillating rising edges that are passing through that stage. Since these k_{osc} oscillating edges are independent and identically distributed, σ_{ts}^2 will be smaller than σ_{tc}^2 ($= \sigma_{tse}^2$) by a factor of k_{osc} .

However, the second assumption is a poor assumption, i.e. $\sigma_{tse} \neq \sigma_{tc}$. The difference between the periodical jitter of an oscillating edge in an NSRO and that of its conventional ring oscillator is highly dependent on the ring oscillator architecture. Hence, this difference cannot be generalized.

In short, assuming all noise sources are white, the phase noise of an NSRO as compared to its conventional ring oscillator will be degraded by $(f_s/f_C)^3$, improved by k_{osc} due to the averaging effect, and affected by the difference between the periodical jitter of an oscillating edge in the NSRO (σ_{tse}) and that of its conventional ring oscillator (σ_{tc}).

3.2.5.2 Flicker Noise

Considering only flicker noise, the impact to phase noise due to application the negative skewed delay scheme can be estimated using the impulse sensitivity function (ISF) analysis [80].

For a ring oscillator in general, [80] shows that the $1/f^3$ corner frequency (f_{1/f^3}) of its phase noise spectrum is related to the $1/f$ noise corner ($f_{1/f}$) through the following relationship.

$$f_{1/f^3} = f_{1/f} \cdot \frac{3}{2\eta N} \cdot \frac{(1-A)^2}{(1-A+A^2)} \quad (3.37)$$

where

$$A \equiv \frac{f'_r}{f'_f}$$

η is a proportionality constant, f'_r and f'_f are the maximum slopes of the rising and falling edges, respectively.

Hence, from Equation (3.37), it can be seen that the amount of $1/f$ noise upconversion is minimized when the rising and falling edges are perfectly symmetrical [80]. For an NSRO, as discussed in Section 3.2.1, there are more contention during the rising edge transition and less during the falling edge transition (or vice versa). In other words, the transition edges of an NSRO are more asymmetrical as compared to that of a conventional ring oscillator. An example of this asymmetry is shown in Figure 3.17(c). Hence, there is more upconversion of $1/f$ noise in an NSRO, degrading its close-in phase noise.

3.2.6 Results

Both single-ended (SE) and differential NSROs with varying N and S configurations are simulated and measured to validate the proposed analysis. Simulations are done in a standard 40 nm/1.1 V CMOS technology, whereas the test chip is fabricated in a standard 0.18 μm /1.8 V CMOS technology due to its lower cost. The test chip contains 28 different configurations of NSROs, including conventional cases (i.e. $N = S$) for fair comparison.

Since the main objective is to validate the proposed analysis, the fabricated NSROs have aggressive startup transistors and larger transistor sizes. Therefore, the oscillation frequencies of the fabricated NSROs are generally low. The chip micrograph is shown in Figure 3.28. For odd total number of stages, both configurations of $S = N - 2$ (i.e. $k_{osc} = 2$) and $S = N - 4$ (i.e. $k_{osc} = 3$) are validated. For even total number of stages, optimum S configuration is chosen by satisfying either Equation (3.25) or Equation (3.29) (such that $k_{osc} = 3$).

Multiple chips are measured through probing using Elite300 probe station. However, only 1 set of measurement results will be presented to avoid cluttering the figures. The measured results are similar across all chips. EE4407B spectrum analyzer is used for the phase noise measurements.

FIGURE 3.28: Micrograph of test chip with 28 different configurations of single-ended (SE) and differential NSROs in 0.18 μm /1.8 V CMOS technology.

3.2.6.1 Single-ended NSRO Results

The calculated and simulated oscillation frequencies of SE NSROs (f_S) are plotted in Figure 3.29(a) for $N = 7$ to 22. The calculated values are obtained using Equation (3.15) together with the rising (τ_{drs}) and falling (τ_{dfs}) edge transition times from simulations. These plots are categorized into N being odd or even, and for $k_{osc} = 2$ or 3.

It can be seen from Figure 3.29(a) that the calculated and simulated oscillation frequencies of these SE NSROs are in good agreement. The good agreement between the calculated and simulated values validates that there are 2 or 3 oscillating edges coexisting inside these NSROs. In addition, the simulated overall phase sequences of these NSROs are as predicted by Section 3.2.2.

The presence of multiple oscillating edges in SE NSROs is further validated by the measurement results. The measured oscillation frequency improvements of SE NSROs over their conventional cases (i.e. f_S/f_C) are plotted in Figure 3.29(b) for $N = 9, 10, 13$ and 16.

It can be seen that the oscillation frequency improvements for odd N and even N configurations are around 1.21–1.69 and 1.96–2.16, respectively. These frequency improvements are much lower than the ideal values of $k_{osc} = 2$ or 3 due to the larger rising and falling edge transition times. A contributing factor to the increase in edge transition times is the additional routings required to apply the

(A)

(B)

FIGURE 3.29: (A) Calculated and simulated f_s of SE NSROs for $N = 7$ to 22 with varying S configurations such that $k_{osc} = 2$ or 3. They are in good agreement. (B) Measured f_s/f_c of SE NSROs for $N = 9, 10, 13$ and 16.

negative skewed delay scheme. These routing overheads add significant amount of parasitic loadings to an NSRO.

The Power-Delay-Products (PDP) of the fabricated SE NSROs are plotted in Figure 3.30. Since the application is for a TDC, the tap-to-tap delays of these NSROs are used for the PDP calculations. It can be seen that the PDPs of NSROs are higher as compared to that of their conventional cases. The higher PDPs of NSROs can be partially attributed to the additional routing parasitics as well.

Using both Figure 3.29 and Figure 3.30, configurations with odd total number of stages are compared. It can be seen that although $S = N - 4$ (i.e. $k_{osc} = 3$) configurations have higher oscillation frequencies as compared to $S = N - 2$ (i.e.

FIGURE 3.30: Measured PDPs of SE conventional ring oscillators and NSROs. Negative skewed even N configurations consume least additional power as compared to conventional ring oscillators.

$k_{osc} = 2$) configurations, it comes at a trade-off of higher power consumption (or higher PDPs). $S = N - 4$ configurations consume more power due to their larger contentions between their NMOS and PMOS during their edge transitions.

In addition, configurations that achieve $k_{osc} = 3$ are compared. It can be seen that even N configurations have higher oscillation frequencies with lower PDPs as compared to odd N , $S = N - 4$ configurations. The better performance of even N configurations is attributed to their comparatively smaller contentions between their NMOS and PMOS during their edge transitions.

Overall, the results show that SE NSRO configurations with even total number of stages outperform their odd total number of stages counterparts, and hence, are more suitable for use by a TDC.

3.2.6.2 Differential NSRO Results

Similarly, the extension of the negative skewed delay scheme to differential ring oscillators is also verified by the measurement results. The measured oscillation frequency improvements of differential NSROs over their conventional cases (i.e. f_s/f_C) are plotted in Figure 3.31 for $N = 11$ to 20. For $N = 11, 12, 14$ and 15, these NSROs are built using source-coupled logic (SCL) stages. For $N = 17-20$, these NSROs are built using saturated delay (SD) stages.

FIGURE 3.31: Measured f_s/f_c of differential NSROs. $N = 11, 12, 14$, & 15 differential NSROs and $N = 17$ to 20 differential NSROs are built using SCL and SD stages, respectively.

As can be seen, the oscillation frequency improvements for the odd N and even N configurations are around 1.35–2.51 and 1.92–2.61, respectively. Similar to the SE NSRO cases, the oscillation frequency improvements are lower than the ideal values of $k_{osc} = 2$ or 3 due to the larger edge transition times. The additional routing parasitics introduced are also a contributing factor to the larger edge transition times. The overall phase sequences of these differential NSROs are also as predicted by Section 3.2.2, verifying that there are 2 or 3 oscillating edges coexisting within these NSROs.

The PDPs of SD differential NSROs are plotted in Figure 3.32. It can be seen that the PDPs of these SD differential NSROs are lower as compared to that of their conventional cases. The lower PDPs of these SD differential NSROs indicate that they are more power efficient, where the increase in their oscillation frequencies is more than the increase in their power consumption. This better power efficiency is in spite of the additional routing parasitics that are introduced into the SD differential NSROs.

The PDPs of SCL differential NSROs are not shown as their power consumption are independent of their oscillation frequencies and S configurations. The power consumption of a SCL differential NSRO can be expressed as follows.

$$Power = N \cdot I_{tail} \cdot V_{DD} \quad (3.38)$$

FIGURE 3.32: Measured PDPs of SD differential NSROs. Their conventional cases are also plotted. Negative skewed even N cases have the best PDP performances.

where I_{tail} is the tail bias current for each SCL stage. Hence, the power consumption of a SCL differential NSRO only depends on its total number of stages. In other words, the PDP trend of SCL differential NSROs will simply follow their f_S/f_C trend.

From Figure 3.31 and Figure 3.32, it can be seen that differential NSRO configurations with even total number of stages also outperform their odd total number of stages counterparts in terms of both oscillation frequency and PDP. Hence, configurations with even total number of stages are also preferred for differential NSROs.

Therefore, the extension of the negative skewed delay scheme to differential ring oscillators can improve their oscillation frequencies by more than 200 %. Although the negative skewed delay scheme is less effective as compared to the more commonly used multi-path technique in terms of oscillation frequency improvement, the former does not require any additional transistors. Since there are comparatively fewer active devices in an NSRO, it means that there are fewer noise sources in the NSRO. Therefore, an NSRO can potentially have a better phase noise performance as compared to a ring oscillator employing the multi-path technique. Both the negative skewed delay scheme and the multi-path technique suffer from the same additional routing overhead issue.

TABLE 3.3: Performance Comparison Between Negative Skewed and Other Reported Multi-Path Differential Ring Oscillators

Ring Oscillator:	This Work	PLL 2012 [81]	PLL/TDC 2013 [38]	VCO 2011 [77]	This Work
Architecture ^a	C	MP	MP	MP	NS
Tech. (μm)	0.18	0.13	0.13	0.18	0.18
Total Stages, N	18	4	4	4	18
Period/ N (ns)	4.17	0.10	0.10	0.13	1.83
Power (mW)	2.09	8.25	7.22	13.0 ^b	2.46
PDP (pJ)	8.73	0.86	0.75	1.75 ^b	4.50
PN ^a (dBc/Hz)	-83.67	-120.00	-91.70	-102.00	-74.98
at f offset	100 kHz	10 MHz	1 MHz	1 MHz	100 kHz
FoM_{RO} (dBc/Hz)	-122.95	-158.44	-150.72	-156.26 ^b	-120.72
Area/ N (μm^2)	274	1145	9525 ^c	595	336

^aC: Conventional / MP: Multi-Path / NS: Negative Skewed / PN: Phase Noise

^bPower including buffers

^cArea including TDC

A comparison between negative skewed and other reported multi-path differential ring oscillators is shown in Table 3.3. The Figure-of-Merit (FoM_{RO}) is calculated as follows.

$$FoM_{RO} = \mathcal{L}(f) - 20 \log \left(\frac{f_{osc}}{f} \right) + 10 \log \left(\frac{Power}{1\text{mW}} \right) \quad (3.39)$$

where $\mathcal{L}(f)$ and f_{osc} denote the SSB phase noise PSD and the oscillation frequency, respectively, regardless of architecture. Power is measured in mW. As mentioned, the main objective of this work is to validate the proposed analysis. Hence, it is difficult to have a fair comparison between this and other works. Nevertheless, it can be seen from Table 3.3 that the negative skewed delay scheme can potentially be better than the multi-path technique in terms of power consumption and area efficiency.

A general trend can be observed from Figure 3.29 to Figure 3.32. The longer the length of an NSRO, the least effective the negative skewed delay scheme will be. This trend is resultant from the larger routing parasitics that will be introduced when the total number of stages is larger.

TABLE 3.4: Measured Phase Noise Performances of Fabricated Single-Ended NSROs Divided-by-32 Outputs

Single-Ended NSROs					
N, S	$f_S/32$ (MHz)	Power (μ W)	PN @ 100 kHz (dBc/Hz)	PN @ 1 MHz (dBc/Hz)	FoM_{RO} @ 1 MHz (dBc/Hz)
9, 9	2.65	65.07	-99.90	-121.48	-141.82
9, 7	3.46	134.64	-99.49	-122.14	-141.63
9, 5	4.49	214.20	-95.65	-123.00	-142.74
10, 3	5.16	184.50	-98.98	-121.56	-143.15
13, 13	1.83	64.51	-102.45	-120.28	-137.45
13, 11	2.22	136.13	-101.88	-120.88	-136.47
13, 9	2.62	213.12	-100.04	-121.51	-136.58
16, 7	2.92	191.34	-100.10	-122.26	-138.74

3.2.6.3 Phase Noise Results

The measured phase noise performances of all the fabricated NSROs divided-by-32 outputs¹ are tabulated and compared in Table 3.4 to Table 3.6.

For fair comparison, the phase noise performances are compared at the same frequency offsets from the center frequency. For differential NSROs, due to the low divided-by-32 oscillation frequencies for some of these NSROs, their phase noise performances are measured at relatively low frequency offsets (at 10 kHz, 30 kHz, and 100 kHz offsets) in order to avoid their 2nd harmonic. Hence, only their close-in phase noise due to the upconversion of flicker noise can be compared. For single-ended (SE) NSROs, the frequency offset of 1 MHz is after the $1/f$ corner of their phase noise spectrums. Hence, their phase noise due to white noise sources can be compared.

Note that there are anomalies in the measured phase noise performances. The measured phase noise performances of the $N = 12, S = 5$ SCL differential NSRO at 10 kHz and 30 kHz offsets, and the $N = 15, S = 11$ SCL differential NSRO at 10 kHz offset are much poorer as compared to the rest. These anomalies are likely

¹Note that $20 \log_{10}(32)$ is not added to the measured phase noise results as the results shown are for divided-by-32 outputs.

TABLE 3.5: Measured Phase Noise Performances of Fabricated SCL Differential NSROs Divided-by-32 Outputs

SCL Differential NSROs					
N, S	$f_S/32$ (kHz)	Power ^a (μ W)	PN @ 10 kHz (dBc/Hz)	PN @ 30 kHz (dBc/Hz)	FoM_{RO} @ 30 kHz (dBc/Hz)
11, 11	53.74	19.80	-81.74	-87.40	-109.50
11, 9	82.18	19.80	-76.81	-86.74	-112.53
11, 7	135.03	19.80	-73.34	-85.97	-116.07
12, 12	49.24	21.60	-84.30	-85.57	-106.53
12, 5	128.58	21.60	-47.45	-60.69	-89.99
14, 14	40.37	25.20	-85.53	-87.96 ^b	-106.52
14, 11	96.56	25.20	-82.03	-87.41	-113.55
15, 15	37.21	27.00	-87.86	-85.08 ^b	-102.64
15, 13	50.18	27.00	-82.34	-86.29	-106.44
15, 11	75.94	27.00	-69.37	-80.38	-104.13

^aCalculated using Equation (3.38).^bOnly about 7 kHz to 10 kHz offset from 2nd harmonic.

TABLE 3.6: Measured Phase Noise Performances of Fabricated SD Differential NSROs Divided-by-32 Outputs

SD Differential NSROs					
N, S	$f_S/32$ (kHz)	Power (mW)	PN @ 10 kHz (dBc/Hz)	PN @ 100 kHz (dBc/Hz)	FoM_{RO} @ 100 kHz (dBc/Hz)
17, 17	401.51	2.09	-94.76	-112.64	-121.52
17, 15	776.37	2.23	-94.00	-109.24	-123.55
17, 13	886.03	2.43	-92.40	-107.44	-122.53
18, 18	416.39	2.09	-98.14	-113.77	-122.95
18, 5	949.41	2.46	-92.22	-105.08	-120.72
19, 19	398.32	2.06	-100.37	-113.55	-122.42
19, 17	699.18	2.28	-94.04	-110.54	-123.85
19, 15	758.07	2.46	-91.86	-108.84	-122.52
20, 20	380.49	2.05	-100.05	-113.55	-122.04
20, 9	731.48	2.47	-92.58	-107.95	-121.31

due to artifacts from the poorly optimized chip and measurement setup for phase noise measurements.

From Table 3.4, the phase noise performances of SE NSROs at 1 MHz offset are compared. There is a trend where the phase noise due to white noise sources slightly improves when the negative skewed delay scheme is applied. The phase noise improves by up to about 1.5 dBc/Hz. Referring to Equation (3.35) and Equation (3.36), this trend can be attributed to the lower f_S/f_C ratios of SE NSROs. This trend also indicates that the periodical jitters of SE NSROs are much better as compared to that of their conventional cases. Therefore, the negative skewed delay scheme is especially beneficial for applications such as TDCs and clock and data recovery (CDR) systems where jitter is more important than phase noise performance.

The impact to phase noise due to the upconversion of flicker noise can be observed from the rest of the measured phase noise performances (i.e. from SE NSROs at 100 kHz offset, differential NSROs at 10 kHz, 30 kHz, and 100 kHz offsets). In line with Section 3.2.5.2, the phase noise due to the upconversion of flicker noise degrades when the negative skewed delay scheme is applied. Ignoring the anomalies, the phase noise degrades by up to about 8.5 dBc/Hz. The greater asymmetry between the rising and falling edges in these NSROs causes more upconversion of $1/f$ noise. However, it is worth pointing out that the asymmetrical rising and falling edges of an NSRO can be easily rebalanced through proper sizing of its transistors. Therefore, the amount of $1/f$ noise upconversion in an NSRO can be minimized.

Overall, NSROs with total number of stages (N) varying from 9 to 20 are measured. The measurement results validate the proposed analysis of the negative skewed delay scheme, the extension of this scheme to differential ring oscillators, and the impact of this scheme to phase noise.

3.3 Summary

In summary, this chapter has investigated two building blocks of TDCs.

1. A novel edge comparator that achieves an input time hysteresis window of about 55 fs is proposed. The input time hysteresis effect enables the proposed edge comparator to be more robust against noise and jitters. Hence, the proposed edge comparator is more reliable when comparing inputs with slow varying time differences, or when comparisons are repeated.

The input time hysteresis effect is achieved through the SR latch memory effect, and the two additional M11 and M12 NMOS transistors connected in a negative feedback manner.

The presence of the input time hysteresis effect is verified through chip measurements.

2. A time-domain analysis featuring the sequence tree for a ring oscillator employing the negative skewed delay scheme is proposed. The proposed time-domain analysis accounts for the large improvement in oscillation frequency, and is efficient in quickly determining the optimum configuration and behavior of an arbitrary length NSRO.

Small signal analysis of an NSRO is also presented to supplement the time-domain analysis. The small signal analysis characterizes the general behavior of an NSRO.

In addition, the extension of the negative skewed delay scheme to differential ring oscillators is demonstrated. Therefore, differential ring oscillators can also reap the benefits of employing this scheme.

The impact to phase noise due to the application of the negative skewed delay scheme is also briefly investigated. It depends on the amount of frequency improvement, the number of oscillating edges, the periodical jitter of an oscillating edge, and the symmetry between the rising and falling edges of an NSRO.

Both simulated and measurement results are obtained to validate all the above discussions. The results also show that an NSRO with even total number of stages instead of odd total number of stages could be used to achieve a higher oscillation frequency while consuming lower power.

The improvement of the edge comparator and the understanding of the negative skewed delay scheme for ring oscillators facilitate the design of a high performance TDC for the overall time-mode ADC.

Chapter 4

Branching TDC Architecture

TIME-to-Digital converter is one of the two main building blocks of a time-mode ADC. It converts the time difference that is generated by the VTC into its digital representation, thereby completing the analog-to-digital conversion.

After the investigation of the TDC building blocks in Chapter 3, this chapter proposes a suitable TDC architecture for the time-mode ADC. The TDC should fulfill the following requirements so as to meet the targeted specifications of the time-mode ADC (Table 2.3).

- Achieve a sub-gate delay TDC time resolution of about 5 ps.
- Have a large measurement range of more than 8-bit.
- Achieve good linearity performances.
- Scale well with advancing CMOS technology.

As mentioned, the ring oscillator based TDC is an effective architecture that achieves the required wide measurement range. However, its TDC time resolution is limited by the tap-to-tap delay of its ring oscillator.

In order to achieve a fine TDC time resolution of about 5 ps, a novel branching TDC architecture is proposed. Similar to the ring oscillator based TDC, the proposed architecture also uses a ring oscillator as its core to quantize the input time difference. The difference is that it uses a proposed branching phase interpolation technique to interpolate between the tap-to-tap phases of the ring oscillator.

Hence, the TDC time resolution of this TDC architecture is improved, and is not limited by the tap-to-tap delay of the ring oscillator. The required TDC time resolution can be achieved by the proposed architecture given sufficient interpolation factor. In addition, the proposed branching technique is compatible with CMOS scaling. The phase interpolation can be achieved via two means:

1. Through deterministic positioning of the interpolating edges.
2. Through stochastic positioning of the interpolating edges.

This chapter is split into two main parts. The first part presents a branching TDC implementation that utilizes the first method, whereas the second part presents another implementation that utilizes the second method.

The first method is verified using a prototype chip fabricated in a standard 40 nm CMOS technology, whereas the second method is verified through simulations in a standard 65 nm CMOS technology.

Note that all TDC implementations presented in this thesis only utilize rising edges in their time quantizations. If both the rising and falling edges are used, it will incur linearity errors resulting from the mismatch between the rising and falling edges. Hence, the use of both rising and falling edges is avoided.

4.1 12-bit Branching TDC

In the first part of this chapter, a 12-bit branching TDC implementation in a standard 40 nm CMOS technology is presented. This TDC implementation serves as a proof of concept for the proposed branching phase interpolation technique, and will be referred to as the BTDC prototype.

In this BTDC prototype, the proposed branching phase interpolation technique interpolates between the tap-to-tap rising edges of a core 16-stage gated ring oscillator (GRO) by a factor of 4. Hence, the TDC time resolution of this BTDC prototype is $4\times$ finer than the propagation delay of 2 inverter stages in the GRO.

In the voltage domain, the reliability and accuracy of an ADC are highly dependent on the performance of its voltage reference. An ADC will only be as accurate

as its voltage reference. The same is true in the time domain. The reliability of this BTDC prototype depends on the accuracy of its TDC time resolution. However, since its TDC time resolution is dependent on the stage delay of its GRO, its TDC time resolution can vary substantially with PVT variations. Hence, this BTDC prototype incorporates fully digital based delay tuning capability into all of its delay stages. This fully digital based delay tuning capability enables its TDC time resolution to be calibrated against PVT variations, while allowing it to scale with advancing CMOS technology.

Despite the importance of the TDC time resolution to the reliability of the TDC, many TDCs in the literature, such as [24, 29, 34, 35, 49, 56, 62, 64, 82], do not address the variability issue of its TDC time resolution. Note that calibrations for improving the linearity of a TDC is different from calibrations for minimizing the changes of a TDC time resolution. The former is associated with the uniformity between all of the TDC time quantization steps, whereas the latter is associated with the average time quantization step size.

This BTDC prototype also features several power saving techniques. Hence, it only consumes a low average dynamic power consumption of 275 μW at a sampling rate of 5 MS/s.

The details of this BTDC prototype will be discussed in the following sections.

4.1.1 Branching Phase Interpolation Technique

Firstly, the operational principle of the branching phase interpolation technique that is employed in a branching TDC is explained in this section.

4.1.1.1 Phase Interpolation Principle

The simplified circuit schematic and timing diagram for an example of the branching phase interpolation technique are shown in Figure 4.1(a) and Figure 4.1(b), respectively. The circuit consists of a core N_{RO} -inverter-stage ring oscillator, and N_{BDL} -inverter-stage branching delay lines. Their configuration is such that a branching delay line extends out from each output tap of the ring oscillator. Therefore, the term “branching” is used to describe this technique. In total, there

will be N_{RO} branching delay lines. This whole structure is defined as the branching ring oscillator. In the example of Figure 4.1, $N_{RO} = N_{BDL} = 3$.

FIGURE 4.1: Branching phase interpolation principle. The branching delay lines enable $4\times$ phase interpolation between the tap-to-tap phases of the ring oscillator to be achieved. (A) Simplified circuit schematic. (B) Timing diagram.

Firstly, it is assumed that the propagation delays of a stage for a rising and a falling edge transition are equal. In addition, the rising edges of the ring oscillator are defined to occur at even integers of phase π (i.e. at phases 0, 2π , 4π , and so on). Hence, the falling edges of the same will occur at odd integers of phase π (i.e. at phases π , 3π , and so on). In other words, the inverter stage delay of the ring oscillator (τ_{RO}) is equal to π .

Since the ring oscillator provides and feeds both rising and falling edges into the branching delay lines, the N_{BDL} -stage branching delay lines can produce N_{BDL}

additional rising edges in between two tap-to-tap rising edges of the ring oscillator. These additional rising edges interpolate the output taps of the ring oscillator by a factor of $N_{BDL} + 1$. This behavior is illustrated in Figure 4.1(b). Therefore, the interpolation factor (IF) of the branching technique can be expressed as follows.

$$IF = N_{BDL} + 1 \quad (4.1)$$

In order to interpolate between the output taps of the ring oscillator, the inverter stage delay of the branching delay lines (τ_{DL}) is designed to be a fraction of 2 inverter stages delay of the ring oscillator. This relationship can be expressed as follows.

$$\frac{\tau_{DL}}{2\tau_{RO}} = \frac{x}{IF} \quad (4.2)$$

where x is designed to be an integer.

A rising edge fed to an N_{BDL} -inverter-stage branching delay line will produce rising edges at even positions along this delay line, whereas a falling edge input will produce rising edges at odd positions along this delay line. Hence, the phases of the rising edges produced by this branching delay line can be expressed as follow.

$$\{\phi_{DL\text{Even},i}\} = \{2i\tau_{DL}\} \quad , \quad \text{for } i = 1 \text{ to } \frac{N_{BDL} - 1}{2} \quad (4.3)$$

$$= \left\{ \frac{2ix}{IF}(2\pi) \right\}$$

$$\{\phi_{DL\text{Odd},j}\} = \{\tau_{RO} + \tau_{DL} + 2j\tau_{DL}\} \quad , \quad \text{for } j = 0 \text{ to } \frac{N_{BDL} - 1}{2} \quad (4.4)$$

$$= \left\{ \frac{0.5IF + (2j + 1)x}{IF}(2\pi) \right\}$$

where $\{\phi_{DL\text{Even}}\}$ and $\{\phi_{DL\text{Odd}}\}$ are phases of the rising edges at even and odd positions, respectively, along this branching delay line. Note that the intrinsic phase difference of π or τ_{RO} between the rising and falling edges from the ring oscillator is encompassed within Equation (4.3) and Equation (4.4). In addition, the 2π phase wrap around effect can be applied to both of these equations to express their solutions within a phase of 2π .

In order for the overall branching TDC to have a good linearity, the interpolating rising edges from the branching delay lines should be spaced evenly between

two tap-to-tap rising edges of the ring oscillator. In other words, the following conditions should be satisfied.

1. The combined N_{BDL} phases of Equation (4.3) and Equation (4.4) should be positioned at phases $\left\{\frac{v}{IF}(2\pi)\right\}_{v=1}^{N_{BDL}}$.
2. The interpolation factor should be an even integer.

The first condition can be expressed as follows.

$$\left\{\phi_{DLeven,i}\right\}_{i=1}^{\frac{N_{BDL}-1}{2}} \cup \left\{\phi_{DLOdd,j}\right\}_{j=0}^{\frac{N_{BDL}-1}{2}} = \left\{\frac{v}{IF}(2\pi)\right\}_{v=1}^{N_{BDL}} \quad (4.5)$$

Hence, the inverter stage delay of the branching delay lines should be designed using Equation (4.1) and Equation (4.2) to satisfy Equation (4.5) (i.e. the choice of x depending on N_{BDL}). For the example illustrated in Figure 4.1, x is designed to be 3. An example that does not satisfy Equation (4.5) is when $N_{BDL} = 5$ and $x = 2$.

The second condition arises from the use of both rising and falling edges as inputs to the branching delay lines. If the interpolation factor is not even, the first condition can not be satisfied.

In short, the combination of all the rising edges produced enables the branching delay lines to interpolate between the tap-to-tap phases of the ring oscillator. This interpolation increases the N_{RO} oscillation phases of the ring oscillator by a factor of IF . Thereby, enabling the TDC time resolution of the branching TDC to be $IF \times$ finer than if it is limited by 2 inverter stages delay of the ring oscillator. This branching TDC is another type of a phase interpolation TDC (Section 2.2.3). In general, the TDC time resolution (T_{LSB}) of the branching TDC can be expressed as follows.

$$T_{LSB} = \frac{t_{RO}}{N_{RO}(IF)} = \frac{2\tau_{RO}}{IF} \quad (4.6)$$

where t_{RO} is the oscillation frequency of its ring oscillator.

However, the loading of the branching delay lines to the ring oscillator increases the inverter stage delay of the ring oscillator. Hence, the intrinsic time resolution of the ring oscillator is degraded. The increase of the inverter stage delay is independent of the number of stages in the branching delay lines. Hence, for this

branching technique to be effective, the number of stages in the branching delay lines should be large. The maximum length of a branching delay line is limited by the accumulated jitter along this branching delay line. This accumulated jitter should not exceed the TDC time resolution of the branching TDC.

Since the TDC time resolution is usually in tens of picoseconds or less, the elapsed time that is required for the accumulated jitter to reach this amount can be assumed to be small. Hence, slow varying flicker noise can be neglected. Assuming that the rest of the noise sources are white and uncorrelated, the noise inducing jitter in each of the edge transitions add in the mean-square [19]. Hence, the maximum length of a branching delay line can be expressed as follows.

$$T_{LSB} > \sigma_{DL,N} = \sqrt{N_{BDL}} \sigma_{DL,s} \quad (4.7)$$

where $\sigma_{DL,s}$ is the jitter of an inverter stage in the branching delay line, and $\sigma_{DL,N}$ is the accumulated jitter at the N_{BDL} -stage of the branching delay line.

Note that Equation (4.2) to Equation (4.4), and the second condition of even interpolation factor are not strictly binding. The underlying principle of the proposed branching phase interpolation technique is to use a stage of a branching delay line to create an additional rising edge in between 2 rising edges from the ring oscillator. This additional rising edge increases the number of oscillation phases of the ring oscillator, thereby enabling a finer TDC time resolution to be achieved.

4.1.1.2 Advantages of Proposed Branching Technique

An advantage of the proposed branching phase interpolation technique is as follows. Even if only rising edges are used in the time quantization process, the ring structure of the branching architecture enables every single inverters to be utilized efficiently. This efficient utilization of all inverters is demonstrated in Figure 4.1. In comparison to conventional delay line TDC, Vernier delay lines TDC, or parallel delay lines TDC, half of their inverters will not be utilized for time quantization if only rising edges are considered. These unutilized inverters are only used to built the buffers in these TDC architectures.

Another advantage of the proposed branching phase interpolation technique is its power gating feature. The branching delay lines can be power gated and disabled

when the phase of the branching ring oscillator do not need to be sampled. The power gating of the branching delay lines reduces power consumption, especially if the input time difference to the branching TDC is large.

The oscillations of the branching ring oscillator originate from the core ring oscillator. Hence, the phase information of the entire branching ring oscillator will not be lost even if the branching delay lines are disabled. This property is valid as long as the phase of core ring oscillator is maintained. When sampling of the branching ring oscillator phase is required, the branching delay lines can be re-enabled. Given an initial setup time, the branching delay lines will reproduce the interpolating rising edges using the oscillations from the core ring oscillator. Therefore, the phase of the entire branching ring oscillator can be recovered for sampling.

The minimum setup time required (t_{su}) for the interpolating rising edges to be produced can be derived as follows. The branching ring oscillator has the following properties:

- Since the inputs of the branching delay lines are fed from the core ring oscillator, the phase difference between two branching delay lines extending out from two consecutive rising edges taps of the ring oscillator is 2π .
- Equation (4.5) established that the N_{BDL} interpolating edges are each produced by a particular stage along a branching delay line.

Both of these properties can be observed from Figure 4.1.

After re-enabling the branching delay lines, a first edge will be produced by the ring oscillator at one of its output taps. This first edge will start to propagate through the branching ring oscillator, causing the interpolating rising edges to be produced by the branching delay lines. After a period of time, this first edge will reach the ends of the first two branching delay lines that it is fed into. This process can be described by Equation (4.3) and Equation (4.4), and is illustrated in Figure 4.2. The longest period of time for this process to occur is the minimum setup time required. After this point in time, due to the two aforementioned properties of the branching ring oscillator, all of the N_{BDL} interpolating rising edges in the next 2π window will be ready as they are produced by the subsequent branching delay lines.

FIGURE 4.2: Illustration of the first edge produced by the ring oscillator propagating through and reaching the ends of the first two branching delay lines that it is fed into.

If the first edge produced by the ring oscillator is a rising edge, the setup time required can be derived using Equation (4.3) and Equation (4.4) as follows.

$$\begin{aligned} t_{su} &= \{\phi_{DLodd,j}\}_{j=\frac{N_{BDL}-1}{2}} \\ &= \frac{0.5IF + xN_{BDL}}{IF}(2\pi) \end{aligned} \quad (4.8)$$

If the first edge is a falling edge, modifying Equation (4.3) and Equation (4.4) accordingly, the setup time required can be derived as follows.

$$t_{su} = \max\left(\frac{0.5IF + x(N_{BDL} - 1)}{IF}(2\pi), \frac{xN_{BDL}}{IF}(2\pi)\right) \quad (4.9)$$

In this case, the setup time required depends on x and N_{BDL} . It can be seen that Equation (4.8) is always larger than Equation (4.9). Hence, the minimum setup time required can just be described by Equation (4.8). For the example shown in Figure 4.1, the minimum setup time required is 5.5π or $5.5\tau_{RO}$.

The amount of power savings from this power gating feature can be demonstrated by the BTDC prototype. From simulations, applying a full range input time difference of 148 ns to the BTDC prototype, this power gating feature saves 24.4 % of power as compared to if no power gating is applied.

Lastly, another advantage of the proposed branching phase interpolation technique is that the branching TDC formed will be able to scale well with advancing CMOS technology. Being a phase interpolation TDC architecture, the TDC time

resolution of the branching TDC does not depend on the accurate matching between its delay stages. Hence, matching between its delay stages is not that critical, and its delay stages do not need to be sized up. Linearity errors arising from imperfect matching can be corrected using other calibration means. In fact, the size of the delay stages in the branching TDC should be designed to be small. The smaller delay stages have lower propagation delays, thereby enabling a finer TDC time resolution to be achieved. Hence, the scaling of CMOS technology improves the performance of the branching TDC architecture. This property of phase interpolation TDCs is also discussed at the end of Section 2.2.3.

4.1.2 Branching TDC Prototype Implementation

The block diagram of the 12-bit BTDC prototype is shown in Figure 4.3. It has a coarse-fine TDC architecture.

FIGURE 4.3: Block diagram of the 12-bit BTDC prototype. It composes of a 6-bit ring oscillator based coarse TDC and a 6-bit branching fine TDC.

The coarse TDC is a ring oscillator based TDC, where it uses a core 16-stage gated ring oscillator (GRO) to clock a simple 8-bit counter. It quantizes an input time difference by counting the number of oscillation cycles that the GRO completes within this time period. Hence, the coarse TDC quantizes an input time difference in terms of the oscillation period of its GRO (t_{GRO}). It produces the 6-bit most significant bit (MSB) of the 12-bit output.

The fine TDC uses the proposed branching phase interpolation technique to interpolate between the 16 phases of the core GRO. A branching GRO is implemented where branching gated delay lines (GDL) extend out from the core GRO. As a proof of concept, the length of each GDL is only 3 (i.e. $N_{RO} = 16$, $N_{BDL} = 3$, and $IF = 4$). Therefore, the 16 phases of the GRO is split into 64 finer phases of the branching GRO. The fine TDC further quantizes the input time difference by sampling the START and STOP phases of this branching GRO when the START and STOP signals arrive, respectively. It produces the final 6-bit least significant bit (LSB) of the 12-bit output.

In other words, the BTDC prototype quantizes the input time difference in terms of the overall phase change of its branching GRO. Its TDC time resolution can be expressed using Equation (4.6) as follows.

$$T_{LSB} = \frac{t_{GRO}}{64} \quad (4.10)$$

Since the coarse TDC is a ring oscillator based TDC, the measurement range of the BTDC prototype can be easily extended by using a counter with a longer length. However, as discussed in Section 2.2.4, the measurement range cannot be infinitely large. It is limited by the accumulated jitter of the GRO. If the limited measurement range is relatively short, only uncorrelated white noise sources need to be considered. The maximum length of the counter can be derived as follows, which is similar to Equation (4.7).

$$T_{LSB} > \sigma_{GRO,cm} = \sqrt{32 \cdot 2^{cm}}(\sigma_{GRO,s}) \quad (4.11)$$

where 2^{cm} represents the maximum length of the counter in decimal, $\sigma_{GRO,s}$ is the jitter of a delay stage in the GRO, and $\sigma_{GRO,cm}$ is the accumulated jitter after 2^{cm} cycles of the GRO oscillation. However, if the limited measurement range is large enough for flicker noise to be considered, derivations for the accumulated jitter of the GRO is more complicated. In short, it can be expressed as follows [80, 83].

$$\sigma_{GRO,1/f} = \zeta \Delta T = \zeta(2^{cm} \tau_{GRO}) \quad (4.12)$$

where $\sigma_{GRO,1/f}$ is the accumulated jitter of the GRO due to flicker noise, ζ is a proportionality constant determined by circuit parameters of the GRO, and ΔT

is the elapsed time. The elapsed time can be expressed in terms of the maximum length of the counter and the stage delay of the GRO (τ_{GRO}).

The limited measurement range is demonstrated by the BTDC prototype. Even though its implemented counter is 8-bit long, only the 6-bit LSB of the counter can be used. Beyond 6-bit range, the accumulated jitter of the GRO becomes too large, causing the single-shot precision (SSP) of the BTDC prototype to be much larger than 1 LSB. The measured SSP results is presented later in Section 4.1.3, Figure 4.15 and Figure 4.16. In order to extend the measurement range of the BTDC prototype further, more power has to be consumed by the GRO to reduce its jitter [19].

In the coarse-fine architecture of the BTDC prototype, the fine TDC directly interpolates a cycle of the coarse TDC. Hence, residue generation is not required to interface between the coarse and fine TDCs. However, it also means that the BTDC prototype has an inherent folding nature. Every cycle of the coarse TDC is a repeat of the fine TDC. Therefore, linearity errors from the fine TDC will repeat themselves for the 64 cycles of the coarse TDC operation. This periodicity of the linearity errors will introduce spurs into the output of the BTDC prototype, degrading its spurious-free dynamic range (SFDR).

4.1.2.1 Branching Gated Ring Oscillator

The heart of the 6-bit fine TDC is the branching GRO. Its schematics is shown in Figure 4.4. It is built using a 16-stage GRO, fifteen 3-stage branching GDL, and a 4-stage branching GDL.

The 16-stage GRO employs the negative skewed delay scheme previously discussed and analyzed in Section 3.2 to increase its oscillation frequency. Hence, a finer TDC time resolution of the BTDC prototype can be achieved. However, it comes at a trade-off of higher power consumption as shown in Section 3.2.6. It is also shown in Section 3.2.6 that NSROs with even total number of stages have better performances. Hence, the GRO for this BTDC prototype is implemented with an $N = 16$, $S = 7$ configuration. Its schematic is illustrated in Figure 4.4(a). Since an NSRO can have multiple modes of oscillation at steady state, this negative skewed GRO is carefully designed to ensure that it oscillates with the optimum oscillation mode.

FIGURE 4.4: Schematics of (A) branching GRO, (B) a GRO delay stage, and (C) a branching GDL delay stage. The GRO is a gated $N = 16$, $S = 7$ NSRO. Digital coarse delay tuning through the header PMOS and footer NMOS transistors, and digital fine delay tuning through the output capacitor bank.

The stage delay of the branching GDLs (τ_{GDL}) can be designed to satisfy Equation (4.5) by sizing its transistors appropriately. For a first round hand design, the stage delay can be estimated using Equation (2.3) to Equation (2.5). However, in the final implementation, the stage delay will vary from stage to stage along a branching GDL. This variation arises from higher order effects, such as the dependency of the stage delay on the rise and fall times of its input edge. Hence, fixed offset MOS capacitors are added along the branching GDLs to fine tune the positions of the interpolating rising edges (each produced by a branching GDL stage). The fixed offset capacitors (C_{OS1} to C_{OS3}) are illustrated in Figure 4.5. Since these capacitors do not load the core GRO, the TDC time resolution of the BTDC prototype is not degraded.

The gating functionality of the branching GRO is implemented using header

FIGURE 4.5: Simplified schematic illustrating the fixed offset capacitors that are added along the branching GDLs to fine tune the positions of the interpolating rising edges.

PMOS and footer NMOS transistors in each of its delay stages. These gating transistors can be seen in the schematics of a GRO delay stage and a branching GDL delay stage as shown in Figure 4.4(b) and Figure 4.4(c), respectively. The gating functionality is used for three purposes:

1. To disable the branching GRO when the BTDC prototype is inactive to save power.
2. To disable the branching GRO for sampling of its phase.
3. To disable the branching GDLs when an input time difference to the BTDC prototype is large (i.e the power gating feature of the branching technique as discussed in Section 4.1.1.2).

The phase sampling operation of the branching GRO will be discussed in detailed in Section 4.1.2.4. The gating functionality is not used to implement the inherent noise shaping capability of the GRO [58]. The noise shaping capability is not employed as it is sensitive to leakages.

In a conventional ring oscillator based TDC, its counter only loads one output tap of its ring oscillator. Since only 1 output tap of the ring oscillator has additional loading as compared to the rest of its output taps, non-linearity will be introduced at that tap. The proposed branching technique can also circumvent this non-linearity issue.

TABLE 4.1: Simulated Oscillation Frequency of the GRO and Resulting TDC Time Resolution at Nominal and Worst Case Corners

Corner	Without Tuning Elements		With Tuning Elements	
	f_{GRO}	T_{LSB}	f_{GRO}	T_{LSB}
TT, 27°C	833.1 MHz	18.8 ps	453.4 MHz	34.5 ps
SS, 125°C	558.1 MHz	28.0 ps	365.2M Hz	42.8 ps
FF, -40°C	1.243 GHz	12.6 ps	606.7 MHz	25.8 ps

In the BTDC prototype, instead of clocking its counter using its GRO, its counter is clocked by the 4th stage of its 4-stage branching GDL. Since the stage delay of this branching GDL satisfies Equation (4.2), the buffered GRO oscillations from the 4th stage of this branching GDL will be oscillating in-phase with an output tap of the GRO. Hence, the loading of the counter can be transferred from the GRO to the 4th stage of this branching GDL, while maintaining the original coarse counter clocking operation. However, the transfer of counter loading comes at a trade-off of higher power consumption. The power gating feature of the branching technique cannot be applied to this 4-stage branching GDL. This 4-stage branching GDL needs to continuously buffer the GRO oscillations to maintain the coarse counter clocking operation.

4.1.2.2 Digital Based Delay Tuning

For the BTDC prototype to be reliably used for time quantizations, its TDC time resolution should be fixed and well defined. As shown by Equation (4.10), its TDC time resolution is directly dependent on the oscillation frequency of its GRO, and hence, the stage delay of its GRO.

It is well known that the propagation delay of a digital gate will vary with PVT variations. This fact applies to the stage delay of the GRO as well. The simulated oscillation frequency of the GRO (f_{GRO}) and the resulting TDC time resolution across nominal and worst case corners are tabulated in Table 4.1. They are simulated with and without any delay tuning elements.

It can be observed from Table 4.1 that without any delay tuning elements, the TDC time resolution of the BTDC prototype can vary by +49 % and -33 % due to PVT variations. This amount of variation is unacceptable for most applications.

Therefore, some form of calibration has to be included into the BTDC prototype to tune its TDC time resolution against PVT variations. For the BTDC prototype, manual foreground calibration is implemented. For simplicity, the GRO oscillation frequency of the BTDC prototype is measured using an oscilloscope. At the same time, its TDC time resolution is tuned to maintain the nominal value using the delay tuning capability that is incorporated into the delay stages of its branching GRO.

In order to allow the BTDC prototype to scale with advancing CMOS technology, the delay tuning capability is implemented using a fully digital structure. For the BTDC prototype, simple digital based coarse and fine delay tuning methods are employed for the delay stages of its branching GRO.

The coarse delay tuning is achieved through current starving of the delay stages. In each of the delay stages, between 2 to 4 header PMOS and footer NMOS transistors can be selected to be connected to its core inverter. These current starving transistors are selected through a coarse tuning code. Since switching these current starving transistors will cause a large change in the bias current of the core inverter, the coarse delay tuning of the delay stages has a non-linear response.

The fine delay tuning is implemented by adding a simple capacitor bank with 12 selectable unit MOS capacitors to the output of each of the delay stages. These MOS capacitors are selected through a fine tuning code. These MOS capacitors are small. Hence, the fine delay tuning response of the delay stages is relatively linear. Both the coarse and the fine delay tuning methods are illustrated in Figure 4.4(b) and Figure 4.4(c). The measured coarse and fine delay tuning responses of the GRO stage delay (τ_{GRO}) are shown in Figure 4.6. In essence, the delay stages form Digital-to-Time converters (DTC).

From the simulation results tabulated in Table 4.1, it can be seen that the simple digital based delay tuning capability of the BTDC prototype has reduced the variation of its TDC time resolution to $\pm 25\%$ across worst case corners. Hence, the BTDC prototype is more tolerant against PVT variations.

In this BTDC prototype, its delay stages are manually foreground calibrated. Hence, the digital tuning codes have to be constantly refreshed as the environment changes. However, for future prototypes, automatic calibration could be applied by using both a PLL and a delay-locked loop (DLL) in the following manner:

- The PLL can be used to lock the oscillation frequency of the GRO to an external PVT stable crystal oscillator.
- The DLL can be used to lock the total delay of a branching GDL to multiple stages delay of the GRO according to Equation (4.2).

(A)

(B)

FIGURE 4.6: Measured coarse and fine delay tuning responses of the GRO stage delay (τ_{GRO}). (A) Individual and (B) combined tuning response.

4.1.2.3 Bridging Fine Delay Tuning Capacitors for GRO

For a delay stage of the GRO, its fine delay tuning capacitor bank is not connected from its output node to ground. Instead of this conventional connection method,

its capacitor bank is connected across the outputs of two delay stages in the GRO as shown in Figure 4.4(b). These two delay stages produce rising edges that are back-to-back during oscillation (i.e. tap-to-tap rising edges). Hence, all of the fine delay tuning capacitors connected across the GRO form a bridge-like ring structure. Each of these capacitors is defined as a bridging capacitor. The bridging capacitors structure is exemplified in Figure 4.7(a) using a conventional 5-stage ring oscillator, where C_B and C_P represent the bridging capacitor and the lumped parasitic output capacitor, respectively.

FIGURE 4.7: (A) Example of a conventional 5-stage ring oscillator with bridging capacitors connected to back-to-back rising edges. (B) Model for a first-order approximation of the effective output capacitance ($C_{O,B}$).

The bridging capacitors structure has 3 advantages over the conventional connection method.

1. The effective capacitance implemented by each bridging capacitor is larger.
2. The bridging capacitors structure implement the spatial mismatch filtering proposed by [39].
3. The voltage swing across a bridging capacitor is smaller. Hence, the bridging capacitor has better linearity.

The following analyses for the bridging capacitors structure assume that the initial conditions for all of the bridging and lumped parasitic capacitors are equal to zero.

Firstly, the bridging capacitors at the output node of a GRO delay stage can be first-order modeled by the model shown in Figure 4.7(b). Hence, the effective output capacitance of the GRO delay stage ($C_{O,B}$) can be first-order approximated by the following expression.

$$\begin{aligned} Z_{O,B} &= Z_P // (Z_B + Z_P) // (Z_B + Z_P) \\ \therefore C_{O,B} &= \frac{C_P(3C_B + C_P)}{C_B + C_P} \end{aligned} \quad (4.13)$$

where

$$Z_{O,B} = \frac{1}{sC_{O,B}}, \quad Z_B = \frac{1}{sC_B}, \quad Z_P = \frac{1}{sC_P}.$$

If a bridging capacitor is conventionally connected from the output node of a GRO delay stage to ground, the effective output capacitance of this GRO delay stage ($C_{O,C}$) can be easily derived to be the following expression.

$$C_{O,C} = C_B + C_P \quad (4.14)$$

Hence, using Equation (4.13) and Equation (4.14), the gain in effective output capacitance of a GRO delay stage due to the application of the bridging capacitors structure can be expressed as follows.

$$\frac{C_{O,B}}{C_{O,C}} = \frac{C_P(3C_B + C_P)}{(C_B + C_P)^2} \quad (4.15)$$

Using values of $C_B = 65$ aF and $C_P = 400$ aF, Equation (4.15) calculates that $C_{O,B}$ will be 10 % larger than $C_{O,C}$. This outcome implies that the effective capacitance implemented by a bridging capacitor is larger when it is connected to the GRO delay stages using the bridging structure. In other words, a larger capacitance can be achieved using a smaller capacitor, saving area for the overall chip.

From simulations, considering the full ring of bridging capacitors, the first-order approximation of Equation (4.13) differs from the actual effective output capacitance of the GRO delay stage by only 0.38 %.

Secondly, the bridging capacitors structure implement spatial mismatch filtering [39]. In an ideal case, the GRO delay stages will produce rising edges that are

evenly spaced in time. However, the inevitable presence of mismatch between the GRO delay stages will skew these evenly spaced rising edges away from their ideal positions as shown in Figure 4.8(a). This skew degrades the DNL and INL of the BTDC prototype. The spatial mismatch filtering proposed by [39] compensates for this skew and shifts the rising edges back to their ideal positions.

FIGURE 4.8: (A) Timing Diagram of spatial mismatch filtering [39]. The skewed rising edge is shifted back to its ideal position. (B) Simplified model in Laplace domain of a GRO delay stage output node with bridging capacitors.

The simplified model in Laplace domain for the output node of a GRO delay stage with bridging capacitors ($V_0(s)$) is shown in Figure 4.8(b). Using this simplified model and Kirchhoff's Current Law (KCL), the current integrated on the output node of this GRO delay stage can be derived as follows.

$$\frac{V_0(s)}{Z_P} = I_0(s) + \frac{\frac{V_3(s) + V_2(s)}{2} - V_0(s)}{Z_B/2} \quad (4.16)$$

where $I_0(s)$ is the current produced by this GRO delay stage, $V_2(s)$ and $V_3(s)$ are the output nodes of the GRO delay stages that produce the adjacent rising edges.

Similar to the analysis in [39], the second term in Equation (4.16) is a compensation current that shifts a skewed rising edge of this GRO delay stage back to its ideal central position. The outcome of this analysis is the same as [39] even though bridging capacitors are used instead of resistors. Since the GRO oscillates, the bridging capacitors effectively act as resistors.

The advantage of using bridging capacitors over resistors is that these bridging capacitors consume comparatively less area. The downside is that these bridging capacitors load the GRO, decreasing its oscillation frequency and degrading the TDC time resolution of the BTDC prototype.

For the BTDC prototype, two fixed bridging capacitors are designed to be always connected in between two GRO delay stages. These two fixed bridging capacitors are in addition to the fine delay tuning capacitor bank, and are not controlled by the fine digital tuning code.

Lastly, as a bridging capacitor is connected in between two back-to-back edges of the GRO, the voltage swing across the bridging capacitor is smaller than rail levels. This voltage swing depends on the delay between the back-to-back edges, and the rise and fall times of the back-to-back edges. The smaller voltage swing of the bridging capacitor enables it to have less variation of its capacitance. Hence, the bridging capacitor is more linear than a capacitor that experiences rail-to-rail voltage swing. From simulations, the maximum voltage across the bridging capacitors in the BTDC prototype is only 51.2 % of V_{DD} .

4.1.2.4 Gated Inverters Based Sampler with Power Gating

Conventionally, arbiters are used to sample the phase of a delay line in a TDC. These arbiters will produce a thermometer code that encompasses the phase of the delay line.

However, in the BTDC prototype, arbiters are not used to sample the phases of its branching GRO on the arrival of the START and STOP signals. Instead of arbiters, simple gated inverters based samplers together with a phase sampling operation are proposed to perform this function. The schematic of a proposed gated inverters based sampler is illustrated in Figure 4.9. It is built using chains of gated inverters and D flip-flops.

The proposed phase sampling operation of the branching GRO is as follows. When the START or STOP signal arrives, the branching GRO will be disabled through its gating transistors. Hence, the output voltages of the branching GRO delay stages will be held by their parasitic output capacitors. Therefore, the phase of the branching GRO can be extracted by sampling each of these held output

FIGURE 4.9: Schematic of a gated inverters based sampler. These samplers extract the phase of the branching GRO by sampling the held voltages of its delay stages. Two separate paths are used for the START and STOP sampling.

voltages in the voltage domain using the proposed sampler. The comparison point is the threshold voltage of the first gated inverter ($V_{th,inv}$) in the proposed sampler. Hence, this proposed phase sampling operation will produce the same thermometer code as though arbiters are used. After phase sampling is completed, the D flip-flops will latch the results, allowing the branching GRO to continue to oscillate.

The proposed phase sampling method has three advantages.

1. The proposed sampler has a simpler structure as compared to a conventional arbiter. Hence, it consumes a smaller amount of area and power as compared to an arbiter. From simulations, toggling both the outputs of a proposed sampler and an arbiter used by [33]¹ at 400 MHz, the former consumes 64.1 % lower power as compared to the latter.
2. The proposed phase sampling operation allows the gated inverters of the proposed sampler to be enabled only when phase sampling of the branching GRO is required. At all other times, the gated inverters can be power gated by disabling them through their header PMOS and footer NMOS transistors, thereby reducing power consumption.

In comparison, arbiters cannot be disabled if they are used to sample the phase of the branching GRO. In order to arbitrate in real-time when the START or STOP signal arrives, the arbiters have to remain in operation.

¹It is in fact the conventional edge comparator defined in Section 3.1.1.

Hence, dynamic power will be consumed by the arbiters as the branching GRO toggles.

The power gating of the gated inverters also prevents short circuit currents from flowing through the gated inverters if their inputs are held in between the supply and ground.

3. If arbiters are used to sample the phase of the branching GRO, two separate arbiters would have to be loaded onto each output node of the branching GRO. These two separate arbiters are required in order to sample the START and STOP phases properly for a small input time difference. A single arbiter will not be able to reset in time to sample both the START and STOP phases properly when the input time difference is small.

In contrast, the proposed sampler only requires one gated inverter to be loaded onto each output node of the branching GRO. Two parallel paths are used in the proposed sampler to sample the START and STOP phases separately. Hence, the START and STOP phases can still be properly sampled by the proposed sampler even when the input time difference is small. This circuit structure of the proposed sampler is illustrated in Figure 4.9.

Since the proposed sampler is working in the voltage domain instead of the time domain, its first gated inverter can act as an amplifying buffer to isolate the output node of a branching GRO delay stage from the two parallel paths. Hence, the proposed samplers do not load the GRO as much as compared to arbiters, enabling a finer TDC time resolution of the BTDC prototype to be achieved.

Similar to arbiters, the proposed sampler has metastability issues. If its input voltage is held too close to the threshold voltage of its first gated inverter, an exponentially large amount of time will be required for the proposed sampler to resolve its decision. Although the chain of gated inverters and the D flip-flop ensure that the held voltage gets amplified to rail levels quickly, the metastability recovery time of the proposed sampler is slower as compared to arbiters. Therefore, bubble error correction (BEC) is employed for the BTDC prototype to correct the bubble errors arising from metastability.

Note that since arbiters are not employed in this BTDC prototype, the proposed edge comparator with input time hysteresis presented in Section 3.1 cannot be used here in spite of its benefits.

4.1.2.5 Overall Branching TDC Operation

The simplified timing diagram of the BTDC prototype is shown in Figure 4.10.

FIGURE 4.10: Simplified timing diagram of the BTDC prototype.

In general, the BTDC prototype will be disabled and is inactive when there are no inputs. When an input arrives in the form of a time difference (T_{diff}) between a START and a STOP signal, the BTDC prototype operates as follows.

Correlated double sampling (CDS) is employed for the BTDC prototype. Both the START and STOP phases of the branching GRO will be held and sampled with a designed sampling time of t_{SAM} when the START and STOP signals arrive, respectively. The START and STOP phases are sampled using the proposed phase sampling operation as discussed in Section 4.1.2.4.

Before either of the START or STOP phase is sampled, the branching GDLs of the branching GRO will be re-enabled with a designed initial setup time of t_{GDL} . As discussed in Section 4.1.1.2, this initial setup time allows the branching GDLs to produce the interpolating rising edges required for phase interpolation of the GRO.

The total time required for both the aforementioned processes forms the initial sampling time delay (i.e. $t_{SAM} + t_{GDL}$). This initial sampling time delay is also added to the STOP instance. This addition ensures that the phase change recorded by the branching GRO is always for the input time difference (T_{diff}) between the START and STOP signals.

Depending on the input time difference, the BTDC prototype is designed to operate in two different manners as follows:

1. For $T_{diff} > t_{GDL}$, the branching GDLs will be power gated after sampling of the START phase is completed, until the STOP signal arrives. This operation is shown by the black signals in Figure 4.10.
2. For $T_{diff} \leq t_{GDL}$, the branching GDLs will be re-enabled together with the GRO after sampling of the START phase is completed. In this case, the initial setup time of t_{GDL} is not required as the phases of the branching GDLs are already aligned with the GRO. This operation is shown by the red signals in Figure 4.10.

After sampling of the START and STOP phases are completed, the digital processor converts the two ring-type thermometer codes obtained from both samplings into two corresponding binary codes ($F_{6,START}$ and $F_{6,STOP}$) with BEC. In order to improve the linearity of the BTDC prototype, the implemented BEC detects the transition of $11 \rightarrow 000$ in both of the ring-type thermometer codes. The digital processor also combines the coarse code (C_6) from the counter and both of the fine codes into the final 12-bit output of the BTDC prototype using the following relationship.

$$T_{diff} = C_6 t_{GRO} + (F_{6,STOP} - F_{6,START}) T_{LSB} + q_e, \quad q_e \in [-T_{LSB}, T_{LSB}] \quad (4.17)$$

where q_e is the quantization error.

The various enable pulses for the operation of the BTDC prototype are produced by a pulse generator. The simplified schematic of this pulse generator is shown in Figure 4.11. It is essentially a modified phase-frequency detector, where the addition of buffers, OR, and AND gates enables the pulses profile shown in Figure 4.10 to be generated. The designed sampling time (t_{SAM}) and initial setup time (t_{GDL}) can be approximately expressed as follows.

$$t_{SAM} = t_2 + t_{RST-Q} \quad (4.18)$$

$$t_{GDL} = t_1 + \tau_{inv} \quad (4.19)$$

where t_1 and t_2 are fixed delays that are created from fixed delay lines, t_{RST-Q} is the Reset-to-Q delay of a D flip-flop, and τ_{inv} is the delay of an inverter.

FIGURE 4.11: Simplified schematic of the pulse generator. It is a modified phase-frequency detector where buffers, OR and AND gates are added.

Although not shown, dummy cells are also added into the pulse generator to ensure that the corresponding generated pulses, and the START and STOP signal

paths are symmetrical and matched. Nevertheless, inevitable mismatches between the symmetrical signal paths of the pulse generator will introduce linearity errors into the BTDC prototype.

An important design consideration for the BTDC prototype is that it is an asynchronous system. Therefore, sufficient timing margins or handshaking protocol has to be designed into the BTDC prototype to ensure that its different blocks are operating properly across PVT variations. For this BTDC prototype, the simpler formal method is employed.

For the BTDC prototype, since its branching GRO is a gated structure, the STOP phase from the previous time quantization could have been used as the START phase for the next time quantization. This operation can be achieved by holding the STOP phase in between the two time quantizations using the gating functionality. However, the held STOP phase would have been easily lost to leakage, especially if the time interval between the two time quantizations is large. This problem is further exacerbated by the larger leakage currents in advanced CMOS technology nodes.

Hence, CDS of both the START and STOP phases is used. An added benefit of using CDS is that CDS can remove sampling offsets that are common to both samplings. However, the use of CDS comes at a cost of doubling the quantization noise, or a 3 dB SNR penalty.

The reset signal does not reset the phase of the branching GRO. Therefore, the START and STOP phases are random, leading to the dynamic element matching (DEM) effect [49]. In short, DEM describes that the linearity errors arising from the inter-stages mismatches are randomized by the use of random delay stages for each time quantization. These inter-stages mismatches include the mismatch between the input offsets of the proposed samplers.

Hence, multiple outputs from the BTDC prototype could be averaged to reduce both the randomized linearity errors arising from the inter-stages mismatches, and the increased quantization noise due to CDS.

However, DEM also introduces an additional noise to the BTDC prototype, as each of its time quantizations is subjected to different mismatch errors [49].

4.1.3 Measurement Results

The BTDC prototype was fabricated in a standard 40 nm/1.1 V CMOS technology. It uses a V_{DD} of 1.1 V. Its chip micrograph is shown in Figure 4.12. It occupies an area of 0.25×0.17 mm².

FIGURE 4.12: Chip micrograph of the BTDC prototype. It occupies an area of 0.25×0.17 mm².

At nominal conditions, the oscillation frequency of the GRO is measured to be 431 MHz. Hence, from Equation (4.10), the BTDC prototype achieves a TDC time resolution of 36.2 ps and a 12-bit measurement range of 148 ns.

The measurement setup used to measure the DNL, INL, and single-shot precision (SSP) of the BTDC prototype is shown in Figure 4.13. For static DNL and INL measurements, an input time ramp is generated using two oscillation sources with a slight difference in frequencies. This method of generating an input time ramp is discussed previously in Section 3.1.3, and illustrated in Figure 3.11. The two oscillation sources are generated using a Keysight 33612A 2-channel arbitrary waveform generator (AFG). This AFG has a rated jitter specification of 1 ps. The digital outputs produced by the BTDC prototype are collected using a Keysight 16821A logic analyzer.

For characterizing the static performance of the BTDC prototype, code density test is performed where 2.53×10^6 samples are collected. The code density test is used to average out the jitter noise coming from both the BTDC prototype and the measurement setup. The measured DNL and INL of the BTDC prototype are shown in Figure 4.14. The BTDC prototype achieves a maximum/minimum DNL of 1.30 LSB/−0.93 LSB, and a maximum/minimum INL of 3.43 LSB/−3.61 LSB.

FIGURE 4.13: Measurement setup for measuring the DNL, INL, and SSP of the BTDC prototype.

In addition, the expected non-linearity periodicity of the BTDC prototype resulting from its inherent folding nature can be clearly seen in Figure 4.14(b). The INL repeats itself with a period of about 2^6 codes. As discussed in Section 4.1.2, the inherent folding nature of the BTDC prototype is due to its coarse-fine architecture.

In order to characterize the dynamic performance of the BTDC prototype, a good quality full-swing sinusoidal sequence of input time differences is required. However, it is difficult to generate this time domain signal due to the RC nature of time domain circuits. Hence, as an alternative, the single-shot experiment can be used to characterize the noise of a TDC [27].

In the single-shot experiment, a fixed input time difference is fed repeatedly to a TDC. In the presence of noise, the TDC will produce output codes that vary around a mean value. The standard deviation of these output codes is defined as the SSP. Note that the SSP increases with larger input time differences due to the accumulation of jitter.

Conventionally, the fixed input time difference for the single-shot experiment is generated using the differential delay between two cables. These two cables are fed using a common source so that the noise from the source can be neglected. However, despite the source being common, experimental results of the BTDC prototype show that noise from this setup causes larger SSPs to be measured. This outcome is corroborated by [42]. Hence, the fixed input time difference for the single-shot experiment of the BTDC prototype is generated using the phase shift between two synchronized channels of the AFG. This fixed input time difference is used instead of the differential delay between two cables.

The measured SSPs of the BTDC prototype for input time differences of up to 13.7-bit are shown in Figure 4.15 and Figure 4.16. The expected increase of the

FIGURE 4.14: Measured (A) DNL and (B) INL of the BTDC prototype. It achieves a maximum/minimum DNL and INL of 1.30 LSB/−0.93 LSB and 3.43 LSB/−3.61 LSB, respectively. The non-linearity periodicity of the BTDC prototype can be observed from the INL plot.

SSP due to the accumulation of GRO jitter can be clearly seen from Figure 4.15(a). Hence, the SSP results demonstrate that the effective measurement range of this BTDC prototype is up till 12-bit. Beyond 12-bit measurement range, the SSPs of this BTDC prototype are larger than 1 LSB. More power has to be consumed by the GRO in order to extend the measurement range of this BTDC prototype further. The larger power enables the GRO to reduce its jitter. For the mean output code of 2881 (11.5-bit), a SSP of 0.75 LSB is obtained.

As discussed in Section 4.1.2.5, the DEM effect could be leveraged to improve the linearity of the BTDC prototype. Its linearity could be improved through averaging of its outputs. The aforementioned is demonstrated by the improved

(A)

(B)

FIGURE 4.15: (A) Measured SSP against output code of the BTDC prototype with and without averaging applied. Within 12-bit range, SSPs of 0.75 LSB and 0.43 LSB, respectively, are obtained. (B) SSP histograms for mean output codes of 185 and 2881.

FIGURE 4.16: SSP histograms for mean output code of 13932.

SSP results when four adjacent outputs of the BTDC prototype are averaged. The improved SSP results are also shown in Figure 4.15 and Figure 4.16. For example, the SSP for the mean output code of 2881 is improved to 0.43 LSB.

The BTDC prototype has several noise sources. These noise sources can be categorized into the following:

- Input signal noise from the AFG (σ_{in}).
- Quantization noise of the BTDC prototype (σ_{qe}).
- Accumulated jitter noise of the GRO (σ_{GRO}).
- DEM noise (σ_{DEM}).
- Other noise sources (σ_{other}).

The input signal noise of 1 ps/channel from the AFG and the quantization noise of the BTDC prototype can be calculated as follows.

$$\sigma_{in} = \sqrt{(0.0276\Delta)^2 \times 2} = 0.04\Delta \quad (4.20)$$

$$\sigma_{qe} = \sqrt{\frac{\Delta^2}{12} \times 2} = 0.41\Delta \quad (4.21)$$

The jitter noise of the GRO accumulates every cycle of its oscillation. Hence, the accumulated jitter noise of the GRO is code dependent.

For the DEM noise, as mentioned at the end of Section 4.1.2.5, it is resultant from the different mismatch errors seen by each time quantization. Hence, it encompasses the mismatches between the branching GRO delay stages, and is also code dependent. The DEM noise will be minimum when the input time difference equals any integer oscillation periods of the GRO as the same delay stages will be selected. Conversely, the DEM noise will be maximum when the input time difference equals any half oscillation periods of the GRO [64]. The minimum DEM noise is approximately 0Δ .

The accumulated jitter noise of the GRO and the maximum DEM noise can be estimated using methods similar to [64]. Assuming that all the noise sources are white and uncorrelated, the noise sources will add in the mean-square. Hence, the two aforementioned quantities can be estimated from the SSP² curve that is plotted within the 12-bit measurement range. They can be estimated as follows:

- The variance of the accumulated jitter noise can be estimated from the gradient of the linear function fitted to the SSP² curve.
- The variance of the maximum DEM noise can be estimated from the difference between the upper and lower bounds of the SSP² curve.

Using these methods, the accumulated jitter noise of the GRO and the maximum DEM noise are estimated to be at least $0.04\Delta/\sqrt{\text{cycle}}$ and 0.58Δ , respectively. These values are illustrated in Figure 4.15(a) using the SSP curve even though they are calculated from the SSP² curve.

The other noise sources of the BTDC prototype comprise of the rest of the noise sources. These noise sources include thermal noise and supply noise. The

TABLE 4.2: Noise Breakdown of the BTDC Prototype

Noise Source	RMS Noise
Input signal noise, σ_{in}	0.04Δ
Quantization noise, σ_{qe}	0.41Δ
Accumulated GRO jitter noise, σ_{GRO}	$0.04\Delta/\sqrt{\text{cycle}}$
DEM noise, σ_{DEM}	$0\Delta \sim 0.58\Delta$
Other noise sources, σ_{other}	0.47Δ

other noise sources can also be estimated by subtracting the input signal noise and quantization noise in the mean-square from the lower bound of the SSP² curve. The other noise sources are estimated to be 0.47Δ .

The noise breakdown of the BTDC prototype is summarized in Table 4.2.

The BTDC prototype is sensitive to supply variation as its time quantization is reliant on the propagation delay of its delay stages. Hence, similar to [42], a clean regulated supply of 1.1 V is provided to the BTDC prototype using an external low dropout (LDO) regulator. In [42], on-chip LDO regulators are used for its TDC prototype.

The over temperature behavior of the BTDC prototype is characterized by subjecting it to temperature variation using a Binder MK 53 temperature chamber as shown in Figure 4.13. The single-shot experiment is used to characterize the over temperature behavior. The results are shown in Figure 4.17.

At higher temperatures, the delay of the branching GRO delay stages increases, leading to higher TDC time resolutions of the BTDC prototype and lower mean output codes for a fixed input time difference. Vice versa at lower temperatures. From Figure 4.17(a), it can be seen that the digital based delay tuning capability of the delay stages enables the TDC time resolution to be calibrated against temperature variation. The variation of the TDC time resolution over a temperature range of -40°C to 125°C is reduced by 92.3 % when the digital based delay tuning is applied.

For a TDC in general, assuming zero dead-time, its maximum sampling rate ($F_{S,MAX}$) is inversely proportional to its measurement range. This relationship can

FIGURE 4.17: Measured (A) mean output codes and (B) SSPs of the BTDC prototype for a fixed input time difference over a temperature range of -40°C to 125°C . The mean output codes variation, and hence, the TDC time resolution variation is reduced by 92.3 %.

be expressed as follows.

$$F_{S,MAX} = \frac{1}{2^n T_{LSB}}. \quad (4.22)$$

where n is the total number of bits of the TDC. Therefore, the BTDC prototype has a maximum sampling rate of 6.73 MS/s.

The power consumption of the BTDC prototype is dependent on the input time difference. At a fixed sampling rate, less power will be saved by the power gating of the BTDC prototype for larger input time differences. At a sampling rate of 5 MS/s, the BTDC prototype consumes 275 μW of average dynamic power for a full range input time difference of 148 ns.

As mentioned, it is difficult to characterize the dynamic performance of a TDC. Hence, the ENOB of a TDC is difficult to be measured. As a replacement for the ENOB, Kim et al. [56,62] have proposed the effective number of linear bits (N_{linear}) for a TDC. It is defined as follows.

$$N_{linear} = n - \log_2(INL + 1) \quad (4.23)$$

Kim et al. have shown in [62] that the effective number of linear bits of a TDC is empirically similar to its ENOB through MATLAB simulations. Hence, the figure

of merit of a TDC (FoM_{TDC}) can be defined as follows.

$$FoM_{TDC} = \frac{Power}{2^{N_{linear}} F_S} \quad (4.24)$$

The effective number of linear bits and figure of merit of the BTDC prototype are calculated to be 9.80-bit and 61.9 fJ/conv.-step, respectively, using Equation (4.23) and Equation (4.24).

The performances of the BTDC prototype and other recently reported TDCs in the literature are summarized and compared in Table 4.3. In this table, calibrations for a TDC are split into two different categories as follows:

- Resolution calibration refers to calibration that maintains the time quantization step size (i.e. the TDC time resolution) across PVT variations.
- Linearity calibration refers to calibration that maintains the uniformity between all of the time quantization steps across PVT variations.

It can be observed that the TDC time resolution achieved by the BTDC prototype is relatively large at 36.2 ps. This TDC time resolution is large in spite of the $4\times$ interpolation factor that is implemented for this BTDC prototype. This BTDC prototype does not achieve the TDC time resolution of 5 ps that is required for the overall time-mode ADC.

Moreover, it can be observed that the linearity performance of the BTDC prototype is relatively poor. It has the highest INL of 3.61 LSB. However, the BTDC prototype consumes a low power of 275 μ W due to its power saving features. Hence, the BTDC prototype still achieves a decent figure of merit of 61.9 fJ/conv.-step.

Both the poor TDC time resolution and linearity of the BTDC prototype will be investigated. Hence, improvements can be made to the BTDC prototype so that it can achieve the required specifications for the overall time-mode ADC.

TABLE 4.3: Performance Summary of Proposed BTDC Prototype and Other Recently Reported TDCs

TDC:	JSSC 18 [64]	JSSC 14 [62]	JSSC 15 [59]	JSSC 18 [42]	JSSC 18 [45]	TVLSI 16 [49]	JSSC 10 [34]	ISSCC 15 [50]	BTDC
Architecture	RNS	Pipeline	1–3 MASH	2 Step + SES	2-D Spiral Vernier	Parallel Sample	Parallel Lines	Stochas	Branch
Technology	45nm	65nm	65nm	65nm	45nm SOI	65nm	40nm	14nm Fin	40nm
Total Bit (bit)	8.94	9	11	8	8	14	14	10	12
N_{linear} (bit)	7.80	7.57	9.30	6.83	7.58	13.4	13.1	8.28	9.80
Resolution (ps)	9.40	1.12	2.64 ^b	0.45	1.25	6.00	5.50	1.17	36.2
F_S (MS/s)	215	250	150	50–200	80	1	40	100	5
DNL (LSB)	0.57	0.60	–	0.65	0.25	0.12 ^d	0.60 ^d	0.80	1.30
INL (LSB)	1.10	1.70	2.24	1.25	0.34	0.50 ^d	0.81 ^d	2.30	3.61
SSP (LSB)	0.74	0.69	0.18	1.70	0.31	1.83	0.80	–	0.75
Power (mW)	24.2	15.4	3.52	3.90 ^c	0.69	0.28	1.80	0.78 ^e	0.28
FoM_{TDC} (fJ/C.-s)	505	325	37.1	343	45.1	25.6	4.97	25.1	61.9
Area (mm ²)	0.081	0.140	0.032	0.089	0.040	0.120	0.010	0.036	0.043
Resolution Cal. ^a	No	No	No	FG	BG	No	No	No ^f	FG
Linearity Cal. ^a	No	No	No	FG	BG	BG	FG	NR	No

^aNR: Not Required / FG: Foreground / BG: Background.^bEffective resolution based on integration bandwidth of 15 MHz.^cAt F_S of 100 MS/s. TDC part of PLL, excluding VCO & divider powers of coarse TDC.^dMeasured DNL & INL based on their 6-bit [49] or 5-bit [34] fine TDC.^ePower of external 850 MHz clock is not included.^fResolution depends on external clock.

Nevertheless, the BTDC prototype has achieved the following:

- It has demonstrated the proposed branching phase interpolation technique. Its TDC time resolution is $4\times$ finer than the tap-to-tap rising edges delay of its GRO through the use of this branching technique.
- It has achieved a wide measurement range of 12-bit. This measurement range is sufficient for the overall time-mode ADC even if redundancy is considered.
- Its time quantizations are more reliable and robust against PVT variations due to its digital based delay tuning capability. It is able to calibrate its TDC time resolution against PVT variations.
- It is able to scale well with advancing CMOS technology as it has a fully digital structure.

4.1.4 Issues of the BTDC Prototype Implementation

There are several issues plaguing this BTDC prototype implementation. These issues result in the poor TDC time resolution and linearity of the BTDC prototype. These issues and their trade-offs will be investigated in this section. In addition, a problem with the coarse-fine interface of the BTDC prototype is also discussed.

4.1.4.1 TDC Time Resolution

As shown in Section 4.1.3, a poor TDC time resolution of 36.2 ps is achieved by the BTDC prototype. This poor TDC time resolution can be attributed to two factors:

1. Being a proof of concept, a low interpolation factor of 4 is designed for this BTDC prototype.
2. The use of simple delay tuning capacitors for the digital based fine delay tuning method.

Firstly, as discussed in Section 4.1.1.1, the proposed branching phase interpolation technique will be more effective if the interpolation factor is designed to be

larger. Hence, a finer TDC time resolution could be achieved by the BTDC prototype if a more aggressive interpolation factor is utilized. The larger interpolation factor can better compensate for the loadings of the branching GDLs onto the core GRO.

However, a larger interpolation factor will come at a trade-off of higher area and power consumption. A larger amount of area will be required to implement the longer branching GDLs. In addition, a longer setup time will be required for the longer branching GDLs to produce the interpolating rising edges. This relationship is expressed by Equation (4.8). Hence, more dynamic power will be consumed by the branching GRO during the longer setup time.

Secondly, albeit simple and straightforward to use capacitors as delay tuning elements in the digital based fine delay tuning method, the capacitors load the GRO heavily.

The fine delay tuning method loads 16×12 delay tuning capacitors to the GRO. In addition to these delay tuning capacitors, there are also 16×2 fixed bridging capacitors loaded onto the GRO as mentioned in Section 4.1.2.3. These heavy loadings substantially decrease the oscillation frequency of the GRO, thereby degrading the TDC time resolution of the BTDC prototype.

This degradation of TDC time resolution can be observed from Table 4.1 in Section 4.1.2.2. At nominal conditions, the simulation results show that the TDC time resolution has increased from 18.8 ps to 34.5 ps after the delay tuning elements are added. In addition, as a reference, the stage delay of the oversized NSRO used in [64] is only 9.4 ps. This NSRO is fabricated in a 45 nm CMOS technology. In comparison, the measured stage delay of the GRO used in this BTDC prototype is 72.5 ps.

For the fine delay tuning method, there is a trade-off between TDC time resolution and yield. The TDC time resolution could be improved by reducing the number of delay tuning capacitors loaded onto the GRO. However, the reduction of delay tuning capacitors will reduce the delay tuning range, thereby deteriorating the variation of the TDC time resolution at worst case corners. Vice versa, the yield of the BTDC prototype could be improved with more delay tuning capacitors at an expense of poorer TDC time resolution.

Alternatively, voltage based delay tuning such as through a Digital-to-Analog converter (DAC) could be employed to replace the delay tuning capacitors. This replacement will enable the BTDC prototype to achieve a finer TDC time resolution while retaining its delay tuning capability. However, voltage based delay tuning will require analog blocks such as a voltage reference and amplifiers. These analog blocks are undesirable for scaling into advancing CMOS technology. Hence, there is a trade-off between TDC time resolution and scalability.

Nevertheless, better digital based delay tuning or calibration methods could be employed to enable the BTDC prototype to achieve a finer TDC time resolution. For example, as demonstrated by [45], current starving transistors can also be used to achieve fine delay tuning resolutions. These current starving transistors will not load the GRO. This method can be achieved by designing an appropriate median bias current for the core inverter. Therefore, the fine delay tuning capacitors will not be required.

However, note that with a finer TDC time resolution, more power will have to be consumed by the GRO to lower its accumulated jitter down to comparable levels with the TDC time resolution. Otherwise, the measurement range of the BTDC prototype will be reduced. This relationship is expressed in Equation (4.11) and Equation (4.12).

4.1.4.2 Linearity

Similar to other TDCs, the BTDC prototype suffers from common non-idealities such as inter-stages mismatches, sampler offsets, and accumulation of jitter. However, in addition to these common non-idealities, the BTDC prototype also suffers from other non-idealities that are specific to this implementation, namely:

1. Mismatch between the rise times of the rising edges produced by the GRO and the branching GDLs
2. Mismatch between the gating instants of the GRO and the branching GDLs during phase sampling.

These additional non-idealities further degrade the linearity of the BTDC prototype.

Firstly, in this BTDC prototype, its GRO delay stage is designed to have matched rise and fall times to minimize the jitter induced by flicker noise [80]². The same is also done for its branching GDLs delay stage. However, this jitter consideration leads to a mismatch in the rise times between the rising edge produced by the GRO delay stage and the rising edge produced by the branching GDLs delay stage. This mismatch in rise times is depicted in Figure 4.18.

FIGURE 4.18: Illustration of the mismatch in rise times between the GRO delay stage and the branching GDLs delay stage. This mismatch degrades the linearity of the BTDC prototype.

From Figure 4.18, it can be seen that the time difference between the rising edges will vary along different points of the rising edges. Hence, large linearity errors will be incurred if the comparison point of the proposed sampler (i.e. $V_{th,inv}$) shifts away from its nominal value due to PVT variations.

A solution would be to design both the GRO delay stage and the branching GDLs delay stage to have the same rise time. Concurrently, the delay of the branching GDLs delay stage can be tuned using its fall time to satisfy Equation (4.5). Hence, even if the comparison point of the proposed sampler shifts, the linearity of the BTDC prototype will not be affected.

Note that this solution will cause the rising and falling edges of the branching GDLs delay stage to be asymmetrical, thereby increasing its jitter induced by flicker noise. However, unless the length of the branching GDLs is exceeding long, the slow varying flicker noise of the branching GDLs can be neglected as discussed in Section 4.1.1.1.

²The relationship between flicker noise and the rising and falling edges symmetry of a delay stage is discussed previously in Section 3.2.5.2.

Secondly, in this BTDC prototype, the GRO and the branching GDLs are controlled by separate enable signals as shown in Figure 4.19(a). These enable signals are loaded with different amounts of delay stages by the GRO and the branching GDLs. Hence, during sampling of the branching GRO phase, these enable signals are designed to disable the GRO and the branching GDLs at only approximately the same time. The mismatch between the gating instants leads to a difference in the GRO phase and the branching GDLs phase that are held and sampled. This difference in the sampled phases degrades the linearity of the BTDC prototype.

FIGURE 4.19: (A) Architecture of the enable signals for the GRO and branching GDLs in this BTDC prototype. Different loadings result in a mismatch between disabling instants during phase sampling. (B) Proposed improved version.

An improvement would be to use the enable signal for the GRO as a global enabling and disabling signal, and to use the enable signal for the branching GDLs as a local enabling signal. This proposed improvement is illustrated in Figure 4.19(b). Hence, both the GRO and the branching GDLs can be disabled together at the same time for sampling of the branching GRO phase.

However, this proposed improvement will require additional AND gates as shown in Figure 4.19(b). These additional AND gates will increase the chip area. In addition, the global mismatch between the enabling signals is simply transferred to the local mismatches between the AND gates. Fortunately, the DEM effect could be leveraged to suppress the local mismatches between the AND gates as discussed in Section 4.1.2.5.

4.1.4.3 Coarse-Fine Interface

There is a problem that plagues all coarse-fine TDC that employs the ring oscillator based TDC as the coarse TDC. This problem occurs at the interface between the coarse and fine boundary. It can be described as follows. If the STOP signal arrives too close to the ring oscillator edge that clocks the coarse counter, the coarse counter might not clock properly due to metastability issues. In the BTDC prototype, this improper clocking of its coarse counter results in an error at the LSB of its coarse TDC output or equivalently, at the 7th LSB of its 12-bit output.

A solution would be to use two separate coarse counters that are clocked half period apart by the ring oscillator [49]. This architecture ensures that either one out of the two coarse counters will not face metastability issues. Hence, depending on the measured phase of the ring oscillator, an appropriate coarse counter without metastability issues can be chosen for the final processing of results.

However, for the BTDC prototype, with known input time differences during its characterization, this error at the 7th LSB of its 12-bit output is simply detected and compensated in digital post processing.

4.2 14-bit Stochastic-Based Branching TDC

In the second part of this chapter, a 14-bit stochastic-based branching TDC implementation in a standard 65 nm CMOS technology is presented [84]. This implementation aims to improve the TDC time resolution and linearity of the branching TDC architecture by circumventing the problems faced by the BTDC prototype. Therefore, this implementation demonstrates that the branching TDC architecture can achieve the specifications required for the overall time-mode ADC. This implementation will be referred to as the SBTDC-I prototype.

In this SBTDC-I prototype, its 3-stage GRO is effectively interpolated by a factor of 85.3 using the branching technique. However, the interpolating rising edges produced by its branching GDLs are not positioned through deterministic means as is the case for the BTDC prototype. Instead, the interpolating rising edges are positioned through stochastic processes with redundancy. This method of phase interpolating is the same as the stochastic phase interpolation TDC [50]

discussed in Section 2.2.3.3. Hence, similar to the stochastic phase interpolation TDC, this SBTDC-I prototype is fully synthesized using digital tools.

Compared to the stochastic phase interpolation TDC, this SBTDC-I prototype has two advantages:

1. Its GRO serves as an oscillation source on-chip. Hence, it does not rely on an external clock for its operation.
2. Its measurement range can be easily extended by its coarse-fine architecture without incurring large additional overheads. In other words, its measurement range is not limited to the oscillation period of its GRO.

Similar to the stochastic phase interpolation TDC, good linearity performance is achieved by this SBTDC-I prototype through the stochastic processes and redundancy. Therefore, the linearity issues faced by the BTDC prototype as discussed in Section 4.1.4.2 do not affect this SBTDC-I prototype.

In addition, a simple calibration method is proposed for this SBTDC-I prototype. This simple calibration method compensates for the PVT variations of its TDC time resolution. Hence, this SBTDC-I prototype does not rely on delay tuning capacitors to tune its TDC time resolution. As a result, its TDC time resolution is not degraded by any delay tuning capacitors.

Moreover, a residue generator is proposed for this SBTDC-I prototype. This residue generator circumvents the problem regarding the coarse counter clocking operation that is discussed in Section 4.1.4.3. Hence, this SBTDC-I prototype has a smooth transition at its coarse-fine interface.

The details of this SBTDC-I prototype will be presented in the following sections.

4.2.1 Stochastic-Based Branching Technique

The stochastic-based branching TDC employs the stochastic-based branching phase interpolation technique.

In essence, the stochastic-based branching phase interpolation technique is a combination of both the branching technique and the stochastic phase interpolation technique [50]. The former and the latter techniques are presented in Section 4.1.1 and Section 2.2.3.3, respectively.

4.2.1.1 Phase Interpolation Principle

In the stochastic-based branching technique, the same branching ring oscillator presented in Section 4.1.1.1 is also utilized. The branching ring oscillator is built using a core N_{RO} -stage ring oscillator, and N_{BDL} -stage branching delay lines. There are N_{RO} branching delay lines in the branching ring oscillator. An example of an $N_{RO} = N_{BDL} = 3$ branching ring oscillator is illustrated previously in Figure 4.1(a).

As discussed in Section 4.1.1.1, using the oscillations fed from the ring oscillator, the N_{RO} branching delay lines will generate $N_{RO} \times N_{BDL}$ interpolating rising edges in between an oscillation period of the ring oscillator. Together with the N_{RO} rising edges produced by the ring oscillator, the total number of rising edges produced within an oscillation period of the ring oscillator can be expressed as follows.

$$\text{Total Edges} = N_{RO} + N_{RO} \cdot N_{BDL} = N_{RO} \cdot IF = 2^n \quad (4.25)$$

where 2^n represents the total number of delay stages in the branching ring oscillator.

Ideally, in the absence of jitter or mismatch, the phases of all the rising edges produced by the branching ring oscillator will be well defined. The phases of the rising edges produced by the ring oscillator ($\{\phi_{RO}\}$) can be expressed as follows.

$$\{\phi_{RO,v}\} = \{2v\tau_{RO}\}, \quad \text{for } v = 0 \text{ to } N_{RO} - 1 \quad (4.26)$$

where τ_{RO} is the stage delay of the ring oscillator. The phases of the rising edges produced by a branching delay line can be described by Equation (4.3) and Equation (4.4). They are repeated here for convenience.

$$\{\phi_{DLeven,i}\} = \{2i\tau_{DL}\}, \quad \text{for } i = 1 \text{ to } \frac{N_{BDL} - 1}{2} \quad (4.27)$$

$$\{\phi_{DLOdd,j}\} = \{\tau_{RO} + \tau_{DL} + 2j\tau_{DL}\}, \quad \text{for } j = 0 \text{ to } \frac{N_{BDL} - 1}{2} \quad (4.28)$$

where $\{\phi_{DLeven}\}$ and $\{\phi_{DLOdd}\}$ are the phases of the rising edges at even and odd positions, respectively, along this branching delay line, and τ_{DL} is the stage delay of the branching delay lines.

However, in the presence of jitter and mismatch, both the stage delays of the ring oscillator and the branching delay lines will vary. Therefore, the phases of all the rising edges produced will also vary.

Similar to the analysis presented in Section 2.2.3.3, the overall probability density function (PDF) modeling the summation of all the rising edges produced will converge into a uniform distribution when 2^n is large.

Therefore, an oscillation period of the ring oscillator can be interpolated by the 2^n rising edges produced by the branching ring oscillator. The oscillation period will be evenly interpolated with good linearity as the 2^n rising edges produced will be uniformly distributed. In addition, similar to the stochastic phase interpolation TDC, the linearity of this interpolation can be enhanced through the use of r-bit redundancy. This r-bit redundancy is implemented by truncating the LSB of the final output by r-bit. The timing diagram of this stochastic-based branching phase interpolation principle is illustrated in Figure 4.20. In this timing diagram, it assumes that a 3-stage ring oscillator is used.

FIGURE 4.20: Timing diagram of stochastic-based branching phase interpolation principle. An oscillation period of the ring oscillator is stochastically interpolated by 2^n rising edges. Redundancy through truncation is used to improve linearity.

In other words, the stochastic-based branching TDC can quantize an input time difference in terms of the number of rising edges that occurs within this input time

difference. Its TDC time resolution can be expressed as follows.

$$T_{LSB} = \frac{t_{RO}}{2^{n-r}} = \frac{t_{RO}}{N_{RO}IF_{eff}} \quad (4.29)$$

where t_{RO} is the oscillation period of the ring oscillator, and IF_{eff} is the effective interpolation factor. Equation (4.29) is the same as Equation (2.22), which is the expression for the TDC time resolution of the stochastic phase interpolation TDC. The effective interpolation factor can be expressed as follows.

$$IF_{eff} = \frac{IF}{2^r} \quad (4.30)$$

In fact, the stochastic-based branching technique uses the underlying principle of the branching technique as discussed in Section 4.1.1.1. It uses a stage of a branching delay line to produce an additional rising edge within the oscillation period of the ring oscillator. Therefore, 2^n rising edges can be produced by the 2^n stages of the branching ring oscillator.

In contrast to the branching technique, the stochastic-based branching technique is not used to increase the number of uniformly spaced oscillation phases of the ring oscillator. Hence, for a stochastic-based branching TDC, it is not bounded by the conditions of Equation (4.2) and Equation (4.5). In addition, its interpolation factor does not need to be an even integer. Instead, the stage delay of its branching delay lines can just be designed with the following relationship.

$$\tau_{DL} \neq \tau_{RO} \quad (4.31)$$

Equation (4.31) ensures that the rising edges produced by the branching delay lines do not overlap with the rising edges produced by the ring oscillator. Thereby, aiding in the stochastic phase interpolation process.

In the stochastic-based branching technique, the minimum setup time required (t_{su}) for the branching ring oscillator to produce its 2^n rising edges can be described by Equation (4.8). It is repeated here for convenience.

$$\begin{aligned} t_{su} &= \{\phi_{DLodd,j}\}_{j=\frac{N_{BDL}-1}{2}} \\ &= \tau_{RO} + N_{BDL}\tau_{DL} \end{aligned} \quad (4.32)$$

However, in order to allow more jitter to accumulate for the stochastic processes, an extended setup time should be given to the branching ring oscillator.

4.2.1.2 Advantages of Stochastic-Based Branching Technique

The stochastic-based branching technique is able to reap the benefits of both the branching technique, and the stochastic phase interpolation technique. The advantages of a stochastic-based branching TDC can be summarized as follows:

- It is able to efficiently utilize all the inverters in its branching ring oscillator even if only rising edges are considered. As discussed, 2^n rising edges will be produced from all 2^n delay stages of its branching ring oscillator within an oscillation period of its ring oscillator.
- It can save power through the power gating feature of the branching technique. Its branching delay lines only need to be enabled when the oscillation period of its ring oscillator needs to be interpolated.
- Its linearity is robust against PVT variations even without any calibrations for linearity. As demonstrated by [50], since the uniform distribution of the interpolating rising edges relies on the mismatch and jitter of the branching ring oscillator delay stages, additional mismatch and jitter from PVT variations will not degrade its linearity. In fact, its linearity will be worst when both mismatch and jitter are absent.
- Similar to the stochastic phase interpolation TDC, it does not require accurate matching during layout. Hence, it can be fully synthesized. This advantage is a result of its robustness against mismatch.
- It is able to scale well with advancing CMOS technology. This advantage is also a result of its robustness against mismatch. The larger mismatches in advanced CMOS technology nodes will not degrade its performance.

4.2.2 Fully Synthesizable Branching TDC Implementation

The block diagram of the 14-bit SBTDC-I prototype is shown in Figure 4.21. It also has a coarse-fine TDC architecture.

FIGURE 4.21: Block diagram of the 14-bit SBTDC-I prototype. It composes of a 6-bit ring oscillator based coarse TDC and an 8-bit stochastic-based branching fine TDC.

The coarse TDC of the SBTDC-I prototype is also a ring oscillator based TDC. It uses a main 3-stage GRO in the stochastic core to clock a 15-bit counter, quantizing an input time difference in terms of the oscillation period of this GRO (t_{GRO}). The coarse TDC only uses 6-bit out of the 15-bit counter, producing the 6-bit MSB of the 14-bit SBTDC-I prototype output.

The fine TDC employs the stochastic-based branching technique. It is a 12-bit stochastic-based branching TDC. It is built using branching GROs, rising edge detectors, and a Wallace tree Ones adder [85]. The fine TDC stochastically interpolates an oscillation period of the main GRO by an interpolation factor of 1365.3. Similar to [50], it uses a redundancy of 4-bit to improve the linearity of this interpolation. Hence, the fine TDC only uses its 8-bit MSB of its 12-bit output. Therefore, the effective interpolation factor of the fine TDC is 85.3. The fine TDC further quantizes the input time difference by quantizing the complimentary of the quantization error from the coarse TDC. It quantizes this time interval by counting the number of rising edges produced by its stochastic core within this time interval. The fine TDC produces the 8-bit LSB of the 14-bit SBTDC-I prototype output.

A proposed residue generator is used to interface between the coarse and the fine TDCs of the SBTDC-I prototype. It produces the complimentary of the quantization error from the coarse TDC to be further quantized by the fine TDC. In other words, the residue time generated (t_{res}) is the time difference between the STOP signal and the next main GRO rising edge that clocks the coarse counter. This residue time generated is illustrated in the timing diagram of the SBTDC-I prototype, shown in Section 4.2.2.5, Figure 4.27.

The TDC time resolution of the SBTDC-I prototype can be expressed as follows.

$$T_{LSB} = \frac{t_{GRO}}{2^{12-4}} = \frac{t_{GRO}}{3(85.3)} \quad (4.33)$$

Since the coarse TDC is also a ring oscillator based TDC, the measurement range of the SBTDC-I prototype can also be easily extended by using more bits out of its 15-bit counter. However, the measurement range is also limited by the accumulated jitter of the GRO. The maximum measurement range can be described by Equation (4.11) and Equation (4.12) from Section 4.1.2 as well.

In addition, the SBTDC-I prototype also has an inherent folding nature due to its coarse-fine architecture. The linearity errors from the fine TDC will repeat themselves for the 64 cycles of the coarse TDC operation.

As mentioned in Section 4.2.1.2, the stochastic-based branching TDC does not require accurate matching during layout due to its robustness against mismatch. This property is demonstrated by the SBTDC-I prototype. The SBTDC-I prototype is built using only standard digital library cells, and is fully synthesized using digital tools.

4.2.2.1 Stochastic-Based Branching Fine TDC Core

The core of the 12-bit stochastic-based branching fine TDC is its branching GROs. These branching GROs produce the 2^{12} interpolating rising edges for the fine TDC operation. The schematic of these branching GROs is shown in Figure 4.22.

In the branching GROs, both the delay stages for their GROs and their branching GDLs are built using NAND gates to implement the gating functionality. The main purpose of the gating functionality is to disable the branching GROs when

FIGURE 4.22: Schematic of the branching GROs. There are a total of 4107 unit NAND gates, producing the 2^{12} rising edges for the stochastic phase interpolation operation.

the SBTDC-I prototype is inactive. Thereby, reducing power consumption of the SBTDC-I prototype.

The main GRO is a simple conventional 3-stage GRO. For each time quantization of the SBTDC-I prototype, the main GRO is always reset to and starts from a fixed initial oscillation phase. Note that this main GRO is also used to clock the counter in the coarse TDC as discussed previously.

The branching GDLs are also simple GDLs. They are built using unit NAND gates with a smaller size as compared to the unit NAND gates of the GROs. Thereby, satisfying Equation (4.31) such that the interpolating rising edges produced by the branching GROs do not overlap.

In order for a single branching GRO to produce 2^{12} interpolating rising edges for the fine TDC operation, each length of its branching GDLs would need to be 1365 delay stages long. Hence, using Equation (4.32), the minimum setup time required for the single branching GRO to produce its 2^{12} interpolating rising edges

can be expressed as follows.

$$t_{su} = \tau_{GRO} + 1365\tau_{GDL} \quad (4.34)$$

where τ_{GRO} and τ_{GDL} are the stage delays of the unit NAND gates in the GRO and the branching GDLs, respectively. This long setup time required will cause the SBTDC-I prototype to burn a large amount of dynamic power. It also substantially decrease the maximum sampling rate of the SBTDC-I prototype.

Therefore, a main branching GRO is employed together with 36 replicas of itself. The 36 replica branching GROs are defined as the auxiliary branching GROs. In this configuration, there are effectively 111 output taps from the 37 GROs. Hence, the length of each branching GDL only needs to be 36 delay stages long. This configuration will enable the 2^{12} interpolating rising edges to be produced by the 4107 unit NAND gates of the 37 branching GROs. This configuration is illustrated in Figure 4.22. Each of the 37 branching GROs is enabled sequentially, separated by a small delay of τ_{os} such that the interpolating rising edges produced by each branching GRO do not overlap.

The minimum setup time required for the 37 branching GROs to produce the 2^{12} interpolating rising edges can be expressed as follows.

$$t_{su} = 36\tau_{os} + \tau_{GRO} + 36\tau_{GDL} \quad (4.35)$$

Assuming that $\tau_{os} \approx \tau_{GRO} \approx \tau_{GDL}$, using Equation (4.34) and Equation (4.35), it can be estimated that this configuration of 37 branching GROs has reduced the minimum setup time required by about 95 %. Thereby, reducing the power consumption and increasing the maximum sampling rate of the SBTDC-I prototype.

Note that the main GRO that clocks the coarse counter is from the main branching GRO. In addition, it is not critical to match between the main GRO and the auxiliary GROs. The TDC time resolution of the SBTDC-I prototype only depends on the oscillation period of the main GRO, whereas the auxiliary GROs only produce the interpolating rising edges for the fine TDC operation.

4.2.2.2 Simple Calibration Method for GRO

As evident from Equation (4.33), the TDC time resolution of the SBTDC-I prototype is dependent on the oscillation period of its main GRO. Hence, the TDC time resolution will vary with PVT variations.

Similar to the BTDC prototype, the SBTDC-I prototype has to calibrate its TDC time resolution for it to be reliably used for time quantizations. In other words, the oscillation period of its main GRO needs to be calibrated against PVT variations. In addition, the calibration method should be compatible with CMOS scaling so that the SBTDC-I prototype can scale with advancing CMOS technology.

An all-digital PLL (ADPLL) structure could be used to lock the oscillation period of the main GRO to an external PVT stable crystal oscillator. However, an ADPLL structure is complicated and non-trivial to implement.

Therefore, a simple digital based foreground calibration method is proposed for the SBTDC-I prototype. This simple calibration method is illustrated in Figure 4.23, and can be described as follows.

FIGURE 4.23: Simple digital based foreground calibration method for the SBTDC-I prototype. The oscillation period of the main GRO is measured by counting the number of its cycles within a reference time period.

Using the 15-bit counter, the oscillation period of the main GRO can be simply measured by counting the number of its oscillation cycles within a reference time period (T_{REF}). This reference time period is implemented using an oscillation period of an external PVT stable crystal oscillator. This measurement of the main GRO oscillation period can be expressed as follows.

$$T_{REF} = C_{15}t_{GRO} + q_e, \quad q_e \in [0, t_{GRO}]$$

$$t_{GRO} = \frac{T_{REF}}{C_{15}} - \frac{q_e}{C_{15}}, \quad q_e \in [0, t_{GRO}] \quad (4.36)$$

where C_{15} represents the number of main GRO oscillation cycles, and q_e is the quantization error. From Equation (4.36), the TDC time resolution of the SBTDC-I prototype can be extracted using Equation (4.33). By measuring the TDC time resolution, the 14-bit output of the SBTDC-I prototype can be scaled in the digital domain to compensate for the PVT variations of the TDC time resolution.

It is evident from Equation (4.36) that there is a quantization error in this simple calibration method. This quantization error will translate into an error in the 14-bit output of the SBTDC-I prototype.

However, Equation (4.36) also shows that this quantization error can be minimized. It can be minimized by designing both the length of the counter and the reference time period to be large. For the 14-bit SBTDC-I prototype, the 15-bit counter is chosen so that an accuracy of 15-bit can be achieved during this simple calibration method.

Note that in this simple calibration method, the main GRO needs to oscillate for a large number of cycles. Hence, the main GRO accumulates a large amount of jitter. This accumulated jitter of the main GRO is dominated by flicker noise, and can be expressed by Equation (4.12). It is repeated here for convenience.

$$\sigma_{GRO,1/f} = \zeta \Delta T \approx \zeta(C_{15}t_{GRO}) \quad (4.37)$$

In other words, this method of measuring the main GRO oscillation period is noisy. Therefore, in this simple calibration method, a large sample of the main GRO oscillation period needs to be measured. The main GRO oscillation period can then be estimated from the mean of the collected samples.

In addition, note that this simple calibration method only calibrates the TDC time resolution of the SBTDC-II prototype, or equivalently, its gain error. This simple calibration method does not correct the linearity errors of the SBTDC-I prototype. However, as discussed in Section 4.2.1.2, the linearity of the SBTDC-I prototype is robust against PVT variations due to the stochastic-based branching technique.

This simple calibration method is a trade-off of accuracy with simplicity.

4.2.2.3 Residue Generator

A residue generator is proposed to interface between the coarse and the fine TDCs of the SBTDC-I prototype. It generates a residue time from the coarse TDC to be further quantized by the fine TDC. The residue time is the time difference between the STOP signal and the next main GRO rising edge that clocks the coarse counter.

However, if the residue time is too small, the control signals of the SBTDC-I prototype might not have sufficient time to respond properly. This improper control of the SBTDC-I prototype can result in two problems:

1. The residue time might not be correctly generated. The wrong rising edge from the main GRO might be used for the residue generation, resulting in a residue time that is too large.
2. The coarse counter might not clock properly due to metastability issues as discussed Section 4.1.4.3.

Both of these problems will result in a large error in the output of the SBTDC-I prototype.

In order to circumvent the aforementioned problems, the proposed residue generator selectively delays the STOP signal such that the STOP signal will always occur during the first half phase of the main GRO oscillation cycle. Therefore, the time difference between the STOP signal and the next main GRO rising edge will be sufficiently large for the SBTDC-I prototype to respond properly. This selective delay architecture of the proposed residue generator is illustrated in Figure 4.24.

The selective delay function of the proposed residue generator is achieved as follows. The phase of the main GRO oscillation cycle is detected by an arbiter when the STOP signal arrives. This arbiter is implemented by a simple D flip-flop. If the STOP signal arrives during the first half phase, it does not need to be delayed. Conversely, if the STOP signal arrives during the second half phase, it will be delayed by a fixed time delay of t_{DEL} . This fixed time delay is designed to be approximately equal to half of the main GRO oscillation period, and can be expressed as follows.

$$t_{DEL} \approx \frac{t_{GRO}}{2} \quad (4.38)$$

FIGURE 4.24: Simplified schematic and timing diagram of the proposed residue generator. The STOP signal will be selectively delayed depending on the arbitration result of the D flip-flop.

The ability to selectively delay the STOP signal is achieved by creating both delayed and non-delayed propagation paths for the STOP signal simultaneously. Depending on the arbitration result of the D flip-flop, the appropriate propagation path for the STOP signal is chosen using a 2-to-1 multiplexer.

While the STOP signal is being processed, the oscillation signal of the main GRO also propagates through a replica non-delayed path of the STOP signal. Thereby, maintaining the intrinsic time difference between the STOP signal and the main GRO rising edge. In addition, this structure ensures that the correct main GRO rising edge will be used to clock the coarse counter.

The selectively delayed STOP signal and the GRO rising edge are then fed to a final pulse generator to produce the residue time. The pulse generator is implemented with an XOR gate.

Note that if the fixed time delay is applied to the STOP signal, it can be removed in the digital processor as the result of the arbitration is known. However, the removal of this fixed time delay will require the knowledge of its actual time

delay value. This fixed time delay will vary with PVT variations. Fortunately, this fixed time delay can be foreground measured using the SBTDC-I prototype itself as will be shown later in Section 4.2.2.6.

Overall, the selective delay architecture of the proposed residue generator ensures a smooth transition at the coarse-fine interface of the SBTDC-I prototype. However, there are four considerations to take into account for this proposed residue generator.

1. The STOP signal path and the main GRO oscillation signal path have to be matched to maintain their intrinsic time difference. However, as the SBTDC-I prototype is fully synthesized, these two paths will not be matched. Their mismatch will add to the fixed time offset (t_{OS}) of the SBTDC-I prototype. This fixed time offset can also be foreground measured as will be shown later in Section 4.2.2.6.
2. When the time difference between the STOP signal and the main GRO rising edge is small, the D flip-flop will be working in the metastability region. Hence, sufficient time has to be given for the D flip-flop to resolve its decision in metastability.
3. The D flip-flop has setup and hold times. Hence, the selective delay of the STOP signal does not switch over from delayed to non-delayed mode right after a main GRO rising edge. Vice versa for a main GRO falling edge. Instead, the selective delay only switches from one mode to the other after the hold time of the D flip-flop is satisfied. This effect is beneficial for the SBTDC-I prototype. It ensures that the switch over of the selective delay mode occurs only slightly after a main GRO rising edge. Thereby, ensuring that the residue time generated is never too small, and never overflows pass the oscillation period of the main GRO.
4. There is a timing margin for the fixed time delay. If the fixed time delay is too small or too large, the delayed STOP signal can still occur too close to the next main GRO rising edge. This behavior is illustrated in Figure 4.25. Hence, although the fixed time delay can be foreground measured, it might still need to be tuned to ensure that this timing margin is not violated. In the SBTDC-I prototype, voltage based delay tuning of the fixed time delay is employed as a backup plan to ensure that this timing margin is met.

FIGURE 4.25: Violation of the timing margin for the fixed time delay. The delayed STOP signal can occur too close to the next main GRO rising edge if the fixed time delay is too small or too large.

4.2.2.4 Rising Edge Detectors

For the stochastic-based branching fine TDC operation, the fine TDC has to count the number of interpolating rising edges that are produced by its branching GROs within the residue time generated. This function is performed by the rising edge detectors and the Wallace tree Ones adder of the fine TDC.

The rising edge detectors could be implemented using simple D flip-flops with enable. These D flip-flops can be enabled for the residue time generated to detect the occurrences of the interpolating rising edges within the residue time generated. However, the residue time generated, or equivalently, the enable pulse of the D flip-flops cannot be too narrow as the narrow pulse will disappear due to its finite rise and fall times.

In order to circumvent this narrow pulse issue, a time offset of a main GRO oscillation period is added to the enable pulse using a digital synchronizer circuit. This circuit structure is illustrated in Figure 4.26.

However, this additional time offset extends the required measurement range of the fine TDC to two oscillation periods of the main GRO. The range of the residue time generated can be expressed as follows.

$$t_{res} + t_{GRO} \in (t_{GRO}, 2t_{GRO}) \quad (4.39)$$

4.2.2.5 Overall Stochastic-Based Branching TDC Operation

The simplified timing diagram of the SBTDC-I prototype is shown in Figure 4.27.

FIGURE 4.27: Simplified timing diagram of the SBTDC-I prototype.

Similar to the BTDC prototype, the SBTDC-I prototype will be disabled and is inactive when there are no inputs. When a **START** and a **STOP** signal arrive with an input time difference of T_{diff} , the SBTDC-I prototype operates as follows.

When the **START** signal arrives, only the main GRO of the main branching GRO will be enabled for coarse TDC operation. The main GRO starts its oscillation from a fixed initial oscillation phase.

When the **STOP** signal arrives, it triggers two events simultaneously as follows:

1. The branching GDLs of the main branching GRO and the 36 auxiliary branching GROs will be enabled. They are enabled to set up the 2^{12} interpolating rising edges for the stochastic-based branching phase interpolation operation of the fine TDC.
2. The **STOP** signal will be selectively delayed by the proposed residue generator. The selectively delayed **STOP** signal then disables the counter of the

coarse TDC. At this point, the coarse TDC operation is completed. The proposed residue generator also generates the residue time from the coarse TDC operation.

In Figure 4.27, the case where the STOP signal is not selectively delayed is shown by the black signals, whereas the case where the STOP signal is selectively delayed is shown by the red signals.

The residue time generated will be delayed to allow sufficient time for the 2^{12} interpolating rising edges to be ready. The residue time generated is delayed by more than the minimum setup time required by the 37 branching GROs as described by Equation (4.35). The residue time generated is then fed to the rising edge detectors. The rising edge detectors track the number of interpolating rising edges that are produced by the branching GROs within the residue time interval. At this point, the fine TDC operation is completed, and all of the 37 branching GROs will be disabled.

Finally, the digital processor produces and truncates the 12-bit output of the fine TDC to just its 8-bit MSB. The digital processor also combines the coarse code (C_6) from the counter, the truncated fine code (F_8), and the arbitration result (ARB) of the proposed residue generator. It produces the final 14-bit output of the SBTDC-I prototype using the following relationship.

$$T_{diff} = C_6 t_{GRO} + (t_{GRO} - F_8 T_{LSB}) - t_{OS} - ARB t_{DEL} + q_e, \quad q_e \in [0, T_{LSB}] \quad (4.40)$$

where t_{OS} is the fixed time offset of the SBTDC-I prototype, and q_e is the quantization error. The fixed time offset comprises of the following three components:

- The fixed initial oscillation phase of the main GRO.
- The overall mismatch between the START and the STOP signal paths of the SBTDC-I prototype.
- The mismatch between the STOP and the main GRO oscillation signal paths in the proposed residue generator as discussed in Section 4.2.2.3.

Similar to the BTDC prototype, sufficient timing margins are also designed into the asynchronous system of the SBTDC-I prototype. These timing margins ensure

that the different blocks of the SBTDC-I prototype are able to operate properly across PVT variations.

For the same reasons as the BTDC prototype, the SBTDC-I prototype is also not designed to retain the phase of its main GRO in between time quantizations. In short, the held phase of its main GRO would have been easily lost to leakages.

However, in contrast to the BTDC prototype, correlated double sampling (CDS) is not employed for the SBTDC-I prototype. Hence, the quantization noise of the SBTDC-I prototype is not doubled.

4.2.2.6 Overall Calibration Scheme

As discussed in Section 4.2.2.2, the TDC time resolution of the SBTDC-I prototype has to be calibrated against PVT variations. In addition to the TDC time resolution, the following two time quantities also have to be calibrated against PVT variations.

1. The fixed time offset (t_{OS}) of the SBTDC-I prototype.
2. The fixed time delay (t_{DEL}) of the proposed residue generator.

This requirement is evident from Equation (4.40). The time quantization of the SBTDC-I prototype is dependent on these two time quantities.

These two time quantities can be calibrated against PVT variations by measuring them in the foreground.

Firstly, the fixed time offset can be foreground measured by the SBTDC-I prototype itself using an input time difference of zero. This capability of the SBTDC-I prototype is enabled by its fine TDC quantization process.

The fine TDC quantizes the complimentary of the quantization error from the coarse TDC. Therefore, using an input time difference of zero, the residue time generated for the fine TDC will comprise of the fixed time offset as follows.

$$t_{res} = 2t_{GRO} - t_{OS} \quad (4.41)$$

Therefore, the fine TDC is able to measure and quantize the fixed time offset of the SBTDC-I prototype. Using Equation (4.40), the overall output of the SBTDC-I prototype in this measurement can be expressed as follows.

$$0 = 0 \cdot t_{GRO} + (t_{GRO} - F_8 T_{LSB}) - t_{OS} - 0 \cdot t_{DEL} + q_e \quad (4.42)$$

Therefore,

$$t_{OS} = t_{GRO} - F_8 T_{LSB} + q_e. \quad (4.43)$$

Note that the fixed time offset is designed to be larger than zero. Hence, the effective STOP signal is always later than the effective START signal. In addition, as shown by Equation (4.42), the fixed time offset is designed such that the STOP signal will not be selectively delayed when the input time difference is zero. The fixed time offset can be controlled through the initial oscillation phase of the main GRO.

Secondly, the fixed time delay of the proposed residue generator can also be foreground measured by the SBTDC-I prototype. The fixed time delay can be measured by using a replica of itself as the input time difference to the SBTDC-I prototype. In this measurement, using Equation (4.40), the overall output of the SBTDC-I prototype can be expressed as follows.

$$t_{DEL} = 1 \cdot t_{GRO} + (t_{GRO} - F_8 T_{LSB}) - t_{OS} - 1 \cdot t_{DEL} + q_e \quad (4.44)$$

Therefore,

$$t_{DEL} = \frac{2t_{GRO} - F_8 T_{LSB} - t_{OS} + q_e}{2}. \quad (4.45)$$

Note that in this measurement, as shown by Equation (4.44), the STOP signal will be selectively delayed as the fixed time delay is approximately equal to half of the main GRO oscillation period (Equation (4.38)).

Overall, the SBTDC-I prototype can be foreground calibrated against PVT variations using the calibration scheme as follows:

1. Firstly, calibrate the TDC time resolution by using the simple calibration method presented in Section 4.2.2.2. The TDC time resolution can be foreground measured using Equation (4.36) with Equation (4.33).
2. Secondly, calibrate the fixed time offset by giving an input time difference of zero to the SBTDC-I prototype. The fixed time offset can be foreground measured using Equation (4.43).
3. Lastly, calibrate the fixed time delay of the proposed residue generator by giving a replica of this delay as an input time difference to the SBTDC-I prototype. The fixed time delay can be foreground measured using Equation (4.45).

A flowchart of this calibration scheme is illustrated in Figure 4.28. If the SBTDC-I prototype is implemented as part of an SoC with supply voltage and temperature sensing capabilities, this calibration scheme can be initiated by the voltage and temperature sensors. Alternatively, foreground calibration of the SBTDC-I prototype can be periodically refreshed. For simplicity, the latter method is utilized for this implementation of the SBTDC-I prototype.

4.2.3 Simulation Results

The SBTDC-I prototype is designed and simulated in a standard 65 nm/1.2 V CMOS technology. It is designed with a V_{DD} of 0.8 V. It is fully synthesized using Synopsis Design and IC Compiler tools. Its chip layout is shown in Figure 4.29. It occupies an area of $0.79 \times 0.28 \text{ mm}^2$.

At nominal conditions (i.e. TT corner, 27°C), the oscillation period of the main GRO is simulated to be 130 ps. Hence, using Equation (4.33), the SBTDC-I prototype achieves a sub-gate delay TDC time resolution of 509 fs. However, it is expected that this TDC time resolution will degrade to about 850 fs after fabrication. Therefore, the SBTDC-I prototype has an expected 14-bit measurement range of 13.93 ns.

In order to properly simulate the SBTDC-I prototype, a simulation step size that is finer than its TDC time resolution is required. In addition, the SBTDC-I prototype has a huge netlist due to its 2^{12} delay stages and rising edge detectors.

FIGURE 4.28: Flowchart of the calibration scheme for the SBTDC-I prototype.

FIGURE 4.29: Chip layout of the SBTDC-I prototype. It occupies an area of $0.79 \times 0.28 \text{ mm}^2$.

Consequently, it will take an excessively long period of time to simulate the full 14-bit measurement range of the SBTDC-I prototype.

Therefore, a scaled-down 6-bit version of the SBTDC-I prototype is used as a proof of concept (PoC). The scaled-down 6-bit SBTDC-I PoC comprises of a 2-bit coarse TDC, a 6-bit fine TDC, and the proposed residue generator. The fine TDC uses a redundancy of 2-bit. Hence, the fine TDC only uses its 4-bit MSB of its 6-bit output. Similarly, using Equation (4.33), the scaled-down SBTDC-I PoC achieves a TDC time resolution of 8.14 ps.

For static DNL and INL simulations, an input time ramp is generated using two oscillation sources with a slight difference in frequencies³. The DNL and INL of the scaled-down SBTDC-I PoC are simulated at temperatures of 27°C, −40°C, and 125°C. Note that no additional calibrations for linearity are applied to the scaled-down SBTDC-I PoC to compensate for this variation in temperature. The results of these DNL and INL simulations are plotted in Figure 4.30. The scaled-down SBTDC-I PoC achieves a maximum/minimum DNL of 0.34 LSB/−0.38 LSB, and a maximum/minimum INL of 0.63 LSB/−0.40 LSB across the temperature corners.

FIGURE 4.30: Simulated DNL and INL of the scaled-down SBTDC-I PoC across temperature corners. It achieves a maximum/minimum DNL and INL of 0.34 LSB/−0.38 LSB and 0.63 LSB/−0.40 LSB, respectively.

³Refer to Section 3.1.3 and Figure 3.11 for this method of generating an input time ramp.

Good linearity performances across the temperature corners are achieved by the scaled-down SBTDC-I PoC even though it has no additional calibrations for linearity. Therefore, the scaled-down SBTDC-I PoC demonstrates the robustness of the stochastic-based branching technique against temperature variation. As discussed in Section 4.2.1.2, the robustness of the stochastic-based branching technique stems from its stochastic nature.

In addition, the scaled-down SBTDC-I PoC does not have large linearity errors at its coarse-fine boundaries. Thereby, demonstrating that the selective delay architecture of the proposed residue generator enables the scaled-down SBTDC-I PoC to have smooth coarse-fine transitions. The regions of codes where the proposed residue generator switches between its selective delay mode are highlighted in Figure 4.30. The coarse-fine boundaries are located at slightly before the codes where the arbitration result changes from 1 to 0.

Moreover, the expected non-linearity periodicity of the scaled-down SBTDC-I PoC due to its inherent folding nature can also be observed from Figure 4.30. The DNL and INL of the scaled-down SBTDC-I PoC approximately repeat themselves every 2^4 codes.

The robustness of the scaled-down SBTDC-I PoC against process variation is verified using Monte Carlo simulations. The single-shot experiment is employed for these Monte Carlo simulations as a performance indicator. The simulated SSP results of the scaled-down SBTDC-I PoC due to process variation are shown in Figure 4.31. The scaled-down SBTDC-I PoC achieves a decent SSP of 1.11 LSB, demonstrating its robustness against process variation despite not having any additional calibrations for linearity.

For the full scale 14-bit SBTDC-I prototype, it is verified by simulating it at specific regions of interest. There are three regions of interest as follows:

1. Region of codes where the input time differences are small.
2. Regions of codes where the arbitration result of the proposed residue generator changes from 0 to 1.
3. Regions of codes where the arbitration result of the proposed residue generator changes from 1 to 0.

FIGURE 4.31: Simulated SSP results of the scaled-down SBTDC-I PoC due to process variation. It achieves SSPs of 1.00 LSB and 1.11 LSB for fixed input time differences of 268 ps and 385 ps, respectively.

In addition, since it is expected that the non-linearity of the 8-bit fine TDC will repeat itself for the 64 cycles of the 6-bit coarse TDC operation, only the first cycle of the fine TDC repetitions is simulated. In other words, for the second and third regions of interest, only the first changes of the arbitration result from 0 to 1 and 1 to 0, respectively, are simulated.

Using simulated results of the SBTDC-I prototype at the aforementioned regions of interest, the DNL and INL for the first cycle of the fine TDC repetitions are estimated and plotted in Figure 4.32. The SBTDC-I prototype is estimated to achieve a maximum/minimum DNL of 0.27 LSB/−0.11 LSB, and a maximum/minimum INL of 2.94 LSB/−1.16 LSB.

For the SBTDC-I prototype, using Equation (4.22) and a simulated TDC time resolution of 509 fs, its maximum sampling rate ($F_{S,MAX}$) is 120 MS/s.

However, the DNL and INL simulations for the SBTDC-I prototype are performed at a slightly higher sampling rate (F_S) of 125 MS/s so as to reduce simulation time. For these simulations, the SBTDC-I prototype consumes 70.8 mW of average dynamic power.

The effective number of linear bits (N_{linear}) and figure of merit (FoM_{TDC}) of the SBTDC-I prototype are calculated to be 12.0-bit and 136 fJ/conv.-step, respectively, using Equation (4.23) and Equation (4.24).

FIGURE 4.32: Simulated DNL and INL of the full scale 14-bit SBTDC-I prototype. It achieves an estimated maximum/minimum DNL and INL of 0.27 LSB/−0.11 LSB and 2.94 LSB/−1.16 LSB, respectively.

Note that the SBTDC-I prototype is expected to have a reduced maximum sampling rate of 71.8 MS/s after fabrication as its TDC time resolution is expected to degrade to 850 fs.

The performance of the SBTDC-I prototype is summarized in Table 4.4. It can be compared with the BTDC prototype and other recently reported TDCs in the literature. Table 4.4 is an extension of Table 4.3.

As compared to the BTDC prototype, the TDC time resolution of the SBTDC-I prototype is much finer. This improvement in TDC time resolution can be attributed to two main factors:

1. A much larger effective interpolation factor of 85.3 is used for the SBTDC-I prototype.
2. The oscillation frequency of the main GRO in the SBTDC-I prototype is not reduced by any delay tuning capacitors.

In fact, the expected TDC time resolution of the SBTDC-I prototype is second finest as compared to the other recently reported TDCs in the literature. Therefore, the SBTDC-I prototype demonstrates that the stochastic-based branching

technique can achieve the TDC time resolution requirement of 5 ps for the overall time-mode ADC.

Although the linearity performance of the SBTDC-I prototype is just an estimate, it shows that it has improved as compared to the BTDC prototype. As the interpolating rising edges of the SBTDC-I prototype are positioned using stochastic processes instead of deterministic means, the SBTDC-I prototype does not suffer from the linearity issues that are faced by the BTDC prototype. These linearity issues are discussed previously in Section 4.1.4.2.

However, the INL of the SBTDC-I prototype is still relatively poor as compared to the other recently reported TDCs in the literature. Excluding the BTDC prototype, the SBTDC-I prototype has the highest INL of 2.94 LSB. This INL performance will be improved by the stochastic-based branching TDC implementation of the overall time-mode ADC.

From Table 4.4, it can be observed that the power and area consumption of the SBTDC-I prototype are comparatively large. The SBTDC-I prototype has the largest power and area consumption of 70.8 mW and 0.221 mm², respectively. Consequently, the figure of merit of the SBTDC-I prototype at 136 fJ/conv.-step is worst than that of the BTDC prototype at 61.9 fJ/conv.-step.

The large power and area consumption of the SBTDC-I prototype are trade-offs of it being a fully synthesized design. An individual reset transistor is not available in the standard digital library of the CMOS technology used. Hence, the delay stages of the SBTDC-I prototype are implemented using NAND gates. These NAND gates allow the disabled state of the SBTDC-I prototype to be controllable. However, these NAND gates consume more power and area than simple gated inverters. Simple gated inverters could have been used as the delay stages of the SBTDC-I prototype if individual reset transistors are available.

TABLE 4.4: Performance Summary of Proposed BTDC and SBTDC-I Prototypes and Other Recently Reported TDCs

TDC:	JSSC 18 [64]	JSSC 14 [62]	JSSC 15 [59]	JSSC 18 [42]	JSSC 18 [45]	TVLSI 16 [49]	JSSC 10 [34]	ISSCC 15 [50]	BTDC	SBTDC I ^g
Architecture	RNS	Pipeline	1–3 MASH	2 Step + SES	2-D Spiral Vernier	Parallel Sample	Parallel Lines	Stochas	Branch	Stochas Branch
Technology	45nm	65nm	65nm	65nm	45nm SOI	65nm	40nm	14nm Fin	40nm	65nm
Total Bit (bit)	8.94	9	11	8	8	14	14	10	12	14
N_{linear} (bit)	7.80	7.57	9.30	6.83	7.58	13.4	13.1	8.28	9.80	12.0
Resolution (ps)	9.40	1.12	2.64 ^b	0.45	1.25	6.00	5.50	1.17	36.2	0.85
F_S (MS/s)	215	250	150	50–200	80	1	40	100	5	125
DNL (LSB)	0.57	0.60	–	0.65	0.25	0.12 ^d	0.60 ^d	0.80	1.30	0.27 ^h
INL (LSB)	1.10	1.70	2.24	1.25	0.34	0.50 ^d	0.81 ^d	2.30	3.61	2.94 ^h
SSP (LSB)	0.74	0.69	0.18	1.70	0.31	1.83	0.80	–	0.75	–
Power (mW)	24.2	15.4	3.52	3.90 ^c	0.69	0.28	1.80	0.78 ^e	0.28	70.8
FoM_{TDC} (fJ/C.-s)	505	325	37.1	343	45.1	25.6	4.97	25.1	61.9	136
Area (mm ²)	0.081	0.140	0.032	0.089	0.040	0.120	0.010	0.036	0.043	0.221
Resolution Cal. ^a	No	No	No	FG	BG	No	No	No ^f	FG	FG
Linearity Cal. ^a	No	No	No	FG	BG	BG	FG	NR	No	NR

^aNR: Not Required / FG: Foreground / BG: Background.^bEffective resolution based on integration bandwidth of 15 MHz.^cAt F_S of 100 MS/s. TDC part of PLL, excluding VCO & divider powers of coarse TDC.^dMeasured DNL & INL based on their 6-bit [49] or 5-bit [34] fine TDC.^ePower of external 850 MHz clock is not included.^fResolution depends on external clock.^gSimulated results.^hSimulated DNL & INL based on its 8-bit fine TDC.

Overall, the SBTDC-I prototype has achieved the following:

- It has demonstrated the proposed stochastic-based branching technique. Its TDC time resolution is effectively $85.3\times$ finer than the tap-to-tap rising edges of its main GRO.
- Its time quantizations are reliable and robust against PVT variations. Its TDC time resolution can be calibrated against PVT variations using the proposed simple calibration method. Overall, it can be foreground calibrated against PVT variations using the calibration scheme as discussed in Section 4.2.2.6.
- It is expected to achieve a sub-gate delay TDC time resolution of 850 fs. Its TDC time resolution is not degraded by any delay tuning capacitors.
- It has achieved a wide measurement range of 14-bit through its coarse-fine architecture and the proposed residue generator.
- It has smooth transitions at its coarse-fine boundaries. This achievement is enabled by the selectively delay architecture of the proposed residue generator.
- Its linearity is robust against PVT variations due to its stochastic nature.
- It is fully synthesized as it does not require accurate matching during layout. This achievement is also a result of its stochastic nature.
- It is able to scale well with advancing CMOS technology due to both its digital structure and stochastic nature.

4.3 Summary

In summary, this chapter has presented the proposed branching phase interpolation TDC architecture.

In the branching TDC architecture, interpolating rising edges are generated using a proposed branching technique. These interpolating rising edges interpolate between the tap-to-tap rising edges of its ring oscillator. Therefore, the TDC time

resolution of the branching TDC architecture can be finer than and is not limited by the tap-to-tap rising edges of its ring oscillator.

Two branching TDC implementations have been presented:

1. A 12-bit BTDC prototype fabricated in a standard 40 nm CMOS technology.
2. A 14-bit SBTDC-I prototype fully synthesized in a standard 65 nm CMOS technology.

In the BTDC prototype, its interpolating rising edges are positioned using deterministic means. An interpolation factor of 4 is implemented. Hence, these interpolating rising edges increase the oscillation phases of its 16-stage GRO from 16 to 64. Thereby, enabling it to achieve a TDC time resolution of 36.2 ps.

The BTDC prototype has a simple digital based delay tuning capability incorporated into its delay stages. Hence, it is able to tune its TDC time resolution against PVT variations. However, the simple delay tuning method degrades its TDC time resolution. As a result, its TDC time resolution is relatively large in spite of the branching technique. In general, there are trade-offs between the TDC resolution, yield, and scalability of the BTDC prototype.

In addition, the BTDC prototype has several power saving techniques. It reduces its power consumption through power gating of its branching GDLs, using the proposed gated inverters based samplers instead of arbiters, and power gating of these proposed samplers. Hence, it consumes a low average dynamic power of 275 μ W at a sampling rate of 5 MS/s.

Overall, the BTDC prototype achieves DNL, INL, SSP, and figure of merit of 1.30 LSB, 3.61 LSB, 0.75 LSB, and 61.9 fJ/conv.-step, respectively.

In the SBTDC-I prototype, its interpolating rising edges are positioned using stochastic processes with redundancy. An effective interpolation factor of 85.3 is implemented. Hence, 256 interpolating rising edges are uniformly distributed within an oscillation period of its 3-stage main GRO. Thereby, enabling it to achieve an expected sub-gate delay TDC time resolution of 850 fs.

The SBTDC-I prototype employs a simple calibration method to compensate its TDC time resolution against PVT variations. This simple calibration method trades off accuracy with simplicity.

In addition, the SBTDC-I prototype uses a proposed residue generator with selective delay architecture. This proposed residue generator ensures the SBTDC-I prototype to have a smooth transition at its coarse-fine interface.

At a sampling rate of 125 MS/s, the SBTDC-I prototype is simulated to consume 70.8 mW of average dynamic power. In addition, from simulations, the SBTDC-I prototype achieves estimated DNL, INL, and figure of merit of 0.27 LSB, 2.94 LSB, and 136 fJ/conv.-step, respectively.

In general, both branching TDC implementations have demonstrated that they are able to achieve fine TDC time resolutions with wide measurement ranges. In addition, both implementations are able to scale with advancing CMOS technology due to their fully digital structures. The ability of the SBTDC-I prototype to scale with advancing CMOS technology is also enhanced by its stochastic nature.

Therefore, the proposed branching TDC architecture is suitable for the TDC block of the overall time-mode ADC.

Chapter 5

Scalable Time-Mode ADC

IN this chapter, the design and implementation of an 8-bit highly digital time-mode ADC in a standard 40 nm/1.1 V CMOS technology are presented. The targeted specifications of the proposed time-mode ADC are discussed previously in Section 2.3.1, and summarized in Table 2.3. The proposed time-mode ADC has achieved the specifications as follows:

- It is a non-hybrid time-mode ADC. In other words, it does not have a mix of conventional and time-mode ADC architectures. Instead, it has a pure time-mode ADC architecture.
- It is designed to achieve a moderate sampling rate of 16.67 MS/s, and a bandwidth of 8.33 MHz.
- Its VTC accepts rail-to-rail voltage input, not limited by the reduced supply headroom issue.
- It achieves an ENOB of better than 6-bit by using lookup table (LUT) based calibration. The LUT corrects the non-linearities of the VTC and the TDC.
- It has a highly digital structure. It does not use any analog blocks such as amplifiers or voltage references in its implementation. Therefore, it is able to scale well with advancing CMOS technology.

The block diagram of the proposed time-mode ADC is shown in Figure 5.1. It can be divided into four main sub-blocks:

FIGURE 5.1: Block diagram of the proposed 8-bit highly digital time-mode ADC.

1. A front-end track and hold circuit.
2. A proposed VCO-based VTC with time interval amplification.
3. A 13-bit stochastic-based branching TDC.
4. A back-end LUT to correct the VTC and TDC non-linearities.

The front-end track and hold circuit tracks the rail-to-rail input voltage (V_{IN}) when the clock (Clk) is high, and holds the input voltage as a sampled voltage (V_{sam}) when the clock is low. For the proposed time-mode ADC, an input clock with 50 % duty cycle is assumed.

The proposed VCO-based VTC converts the rail-to-rail sampled voltage into a proportional time difference (T_{diff}) for the succeeding TDC block. The voltage-to-time conversion is achieved using two ring oscillator based VCOs. Hence, the proposed VTC is an inverter based VTC that is reviewed in Section 2.1.2.2. Consequently, the transfer function of its voltage-to-time conversion is non-linear. The rail-to-rail conversion range of the proposed VTC is achieved by using both NMOS and PMOS oscillation frequency modulators. The NMOS modulates the oscillation frequency of one VCO, while the PMOS modulates the other VCO. In addition, within the proposed VTC, the time difference generated by the two VCOs is amplified by 8 times. The amplified time difference reduces the TDC time resolution requirement of the succeeding TDC block. The proposed VTC generates a time difference of 393 ps to 3.29 ns that corresponds to an input voltage of 0 V to V_{DD} .

The 13-bit stochastic-based branching TDC converts the time difference into its digital representation. This stochastic-based branching TDC is a full custom

implementation of the fully synthesized SBTDC-I prototype, and will be referred to as the SBTDC-II prototype. Firstly, the full custom implementation of the SBTDC-II prototype allows full flexibility in the design of its branching GRO. In other words, the design of the SBTDC-II prototype is not limited by the standard digital library cells. Secondly, since the TDC time resolution requirement of the SBTDC-II prototype is relaxed by the time interval amplification of the proposed VCO-based VTC, the size of its stochastic-based branching fine TDC can be reduced. Both of the aforementioned reasons reduce the area and power consumption of the SBTDC-II prototype. The SBTDC-II prototype achieves a TDC time resolution of 4.13 ps. It converts the maximum time difference of 3.29 ns produced by the proposed VCO-based VTC into a 9.64-bit digital representation. Hence, only 10-bit out of the 13-bit measurement range of the SBTDC-II prototype is required.

The back-end LUT is used to calibrate and correct the non-linear transfer function of the proposed VCO-based VTC. It also compensates for the non-linearity of the SBTDC-II prototype. For these purposes, the rail-to-rail input voltage is quantized with more than 8-bit accuracy as a redundancy for the LUT operation. As evident from the 2.90 ns output range of the proposed VCO-based VTC and the 4.13 ps TDC time resolution of the SBTDC-II prototype, the input voltage is effectively quantized to a 9.46-bit digital representation. The two aforementioned non-idealities are corrected by matching the non-ideal $2^{9.46}$ codes to their ideal 2^8 codes using the LUT. The LUT is built using a known input signal during foreground calibration.

The details of the proposed time-mode ADC will be presented in the following sections.

5.1 Track and Hold

The simplified schematic and timing diagram of the front-end track and hold circuit are shown in Figure 5.2(a) and Figure 5.2(b), respectively.

Firstly, it is assumed that the isolating switch (M_{ISO}) is shorted and the loading from the VTC is neglected. Hence, the track and hold circuit is a conventional implementation. When the clock goes high, the track and hold circuit is in the tracking phase. During this phase, the sampling switch (M_{SAM}) is switched on such

FIGURE 5.2: The track and hold circuit. It directly connects to the VTC without buffer. The sampling switch is a bootstrapped switch. Bottom plate sampling principle is utilized. (A) Simplified schematic. (B) Timing diagram.

that the sampling capacitor (C_S) tracks the input voltage (V_{IN}). When the clock goes low, the track and hold circuit is in the hold phase. During this phase, the sampling switch is switched off, isolating the sampling capacitor from the input voltage. Hence, the sampling capacitor holds the input voltage at the sampling instant as a sampled voltage (V_{sam}). The sampling instant is the falling edge of the clock.

In order for the track and hold circuit to sample a rail-to-rail input voltage, its sampling switch is implemented using a conventional bootstrapped switch adopted from [86, 87]. For the bootstrapped switch, its gate-source voltage is bootstrapped to V_{DD} using a battery during the tracking phase. Thereby, enabling the source and the drain of the bootstrapped switch to have rail-to-rail voltage swings. The bootstrapping circuit is illustrated in Figure 5.3 where the battery is implemented using a simple capacitor (C_{bat}). Readers are referred to [87] for detailed design considerations and implementation of this bootstrapping circuit.

5.1.1 Distortion

As the track and hold circuit is the front-end of the proposed time-mode ADC, it has to sample the input voltage with more than 10-bit accuracy. Hence, it is

FIGURE 5.3: Schematic of the conventional bootstrapping circuit [86, 87].

imperative that minimum distortion is introduced by track and hold operation. There are three major sources of distortion in the track and hold circuit:

1. Input voltage dependent switched-on resistance of the sampling switch.
2. Input voltage dependent clock feedthrough effect from the sampling switch.
3. Input voltage dependent charge injection effect from the sampling switch.

A comprehensive analysis of these three distortion sources can be found in [88].

The bootstrapped sampling switch also minimizes the distortion from the modulation of its switched-on resistance. The switched-on resistance (R_{ON}) of the sampling switch working in the triode region can be approximated as follows.

$$R_{ON} = \frac{\partial V_{DS}}{\partial I_D} \approx \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{thn})} \quad (5.1)$$

Since the gate-source voltage (V_{GS}) of the sampling switch is bootstrapped to V_{DD} and is constant, the switched-on resistance of the sampling switch is also constant. Hence, the switched-on resistance is to a first-order independent of the input voltage.

The distortions of the input voltage dependent clock feedthrough and charge injection effects from the sampling switch are reduced by utilizing the bottom plate

sampling principle. For this purpose, the isolating switch M_{ISO} is added to the track and hold circuit. The isolating switch is used to isolate the negative terminal of the sampling capacitor from ground slightly before the sampling instant. This isolation is achieved by switching off the isolating switch slightly before the sampling instant. Therefore, at the sampling instant, the sampling capacitor will be floating. The charges from the clock feedthrough and charge injection effects will not be able to flow onto the sampling capacitor as a path to ground is not available. Hence, the distortions from these two effects are reduced. The clock feedthrough and charge injection effects from the isolating switch will just add a DC offset to the sampled voltage. These effects from the isolating switch are not dependent on the input voltage as the source and drain of the isolating switch are constant and equal to ground.

However, in order to ensure that the sampled voltage is properly referenced to ground during the hold phase, the negative terminal of the sampling capacitor is reconnected back to ground slightly after the sampling instant. The operation of the isolating switch is illustrated in the timing diagram shown in Figure 5.2(b). The clock for the isolating switch (Clk_{ISO}) is generated using simple digital logic.

Note that the VTC is designed to begin its voltage-to-time conversion only after the negative terminal of the sampling capacitor is reconnected back to ground.

5.1.2 Sizing of Sampling Capacitor

The sampling capacitor is implemented using a metal-oxide-metal (MOM) capacitor. There are three factors to consider in the sizing of the sampling capacitor:

1. The kT/C noise sampled by the sampling capacitor.
2. The droop (ΔV_{droop}) in the sampled voltage during the hold phase due to leakage currents.
3. The loading from the VTC due to the direct connection of the track and hold circuit to the VTC.

These factors determine the minimum size of the sampling capacitor.

Firstly, the thermal noises from the switched-on resistances of the sampling switch and the isolating switch that are sampled by the sampling capacitor should be smaller than the quantization noise. This condition can be expressed as follows.

$$\frac{q_e^2}{12} \geq \int_0^\infty \frac{4kTR_{eff}}{1 + (2\pi f R_{eff} C_S)^2} df = \frac{kT}{C_S}$$

$$C_S \geq \frac{12kT}{q_e^2} \quad (5.2)$$

where q_e is the quantization error, k is the Boltzmann constant, T is temperature, and f is frequency. The effective combined switched-on resistance of the sampling switch and the isolating switch is approximated as R_{eff} for simplicity. The proposed time-mode ADC is designed with a V_{DD} of 1.1 V. At nominal temperature of 27°C, using Equation (5.2) with 10-bit accuracy, the sampling capacitor has to be larger than 43.05 fF.

Secondly, during the hold phase, there will be a droop in the sampled voltage held by the sampling capacitor. This droop in the sampled voltage is caused by leakage currents (I_{leak}), and can be approximated as follows.

$$I_{leak} = C_S \frac{\Delta V_{droop}}{T_S/2} \quad (5.3)$$

where T_S is the sampling period.

Note that in addition to the droop in the sampled voltage, the input signal also couples to the sampled voltage through the lumped parasitic input capacitor ($C_{p,IN}$) between the source and drain of the sampling switch. This parasitic input capacitor is illustrated in Figure 5.2(a). It is mainly made up of fringing capacitors between the metals and vias connected to the source and drain of the sampling switch. Therefore, the layout of the sampling switch is properly drawn to minimize this parasitic input capacitor.

The total change in the sampled voltage (ΔV_{sam}) during the hold phase is the sum of the droop effect and the input coupling effect. The total change in the sampled voltage should be smaller than half of the quantization error. This relationship can be expressed as follows.

$$|\Delta V_{sam}| \leq \frac{q_e}{2} \quad (5.4)$$

Using Equation (5.4) with 10-bit accuracy, the total change in the sampled voltage should be smaller than 537.11 μV .

Thirdly, as illustrated in Figure 5.2, the track and hold circuit directly connects to the VTC without a buffering amplifier. The buffering amplifier is not used to allow the proposed time-mode ADC to better scale with advancing CMOS technology. However, the trade-off is that the input capacitor of the VTC (C_{VTC}) is not isolated from the sampling capacitor. These two capacitors are connected in parallel. Therefore, the sampling capacitor is designed to be more than 10 times larger than the input capacitor of the VTC such that the latter can be approximately neglected. The input capacitor of the VTC is simulated to be 32.25 fF. Hence, the sampling capacitor is designed to be 507.60 fF. Although this consideration results in a relatively large sampling capacitor to be required, the large sampling capacitor easily satisfies the first and second aforementioned considerations.

5.1.3 Sizing of Sampling and Isolating Switch

The sampling switch and isolating switch have to be sized such that the sampled voltage can track the input voltage to within 10-bit accuracy during the tracking phase. This condition can be approximated by the effective $R_{eff}C_{eff}$ time constant of the track and hold circuit as follows.

$$\begin{aligned} V_{sam} &\approx V_{IN} \left(1 - \exp \frac{-T_S/2}{R_{eff}C_{eff}} \right) \\ \frac{1023}{1024} V_{IN} &\leq V_{IN} \left(1 - \exp \frac{-T_S/2}{R_{eff}C_{eff}} \right) \\ R_{eff}C_{eff} &\leq \frac{T_S/2}{6.93} \end{aligned} \quad (5.5)$$

The $R_{eff}C_{eff}$ time constant is approximately related to the tracking bandwidth (f_{track}) of the track and hold circuit as follows.

$$f_{track} \approx \frac{1}{2\pi R_{eff}C_{eff}} \quad (5.6)$$

Therefore, using Equation (5.6), the condition of Equation (5.5) can be expressed as follows.

$$f_{track} \approx \frac{1}{2\pi R_{eff}C_{eff}} \geq \frac{6.93}{\pi T_S} \quad (5.7)$$

The tracking bandwidth of the track and hold circuit can be obtained from its tracking frequency response.

At a sampling rate of 16.67 MS/s, using Equation (5.7), the sampling switch and isolating switch should be sized such that the tracking bandwidth is larger than 36.76 MHz.

5.1.4 Simulated Performance

The track and hold circuit including the loading from the VTC is designed to have better than 61.96 dB SNDR (10-bit accuracy), and satisfies the conditions of Equation (5.4) and Equation (5.7).

At a sampling rate of 16.67 MS/s, the post-layout simulated SNDR, tracking gain, and total change in held sampled voltage of the track and hold circuit are plotted as functions of input frequency (f_{IN}) in Figure 5.4(a), Figure 5.4(b), and Figure 5.4(c), respectively.

It can be observed that the track and hold circuit has a SNDR of 68.07 dB from Figure 5.4(a), a tracking bandwidth of 2.28 GHz from Figure 5.4(b), and a maximum/minimum total change in held sampled voltage of 458 μ V/−530 μ V from Figure 5.4(c).

5.2 VCO-Based VTC with Time Amplification

A VCO-based VTC is proposed for the time-mode ADC. It features two novel techniques to achieve the following two capabilities:

1. It has a rail-to-rail input range.
2. It linearly amplifies the time difference generated from the voltage-to-time conversion by 8 times.

Therefore, the proposed VCO-based VTC is able to accept and convert a rail-to-rail sampled voltage into a proportionate time difference representation (T_{diff}). In addition, the increased gain of the proposed VCO-based VTC relaxes the TDC

FIGURE 5.4: Post-layout simulated performances of the track and hold circuit. (A) SNDR, (B) tracking gain, and (C) total change in held sampled voltage as functions of input frequency.

time resolution requirement of the succeeding TDC block. In other words, a lower TDC time resolution can be used to quantize the amplified time difference for the same accuracy.

The schematic of the proposed VCO-based VTC is illustrated in Figure 5.5. It can be split into two sub-blocks that perform the following two processes:

1. The VCO-based voltage-to-time conversion.
2. The $8\times$ linear time interval amplification.

FIGURE 5.5: Schematic of the proposed VCO-based VTC with $8\times$ time interval amplification. Voltage-to-time conversion and time interval amplification are achieved using GRO based VCOs and 3-bit counters, respectively.

5.2.1 VCO-Based Voltage-to-Time Conversion

As illustrated in Figure 5.5, two GRO based VCOs are utilized in the proposed VCO-based VTC. Namely, they are a 7-stage N-type VCO and a 5-stage P-type VCO. The sampled voltage simultaneously modulates the propagation delays of the inverters in these two VCOs, thereby converting the sampled voltage into a time information. The propagation delay of each inverter is modulated using a current starved transistor in parallel with a non-current starved transistor. This structure is illustrated by the schematics of the inverters for the N-type VCO and the P-type VCO shown in Figure 5.6(a) and Figure 5.6(b), respectively. The inverter of the N-type VCO uses NMOS as its current starved transistor, whereas the inverter of the P-type VCO uses PMOS as its current starved transistor. The header ($M_{p,h}$)

and footer ($M_{n,f}$) transistors implement the gating functionality, thereby allowing the two VCOs to be enabled only for a conversion.

FIGURE 5.6: Schematics of the inverters in the (A) N-type VCO and (B) P-type VCO. Their propagation delays are modulated using a current starved transistor in parallel with a non-current starved transistor.

In other words, the proposed VCO-based VTC is an inverter based VTC that is discussed in Section 2.1.2. It uses method three of the propagation delay modulating methods that are discussed in Section 2.1.2.2.

For a conventional inverter based VTC, its input range is limited by its non-linear voltage-to-time transfer function as discussed in Section 2.1.2.2, and shown in Figure 2.3(c). The proposed VCO-based VTC overcomes this limitation by utilizing both the N-type VCO and P-type VCO simultaneously. This architecture enables the proposed VCO-based VTC to achieve its rail-to-rail input range. The operational principle behind this architecture is as follows.

The voltage-to-time relationships of the N-type VCO and P-type VCO are derived and shown in Section 2.1.2. In the following derivations, the header and footer gating transistors are assumed to be shorted for simplicity. In short, for the N-type VCO, its oscillation period ($t_{osc,N}$) can be expressed as follows.

$$t_{osc,N} = 7(\tau_{dr,N} + \tau_{df,N}) \quad (5.8)$$

where $\tau_{dr,N}$ and $\tau_{df,N}$ are the propagation delays for a rising and a falling output edge transition, respectively, of its inverter. They can be expressed as follows.

$$\tau_{dr,N} = \frac{C_{tot,N}V_{DD}}{2I_{Dp,N}} \quad (5.9)$$

$$\tau_{df,N} = \frac{C_{tot,N}V_{DD}}{2I_{Dn,N}} \quad (5.10)$$

where $C_{tot,N}$ is the total capacitance including parasitic capacitance at the output of an N-type VCO inverter. $I_{Dp,N}$ and $I_{Dn,N}$ are the saturation drain currents of M_p and M_n in the N-type VCO inverter, respectively. $I_{Dp,N}$ can be expressed as follows.

$$I_{Dp,N} = \frac{1}{2}\mu_p C_{ox} \left(\frac{W}{L} \right)_{p,N} (V_{DD} - |V_{thp}|)^2 \quad (5.11)$$

For current starved $M_{n,A}$, when the sampled voltage is higher than its threshold voltage, it is working in the saturation region. Therefore, $I_{Dn,N}$ can be expressed as follows.

$$I_{Dn,N} = \frac{1}{2}\mu_n C_{ox} \left(\left(\frac{W}{L} \right)_{n,A} (V_{sam} - V_{thn})^2 + \left(\frac{W}{L} \right)_{n,B} (V_{DD} - V_{thn})^2 \right) \quad (5.12)$$

Conversely, when the sampled voltage is lower than the threshold voltage of current starved $M_{n,A}$, $M_{n,A}$ is working in the subthreshold region. Hence, in this case, $I_{Dn,N}$ can be expressed as follows.

$$I_{Dn,N} = I_{DO_n} \left(\frac{W}{L} \right)_{n,A} \exp \left(\frac{V_{sam}}{m_n kT/q} \right) + \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L} \right)_{n,B} (V_{DD} - V_{thn})^2 \quad (5.13)$$

where I_{DO_n} and m_n are the characteristic current and subthreshold slope factor of $M_{n,A}$, respectively.

Similarly, for the P-type VCO, its counterparts for Equation (5.8) to Equation (5.13) can be expressed as follows.

$$t_{osc,P} = 5(\tau_{dr,P} + \tau_{df,P}) \quad (5.14)$$

$$\tau_{dr,P} = \frac{C_{tot,P}V_{DD}}{2I_{Dp,P}} \quad (5.15)$$

$$\tau_{df,P} = \frac{C_{tot,P}V_{DD}}{2I_{Dn,P}} \quad (5.16)$$

where $t_{osc,P}$ is its oscillation period, $\tau_{dr,P}$ and $\tau_{df,P}$ are the propagation delays for a rising and a falling output edge transition, respectively, of its inverter, and $C_{tot,P}$ is the total capacitance including parasitic capacitance at the output of its inverter. $I_{Dp,P}$ and $I_{Dn,P}$ are the saturation drain currents of M_p and M_n in its inverter, respectively. $I_{Dn,P}$ can be expressed as follows.

$$I_{Dn,P} = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_{n,P} (V_{DD} - V_{thn})^2 \quad (5.17)$$

When the sampled voltage is lower than $V_{DD} - |V_{thp}|$, current starved $M_{p,A}$ is working in the saturation region. Therefore, $I_{Dp,P}$ can be expressed as follows.

$$I_{Dp,P} = \frac{1}{2}\mu_p C_{ox} \left(\left(\frac{W}{L}\right)_{p,A} (V_{DD} - V_{sam} - |V_{thp}|)^2 + \left(\frac{W}{L}\right)_{p,B} (V_{DD} - |V_{thp}|)^2 \right) \quad (5.18)$$

Conversely, when the sampled voltage is higher than $V_{DD} - |V_{thp}|$, current starved $M_{p,A}$ is working in the subthreshold region. Hence, $I_{Dp,P}$ can be expressed as follows for this case.

$$I_{Dp,P} = I_{DOp} \left(\frac{W}{L}\right)_{p,A} \exp\left(\frac{V_{DD} - V_{sam}}{m_p kT/q}\right) + \frac{1}{2}\mu_p C_{ox} \left(\frac{W}{L}\right)_{p,B} (V_{DD} - |V_{thp}|)^2 \quad (5.19)$$

where I_{DOp} and m_p are the characteristic current and subthreshold slope factor of $M_{p,A}$, respectively.

Note that the voltage-to-time relationships of Equation (5.8) to Equation (5.19) are first-order estimations. In addition, the same assumptions from Section 2.1.2 are made for the derivations of these equations.

From the voltage-to-time relationships of Equation (5.8) to Equation (5.19), the following characteristics can be observed. For the N-type VCO, its voltage-to-time conversion gain is low when the sampled voltage is smaller than the threshold

voltage of $M_{n,A}$. Its conversion gain is larger when the sampled voltage is larger than the threshold voltage of $M_{n,A}$. This behavior is a result of $M_{n,A}$ working in the subthreshold region for the former case, and in the saturation region for the latter case. Conversely, for the P-type VCO, its conversion gain is large when the sampled voltage is small. Its conversion gain is smaller when the sampled voltage is large. The crossover point between these two conversion gain regions depends on the threshold voltage of $M_{p,A}$. $M_{p,A}$ is working in the saturation region and subthreshold region for the former case and latter case, respectively.

Therefore, the opposite voltage-to-time transfer functions of the N-type VCO and P-type VCO can be used to compensate each other. The difference of their transfer functions results in a relatively linear overall voltage-to-time transfer function over a rail-to-rail input range. As a result, the proposed VCO-based VTC can achieve rail-to-rail input range.

In the proposed VCO-based VTC, the N-type VCO is used to produce the START signal, while the P-type VCO is used to produce the STOP signal. Therefore, the difference in transfer functions of the N-type VCO and P-type VCO is naturally implemented by taking the time difference between the production times of the START and the STOP signals. In addition, the proposed VCO-based VTC uses high threshold voltage transistors. As a result, the crossover points between the two conversion gain regions for both the N-type VCO and P-type VCO are located at approximately half of V_{DD} .

The above operational principle is illustrated in Figure 5.7(a), where the post-layout simulated oscillation periods of the N-type VCO and P-type VCO, and the time difference generated by the proposed VCO-based VTC are plotted as functions of the sampled voltage. Note that this time difference plot includes the $8\times$ linear time interval amplification effect. In addition, the proposed VCO-based VTC is simulated together with the track and hold circuit. It can be observed that although the voltage-to-time conversions of the individual VCOs are highly non-linear, the proposed VCO-based VTC achieves a relatively linear overall voltage-to-time conversion of the rail-to-rail sampled voltage.

The linearity of the proposed VCO-based VTC is still degraded by the harmonic distortions of its two VCOs. These distortions can be seen from the simulated output spectrum of the proposed VTC for a near Nyquist input frequency (f_{IN})

of 8.12 MHz at a sampling rate (F_S) of 16.67 MS/s as shown in Figure 5.7(b). It can be observed that the total harmonic distortion (THD) and spurious-free dynamic range (SFDR) of the proposed VTC are simulated to be 27.70 dB and 28.70 dB, respectively. The SFDR is limited by its third harmonic. The THD limits its SNDR to 27.69 dB. Its simulated SNR at 57.41 dB is not the limiting factor for the resolution of the proposed VTC. These dynamic performance results also show that the proposed VTC achieves an ENOB of 4.31-bit. It does not achieve the ENOB of 7.2-bit targeted for the proposed time-mode ADC. Hence, calibration will be implemented to compensate for the non-linearity of the proposed VCO-based VTC. This calibration will be discussed later in Section 5.4.

FIGURE 5.7: Simulated performances of the proposed VCO-based VTC. (A) t_{osc} of both VCOs and overall T_{diff} generated as functions of the sampled voltage. (B) Output spectrum for a near Nyquist f_{IN} of 8.12 MHz at F_S of 16.67 MS/s.

Since the voltage-to-time conversion of the proposed VCO-based VTC relies on the propagation delay modulation of its inverters, its linearity is also sensitive to PVT variations. Similar to the BTDC prototype, an external LDO regulator will be utilized to provide a clean regulated supply of 1.1 V to the proposed time-mode ADC. Thereby, minimizing the voltage variation. The simulated transfer functions and Nyquist input dynamic performances of the proposed VTC for process and temperature variations are illustrated in Figure 5.8(a) and Figure 5.8(b), respectively. From both aforementioned figures, it can be observed that the linearity of the proposed VTC is degraded by PVT variations. Thereby, increasing the calibration burden required to achieve the targeted ENOB when the PVT conditions of the proposed time-mode ADC shift away from the nominal conditions.

FIGURE 5.8: Simulated performances of proposed VCO-based VTC for process and temperature variations. Its linearity is degraded. (A) Voltage-to-time transfer functions. (B) SNDR, SNR, THD, and SFDR performances.

5.2.2 Time Interval Amplification

The required TDC time resolution of the succeeding TDC block depends on the voltage-to-time gain of the proposed VCO-based VTC. Therefore, it is desirable for the proposed VCO-based VTC to generate a large time difference so that the TDC time resolution requirement can be relaxed. The succeeding TDC block can reduce its area and power consumption if it does not need to achieve an aggressive TDC time resolution.

However, the linearity of an inverter based VTC is limited by its RC characteristic as discussed in Section 2.1.2.2. As a result, it is difficult for the two VCOs of the proposed VCO-based VTC to directly generate a large linear time difference. In simplified terms, a large RC time constant would be required. Instead, it is easier to generate a small linear time difference, and then linearly amplify it.

As discussed in the previous section, the voltage-to-time conversion of the proposed VCO-based VTC relies on the phase difference between the oscillations of its N-type VCO and P-type VCO. This voltage-to-time mechanism can be leveraged to achieve $8\times$ linear time interval amplification.

For two oscillations with a difference in their periods, each cycle of their oscillations will linearly increase their phase difference by the difference in their periods. This principle is discussed previously in Section 3.1.3, and is illustrated in Figure 3.11. Therefore, $8\times$ linear time interval amplification can be achieved by the proposed VCO-based VTC through the use of two identical 3-bit counters. The oscillations of the N-type VCO and P-type VCO are fed into these two counters individually as illustrated in Figure 5.5. The 3-bit counters allow both VCOs to oscillate for 8 cycles before producing the START and STOP signals. As a result, the phase difference of the two VCOs, or equivalently, the time difference generated is linearly amplified by a factor of 8.

Quantitatively, the $8\times$ linear time interval amplification capability of the proposed VCO-based VTC has two benefits:

1. The gain of the proposed VCO-based VTC is increased from 330 ps/V to 2.64 ns/V. Therefore, it converts the 1.1 V rail-to-rail sampled voltage into a 2.90 ns time difference for the succeeding TDC block.
2. The TDC time resolution of the succeeding TDC can be relaxed from 517 fs to 4.13 ps for the same 9.46-bit quantization of the 2.90 ns time difference.

There are two design considerations that need to be taken into account when implementing the linear time interval amplification of the proposed VTC.

1. The accumulated jitters of the N-type VCO and P-type VCO.
2. The conversion time of the proposed VCO-based VTC.

Firstly, the two VCOs of the proposed VCO-based VTC will accumulate jitter as they oscillate. Their individual accumulated jitter should be designed to be smaller than the quantization step size (V_{LSB}) of the proposed time-mode ADC. It is assumed that the amount of linear time interval amplification is small enough for slow varying flicker noise to be neglected. In addition, the rest of the noise sources are assumed to be white and uncorrelated. Therefore, this accumulated jitter condition can be expressed as follows.

$$V_{LSB}A_{VTC} > \sigma_{VCO,acc} = \sqrt{A_{ta}}\sigma_{VCO,c} \quad (5.20)$$

where A_{VTC} is the voltage-to-time gain of the proposed VCO-based VTC, A_{ta} is the amount of linear time interval amplification, $\sigma_{VCO,acc}$ represents the accumulated jitter of either the N-type or P-type VCO, and $\sigma_{VCO,c}$ represents the single cycle jitter of the corresponding VCO. Note that the jitters of both the N-type VCO and P-type VCO are functions of the sampled voltage.

Secondly, the conversion time (T_{VTC}) of the proposed VCO-based VTC is dependent on the oscillation period of the P-type VCO and the amount of linear time interval amplification. The conversion time depends on the P-type VCO only as it produces the STOP signal. The proposed VCO-based VTC has to complete its voltage-to-time conversion within the hold phase of the track and hold circuit. This condition can be expressed as follows.

$$\frac{T_S}{2} \geq T_{VTC,max} = A_{ta}t_{osc,P} + t_{con} \quad (5.21)$$

where t_{con} is the time required for proper control of the proposed VCO-based VTC within the time-mode ADC.

Alternatively, this condition can be interpreted as follows. The maximum sampling rate of the proposed time-mode ADC is limited by the conversion speed of the proposed VCO-based VTC. This interpretation assumes that the combined conversion speed of the succeeding TDC and LUT blocks is not the bottleneck, which is the case for the proposed time-mode ADC.

5.2.3 Proposed VCO-based VTC Operation

The simplified timing diagram of the proposed VCO-based VTC is illustrated in Figure 5.9. Its operation is as follows.

FIGURE 5.9: Simplified timing diagram of the proposed VCO-based VTC.

When Clkb is low, the proposed VCO-based VTC is disabled and inactive. This phase corresponds to the tracking phase of the track and hold circuit. In this phase, both the N-type VCO and P-type VCO are reset to known initial starting phases by $M_{n,rst}$ and $M_{p,rst}$ reset transistors. These reset transistors are illustrated in Figure 5.5.

When Clkb goes high, the proposed VCO-based VTC begins its voltage-to-time conversion. This phase corresponds to the hold phase of the track and hold circuit. Both the N-type VCO and P-type VCO are enabled simultaneously. They begin their oscillations from their known initial starting phases. After 8 cycles of their oscillations, the N-type VCO and P-type VCO produce the START and STOP signals, respectively. At this point, the voltage-to-time conversion is completed. Therefore, the STOP signal is also used to disable both the N-type VCO and P-type VCO.

The time difference between the START and the STOP signals can be expressed as follows.

$$T_{diff} = \phi_{osc,P} + (A_{ta} - 1)t_{osc,P} - (\phi_{osc,N} + (A_{ta} - 1)t_{osc,N}) \quad (5.22)$$

where

$$\phi_{osc,N} = s_N t_{osc,N}, \quad s_N \in [0, 1] \quad (5.23)$$

$$\phi_{osc,P} = s_P t_{osc,P}, \quad s_P \in [0, 1] \quad (5.24)$$

$\phi_{osc,N}$ and $\phi_{osc,P}$ represent the initial starting phases of the N-type VCO and P-type VCO, respectively. They are expressed as products of their corresponding oscillation periods and fixed constant scaling factors (s_N and s_P) between 0 to 1 as shown by Equation (5.23) and Equation (5.24). These initial starting phases are designed by the positions of the $M_{n,rst}$ and $M_{p,rst}$ reset transistors within the N-type VCO and P-type VCO.

The mismatch between the two identical 3-bit counters will introduce non-linearity into the time difference generated. However, the non-linearity of the proposed VCO-based VTC is dominated by the non-linearities of its N-type VCO and P-type VCO. The non-linearity from the mismatch between the two identical counters is comparatively insignificant.

Note that the proposed VCO-based VTC is not designed to use its noise-shaping capability. The noise-shaping capability of a VCO-based VTC is discussed previously in Section 2.1.2.3. Therefore, the proposed time-mode ADC does not require a high oversampling rate, which would have resulted in a higher power consumption.

As illustrated by Figure 5.5 and Figure 5.6, the proposed VCO-based VTC has a highly digital structure. It does not require any analog building blocks. Hence, the proposed VCO-based VTC is able to scale with advancing CMOS technology.

5.3 13-bit Stochastic-Based Branching TDC

The 13-bit SBTDC-II prototype is implemented as the TDC block of the proposed time-mode ADC. It digitizes the time difference generated from the proposed VCO-based VTC. This time difference is proportionate to the input voltage. Note that although the SBTDC-II prototype has a measurement range of 13-bit, only up to 10-bit is used for the overall time-mode ADC operation.

As mentioned in the beginning of this chapter, the SBTDC-II prototype is a full custom implementation of the fully synthesized SBTDC-I prototype. The full custom implementation of the SBTDC-II prototype reduces its area and power consumption in two ways.

Firstly, in contrast to the SBTDC-I prototype, the delay stages of the SBTDC-II prototype do not have to be implemented using NAND gates. Simple gated inverters with individual reset transistors can be used as the delay stages for the SBTDC-II prototype. Hence, the simpler delay stages reduce the area and power consumption of the SBTDC-II prototype.

Secondly, the SBTDC-II prototype is able to reap the benefits from both deterministic and stochastic positionings of the interpolating rising edges. The flexibility from its full custom implementation allows full control over the nominal positions of the interpolating rising edges. The nominal positions of the interpolating rising edges can be designed to be relatively uniformly distributed over the oscillation period of the core GRO. Inevitably, the positions of the interpolating rising edges will vary due to jitter and mismatch. As a result, the interpolating rising edges will be stochastically re-positioned. In order for the SBTDC-II prototype to achieve good linearity performance, redundancy through truncation of its LSB is also employed. However, as the nominal positions of the interpolating rising edges are already relatively uniformly distributed, the amount of redundancy required can be reduced. Hence, the size of the stochastic-based branching fine TDC of the SBTDC-II prototype can be reduced significantly. Consequently, the area and power consumption of the SBTDC-II prototype are reduced.

In general, the architecture, operational principle, and design considerations of the SBTDC-II prototype are the same as the SBTDC-I prototype that is presented in Section 4.2. Therefore, the SBTDC-II prototype will be briefly presented. Only

the changes made to the SBTDC-II prototype from the SBTDC-I prototype will be discussed in detailed. There are two main changes made to the SBTDC-II prototype:

1. Its stochastic core has a different branching GRO implementation.
2. Its residue generator has an improved architecture. The improved architecture eliminates the timing margin issue of the proposed residue generator that is discussed at the end of Section 4.2.2.3.

The block diagram of 13-bit SBTDC-II prototype is illustrated in Figure 5.10. It has a coarse-fine TDC architecture.

FIGURE 5.10: Block diagram of the 13-bit SBTDC-II prototype. It composes of a 7-bit ring oscillator based coarse TDC and a 6-bit stochastic-based branching fine TDC.

The coarse TDC of the SBTDC-II prototype is a ring oscillator based TDC. It quantizes the time difference in terms of the oscillation period of a 10-stage core GRO (t_{GRO}). It uses an in-phase oscillation (GRO) and an out-of-phase oscillation (GROb) of the core GRO to separately clock two 7-bit counters. Depending on

the phase of the core GRO at the arrival of the STOP signal, only the appropriate counter out of the two counters will be selected for the final output generation. Details of this operation will be discussed in Section 5.3.2. The coarse TDC produces the 7-bit MSB of the 13-bit SBTDC-II prototype output.

The fine TDC is a 7-bit stochastic-based branching TDC. It is built using a single branching GRO, rising edge detectors, and a Wallace tree Ones adder [85]. The nominal positions of its 2^7 stochastic interpolating rising edges are designed to be relatively uniformly distributed over the oscillation period of the 10-stage core GRO. Hence, it uses a redundancy of only 1-bit to improve linearity. Overall, the fine TDC stochastically interpolates an oscillation period of the core GRO by an effective interpolation factor (IF_{eff}) of 6.4. The fine TDC further quantizes the time difference by quantizing the complimentary of the quantization error from the coarse TDC. The 6-bit MSB of the fine TDC is used to produce the 6-bit LSB of the 13-bit SBTDC-II prototype output.

The improved residue generator interfaces between the coarse and the fine TDCs. It produces the residue time (t_{res}) from the coarse TDC operation to be further quantized by the fine TDC. The residue time is the complimentary of the quantization error from the coarse TDC.

The TDC time resolution of the SBTDC-II prototype can be expressed as follows using Equation (4.29).

$$T_{LSB} = \frac{t_{GRO}}{2^{7-1}} = \frac{t_{GRO}}{10(6.4)} \quad (5.25)$$

Identical to the SBTDC-I prototype, the SBTDC-II prototype has the following characteristics:

- Its measurement range can be easily extended by using a longer counter. Its maximum measurement range is limited by the accumulated jitter of its core GRO. This relationship can be described by Equation (4.11) and Equation (4.12).
- It has an inherent folding nature. The linearity errors of the fine TDC will repeat themselves for the 128 cycles of the coarse TDC operation.

5.3.1 Stochastic-Based Branching GRO

The branching GRO of the stochastic-based branching fine TDC produces the 2^7 stochastic interpolating rising edges for the fine TDC operation. Its schematic is illustrated in Figure 5.11. It is built using a 10-stage core GRO, eight 14-stage branching delay lines (DL) with enable, and two 13-stage branching DLs with enable.

FIGURE 5.11: Schematic of the branching GRO in the SBTDC-II prototype. The core GRO is a gated $N = 10$, $S = 3$ NSRO. The 2^7 stochastic interpolating rising edges are produced by the 2^7 simple inverters of the branching DLs.

The core GRO is a gated $N = 10$, $S = 3$ NSRO. The negative skewed delay scheme increases its oscillation frequency at a trade-off of higher power consumption as discussed in Section 3.2. Thereby, enabling the SBTDC-II prototype to achieve a finer TDC time resolution. The gating functionality of the core GRO is implemented using header PMOS and footer NMOS transistors in each of its gated inverters. The gating functionality allows the branching GRO to be disabled when the SBTDC-II prototype is inactive to save power.

Individual NMOS and PMOS reset transistors are connected to the output taps of the core GRO as illustrated by Figure 5.11. These reset transistors reset the

core GRO to a known initial oscillation phase when the core GRO is disabled. This initial oscillation phase of the core GRO also ensures that the core negative skewed GRO oscillates with the optimum oscillation mode as described by Section 3.2.2.3.

In order to minimize the oscillation period of the core GRO for a finer TDC time resolution, only a single buffering inverter is loaded onto each output tap of the core GRO. Thereby, minimizing the loadings of the core GRO. The buffered oscillations from these buffering inverters are then fed to the branching DLs, and to the two 7-bit counters for coarse TDC operation. However, the buffered oscillations are not fed to rising edge detectors. The reason is to allow these buffering inverters to better drive the high frequency oscillations of the core GRO into the branching DLs. In other words, the rising edges from the core GRO are not used as part of the 2^7 stochastic interpolating rising edges.

Note that as the 10-stage core GRO has an even total number of stages, it can naturally produce both the in-phase (GRO) and the out-of-phase (GROb) oscillations.

The branching DLs of the branching GRO are implemented using simple inverters instead of gated inverters. As the high frequency oscillations of the core GRO propagate through the branching DLs, these oscillations might disappear due to the pulse shrinking effect. The pulse shrinking effect arises from the unequal rise and fall times of the branching DL inverters [61]. Therefore, the purpose of using simple inverters is to also allow the high frequency oscillations of the core GRO to better propagate all the way to the ends of the branching DLs.

The simple inverters are designed with sufficient strength to ensure that the high frequency oscillations of the core GRO are able to propagate to the ends of the branching DLs. In addition, they are designed such that their rise and fall times are matched at the nominal conditions. Figure 5.12 plots the output from a simple inverter at the end of a branching DL across PVT variations as a representation. It can be seen that the oscillations of the core GRO are able to reach the ends of the branching DLs across PVT variations. Voltage variation is not included as a clean regulated supply of 1.1 V will be supplied to the proposed time-mode ADC using an external LDO regulator as discussed at the end of Section 5.2.1.

The branching DLs can be disabled by disabling their inputs through their first stage NAND gates as illustrated in Figure 5.11. Therefore, the power gating feature

FIGURE 5.12: Output from a simple inverter at the end of a branching DL across PVT variations. High frequency oscillation from the core GRO is able to reach the end of the branching DL.

of the branching technique as discussed in Section 4.1.1.2 can be implemented to save power. In short, the branching DLs are only enabled when the oscillation period of the core GRO needs to be stochastically interpolated.

For the fine TDC, its 2^7 stochastic interpolating rising edges are all produced by the 128 simple inverter stages of its eight 14-stage branching DLs and its two 13-stage branching DLs. Note that the rising edges produced by the first stage NAND gates of the branching DLs are also not used as part of the 2^7 interpolating rising edges. The minimum setup time required (t_{su}) for the branching GRO to produce the 2^7 interpolating rising edges can be derived by modifying Equation (4.32) appropriately. It can be expressed as follows.

$$t_{su} = \tau_{RO} + \tau_{inv} + \tau_{NAND} + 13\tau_{DL} \quad (5.26)$$

where τ_{RO} , τ_{inv} , τ_{NAND} , and τ_{DL} are the single stage delays of the core GRO gated inverter, the core GRO buffering inverter, the branching DLs first stage NAND gate, and the branching DLs simple inverter, respectively.

5.3.2 Residue Generator

The residue generator produces the residue time from the coarse TDC operation. The residue time is the time difference between the STOP signal and the next core GRO rising edge that clocks the coarse counter.

Similar to the SBTDC-I prototype, the residue generator ensures the SBTDC-II prototype to have a smooth transition at its coarse-fine interface. This ability of the residue generator is achieved through its selective delay architecture. However, as compared to the SBTDC-I prototype, the residue generator of the SBTDC-II prototype has an improved architecture. Instead of selectively delaying the STOP signal, the improved residue generator selectively delays the core GRO oscillation. The simplified schematic of the improved residue generator is illustrated in Figure 5.13.

The selective delay function of the improved residue generator is achieved by using both the in-phase (GRO) and out-of-phase (GROb) oscillations of the core GRO simultaneously. Two separate but identical propagation paths are created for the in-phase and out-of-phase oscillations. In addition, both the delayed in-phase (D_GRO) and delayed out-of-phase (D_GROb) oscillations are used to clock two separate coarse counters.

On the arrival of the STOP signal, the phase of the in-phase oscillation will be detected using an arbiter. Similar to the SBTDC-I prototype, this arbiter is also implemented using a simple D flip-flop.

If the STOP signal arrives during the first half phase, the STOP signal will be sufficiently far from the next rising edge of the in-phase oscillation. Hence, the in-phase oscillation will be selected to produce the residue time. In addition, the coarse counter that is clocked by the in-phase oscillation will be selected to be used as the coarse TDC output. Conversely, if the STOP signal arrives during the second half phase, the STOP signal will be sufficiently far from the next rising edge of the out-of-phase oscillation. In this case, the out-of-phase oscillation and the coarse counter that it clocks will be selected instead. The former and latter will be used to produce the residue time and as the coarse TDC output, respectively.

FIGURE 5.13: Simplified schematic and timing diagram of the improved residue generator. Either the GRO or GROb signal will be chosen to produce the residue time depending on the arbitration result of the D flip-flop.

The selection of either the in-phase oscillation or the out-of-phase oscillation for the residue time generation is implemented using a 2-to-1 multiplexer. This multiplexer is controlled by the arbitration result of the D flip-flop.

Note that the STOP signal also propagates through a replica path of the identical oscillation signal paths. Thereby, maintaining the intrinsic time differences between the STOP signal and both of the rising edges from the in-phase and out-of-phase oscillations.

The residue time is generated by the final pulse generator. Identical to the SBTDC-I prototype, the pulse generator of the improved residue generator is also

built using a digital synchronizer circuit and an XOR gate. This pulse generator is illustrated previously in Section 4.2.2.4, Figure 4.26.

The improvement of this residue generator architecture as compared to that of the SBTDC-I prototype is as follows. This improved residue generator essentially locks the fixed time delay (t_{DEL}) to half of the core GRO oscillation period across PVT variations. This improvement has two benefits:

1. The SBTDC-II prototype does not have to foreground calibrate the fixed time delay.
2. This improved residue generator does not face the timing margin issue of the fixed time delay that is discussed at the end of Section 4.2.2.3. This timing margin issue arises from the PVT variations of the fixed time delay. Therefore, the improved architecture of this residue generator allows it to be more robust against PVT variations.

However, the trade-off of the improved residue generator is that there are two separate fixed time offsets ($t_{OS,A}$ and $t_{OS,B}$) for the SBTDC-II prototype. These two fixed time offsets arise from the different mismatches between the propagation path of the STOP signal and the two propagation paths of the in-phase and out-of-phase oscillations.

For the proposed residue generator of the SBTDC-I prototype, four considerations are discussed at the end of Section 4.2.2.3.

The first consideration also applies to the improved residue generator of the SBTDC-II prototype. The STOP signal path and the two oscillation signal paths have to be matched to maintain their intrinsic time differences. As the SBTDC-II prototype is a full custom implementation, the two fixed time offsets incurred from the inevitable mismatches between the signal paths are minimized.

The second and third considerations also apply to the improved residue generator of the SBTDC-II prototype directly. In brief, these considerations can be described as follows:

- Sufficient time has to be given to the D flip-flop for it to resolve its decision in metastability.

- The setup and hold times of the D flip-flop are beneficial for the improved residue generator. They ensure that the switch over of selecting the in-phase or out-of-phase oscillation occurs only slightly after a transition edge of the in-phase oscillation.

5.3.3 Rising Edge Detectors

Identical to the SBTDC-I prototype, the rising edge detectors of the SBTDC-II prototype are also implemented using 1-bit counters with enable. Details for these rising edge detectors are discussed previously in Section 4.2.2.4.

5.3.4 SBTDC-II Prototype Operation

The simplified timing diagram of the SBTDC-II prototype is shown in Figure 5.14.

FIGURE 5.14: Simplified timing diagram of the SBTDC-II prototype.

In general, the operation of the SBTDC-II prototype is the same as SBTDC-I prototype. Before the proposed VCO-based VTC generates the time difference,

the SBTDC-II prototype is disabled and is inactive. When the START and STOP signals are generated, the SBTDC-II prototype operates as follows.

The START signal enables only the core GRO of the branching GRO for coarse TDC operation. The core GRO begins its oscillation from a fixed initial oscillation phase.

The STOP signal triggers two events simultaneously as follows:

1. The branching DLs of the branching GRO are enabled to set up the 2^7 stochastic interpolating rising edges for fine TDC operation.
2. The delayed STOP signal (D_STOP) disables both coarse counters, completing the coarse TDC operation. In addition, the improved residue generator generates the residue time from the coarse TDC operation. Its operation is described previously in Section 5.3.2.

The case where the in-phase oscillation is selected is shown by the black signals in Figure 5.14, whereas the case where the out-of-phase oscillation is selected is shown by the red signals.

The residue time generated is delayed by more than the minimum setup time required by the branching GRO to produce the 2^7 interpolating rising edges. The minimum setup time required is described by Equation (5.26). After which, the residue time generated is fed to the rising edge detectors. The rising edge detectors track the number of interpolating rising edges that occur within the residue time interval, completing the fine TDC operation. The branching GRO is disabled again after this point.

Finally, the digital processor produces and truncates the 7-bit output of the fine TDC to just its 6-bit MSB. It also combines the selected coarse code (C_7 or Cb_7) from the selected counter, the truncated fine code (F_6), and the arbitration result (ARB) from the improved residue generator. It produces the final 13-bit output of the SBTDC-II prototype according to the following relationship.

$$T_{diff} = ARBb(C_7 t_{GRO} - t_{OS,A}) + ARB(Cb_7 t_{GRO} - \frac{t_{GRO}}{2} - t_{OS,B}) + (t_{GRO} - F_6 T_{LSB}) + q_e, \quad q_e \in [0, T_{LSB}] \quad (5.27)$$

where $t_{OS,A}$ and $t_{OS,B}$ are the two fixed time offsets, and q_e is the quantization error.

Similar to the SBTDC-I prototype, the fixed time offsets of the SBTDC-II prototype also comprise of the following three components:

- The fixed initial oscillation phase of the core GRO.
- The overall mismatch between the START and the STOP signal paths of the SBTDC-II prototype.
- $t_{OS,A}$ includes the mismatch between the STOP and the in-phase oscillation signal paths of the improved residue generator, whereas $t_{OS,B}$ includes the mismatch between the STOP and the out-of-phase oscillation signal paths. These offsets are discussed previously in Section 5.3.2.

In addition, sufficient timing margins are also designed into the asynchronous system of the SBTDC-II prototype. Thereby, ensuring that the SBTDC-II prototype is able to operate properly across PVT variations.

The oscillation period of the 10-stage core GRO is measured to be 264.6 ps. Therefore, the SBTDC-II prototype achieves a TDC time resolution of 4.13 ps from Equation (5.25). It quantizes the 2.90 ns time difference generated by the proposed VCO-based VTC into a 9.46-bit digital representation.

5.3.5 SBTDC-II Prototype Calibration Scheme

Similar to both the BTDC and the SBTDC-I prototypes, the SBTDC-II prototype also has to be calibrated against PVT variations for it to be reliably used for time quantizations.

As evident from Equation (5.27), the following time quantities of the SBTDC-II prototype have to be calibrated against PVT variations.

1. The oscillation period of the core GRO, t_{GRO} .
2. The two fixed time offsets, $t_{OS,A}$ and $t_{OS,B}$.

The TDC time resolution (T_{LSB}) is related to the oscillation period through Equation (5.25). Hence, it does not need to be calibrated separately.

However, as a back-end LUT is employed for the proposed time-mode ADC, the SBTDC-II prototype does not need to be calibrated separately. The LUT is used to match the non-ideal $2^{9.46}$ codes produced by the SBTDC-II prototype to the final ideal 2^8 codes. The LUT will be constantly refreshed. Hence, it is able to compensate for and correct the PVT variations of the SBTDC-II prototype output.

Nevertheless, this section discusses the calibration scheme for the SBTDC-II prototype assuming that it is deployed as a stand-alone TDC.

Similar to the SBTDC-I prototype, the SBTDC-II prototype can be calibrated against PVT variations by foreground measuring the aforementioned time quantities.

In principle, the oscillation period of the core GRO, and hence, the TDC time resolution of the SBTDC-II prototype could be foreground measured using the simple calibration method that is proposed in Section 4.2.2.2. Hence, if the 13-bit SBTDC-II prototype is deployed as a stand-alone TDC, its counter would have to be extended to at least 14-bit long. Thereby, enabling an accuracy of 14-bit to be achieved for the foreground measurement of the core GRO oscillation period.

For the stand-alone measurement of the SBTDC-II prototype, the oscillation period of its core GRO will be measured using an oscilloscope for simplicity.

The two fixed time offsets can be foreground measured by the SBTDC-II prototype itself in the same way as the SBTDC-I prototype. They can be foreground measured by giving an input time difference of zero to the SBTDC-II prototype. Since there are two fixed time offsets, two foreground measurement steps are required for the SBTDC-II prototype.

In order to enable the foreground measurements of the two fixed time offsets, the SBTDC-II prototype is designed with the following two prerequisites:

1. The fixed initial oscillation phase of the core GRO is designed to be small.
2. The ability to externally set the arbitration result of the improved residue generator is added into the SBTDC-II prototype. In other words, the improved

residue generator can be externally set to select the in-phase oscillation or the out-of-phase oscillation for the residue time generation.

Firstly, $t_{OS,A}$ can be foreground measured by directly giving an input time difference of zero to the SBTDC-II prototype. In this measurement, using Equation (5.27), the output of the SBTDC-II prototype can be expressed as follows.

$$0 = 1(0t_{GRO} - t_{OS,A}) + 0(0t_{GRO} - \frac{t_{GRO}}{2} - t_{OS,B}) + (t_{GRO} - F_6T_{LSB}) + q_e \quad (5.28)$$

Therefore,

$$t_{OS,A} = t_{GRO} - F_6T_{LSB} + q_e. \quad (5.29)$$

Note that in this measurement, the improved residue generator will select the in-phase oscillation for the residue time generation as the fixed initial oscillation phase of the core GRO is small. This behavior is reflected in Equation (5.28).

Next, $t_{OS,B}$ can be foreground measured by externally setting the improved residue generator to select the out-of-phase oscillation for the residue time generation. Using an input time difference of zero, the output of the SBTDC-II prototype in this measurement can be expressed as follows.

$$0 = 0(0t_{GRO} - t_{OS,A}) + 1(0t_{GRO} - 0\frac{t_{GRO}}{2} - t_{OS,B}) + (t_{GRO} - F_6T_{LSB}) + q_e \quad (5.30)$$

Therefore,

$$t_{OS,B} = t_{GRO} - F_6T_{LSB} + q_e. \quad (5.31)$$

The small fixed initial oscillation phase of the core GRO ensures that the STOP signal will be sufficiently far from the first rising edge of the out-of-phase oscillation. Thereby, ensuring that the residue time generation process does not have metastability issues. In addition, the selective delay concept of the improved residue generator is not applicable in this measurement. The improved residue generator is simply forced to select the out-of-phase oscillation. Therefore, $t_{GRO}/2$ should not be subtracted from this measurement as shown by Equation (5.30).

Overall, the SBTDC-II prototype can be foreground calibrated against PVT variations using the calibration scheme as follows:

1. Firstly, calibrate the TDC time resolution by using the simple calibration method that is proposed in Section 4.2.2.2.

2. Secondly, calibrate $t_{OS,A}$ by directly giving an input time difference of zero to the SBTDC-II prototype. $t_{OS,A}$ can be foreground measured using Equation (5.29).
3. Lastly, calibrate $t_{OS,B}$ by externally setting ARB to high and giving an input time difference of zero to the SBTDC-II prototype. $t_{OS,B}$ can be foreground measured using Equation (5.31).

A flowchart of this calibration scheme is illustrated in Figure 5.15. Similar to the calibration scheme of the SBTDC-I prototype as discussed in Section 4.2.2.6, the calibration scheme of the SBTDC-II prototype can be initiated by supply voltage and temperature sensors if they are available as part of an SoC. However, for simplicity in this implementation, when the SBTDC-II prototype is deployed as a stand-alone TDC, its foreground calibration will be periodically refreshed.

FIGURE 5.15: Flowchart of the calibration scheme for the SBTDC-II prototype.

5.4 Back-End LUT Based Calibration

Although the proposed VCO-based VTC achieves a relatively linear voltage-to-time conversion of the rail-to-rail sampled voltage, its linearity does not reach the targeted 7.2-bit ENOB for the proposed time-mode ADC. In addition, the non-linearity of the SBTDC-II prototype also degrades the overall linearity of the proposed time-mode ADC. Hence, a back-end LUT is employed to correct both the non-linearities of the proposed VCO-based VTC and the SBTDC-II prototype. Thereby, enabling the proposed time-mode ADC to achieve the targeted 7.2-bit ENOB.

The back-end LUT is a simple and straightforward method of linearizing the proposed time-mode ADC. Its operation principle is as follows.

The LUT is built during foreground calibration using a known input voltage signal. For simplicity, this known input voltage signal is assumed to be a simple slow voltage ramp.

The voltage ramp is fed to the proposed time-mode ADC to be quantized. The voltage ramp is designed to be slow such that all $2^{9.46}$ output codes will be produced by the proposed time-mode ADC. For example, using a sampling rate (F_S) of 16.67 MS/s for the proposed time-mode ADC, the maximum ramping speed ($\frac{dV_{ramp}}{dt}_{max}$) of the voltage ramp can be expressed as follows:

$$\begin{aligned} \frac{dV_{ramp}}{dt}_{max} &= \frac{V_{DD}/2^{9.46}}{T_S} \\ &= 26.95 \text{ } \mu\text{V/ns} \end{aligned} \quad (5.32)$$

where $T_S = 1/F_S$ is the sampling period. However, this maximum ramping speed assumes that the proposed time-mode ADC is ideal. Hence, a slower than maximum ramping speed should be used for the voltage ramp to ensure all $2^{9.46}$ output codes are produced.

Since the voltage ramp is a known signal, each of its quantizations can be matched to an ideal 2^8 output code. Therefore, the LUT can be built where each of the measured $2^{9.46}$ raw output codes can be matched to an ideal 2^8 output code. The LUT can then be used to correct the quantizations of the proposed time-mode ADC for unknown input signals.

Note that the proposed time-mode ADC quantizes an input voltage to 9.46-bit accuracy. This 9.46-bit accuracy is 1.46-bit more accurate than the final 8-bit output. The additional 1.46-bit accuracy is designed as a redundancy to improve the correction performance of the LUT operation.

Since the LUT is built during foreground calibration, it will need to be constantly refreshed for PVT variations. Therefore, the LUT also compensates for the PVT variations of the proposed VCO-based VTC and the SBTDC-II prototype.

The LUT matching is illustrated in Figure 5.16, where the measured $2^{9.46}$ raw output codes are matched to the ideal 2^8 output codes.

FIGURE 5.16: Illustration of the $2^{9.46}$ raw output codes and their LUT matched ideal 2^8 output codes.

Albeit simple and straightforward, the back-end LUT is basic and inefficient. Hence, for future prototypes, research could be done to improve the calibration method such that the calibration is more efficient and accurate. This issue is further discussed in Section 6.3.1.

In this implementation of the proposed time-mode ADC, the back-end LUT is implemented off-chip using MATLAB for simplicity.

5.5 Overall Time-Mode ADC Operation

The operation of the proposed time-mode ADC is described in detailed by the separate timing diagrams of the track and hold circuit, the proposed VCO-based

VTC, and the SBTDC-II prototype. Their timing diagrams are illustrated in Figure 5.2(b), Figure 5.9, and Figure 5.14, respectively.

The combined simplified timing diagram of the proposed time-mode ADC is shown in Figure 5.17. It illustrates the operation sequence between the four main sub-blocks of the proposed time-mode ADC during a conversion cycle.

FIGURE 5.17: Simplified timing diagram of the proposed time-mode ADC. It illustrates the combined operation of the track and hold circuit, the proposed VCO-based VTC, the SBTDC-II prototype, and the back-end LUT.

In general, the operation of the proposed time-mode ADC is controlled by the input clock (Clk). Both the track and hold circuit and the proposed VCO-based VTC operate synchronously to this input clock. Conversely, the SBTDC-II prototype and the back-end LUT operate asynchronously to this input clock. The operation of the proposed time-mode ADC is summarized as follows.

When the input clock is high, the track and hold circuit tracks the input voltage. During this tracking phase, the other three sub-blocks are disabled and inactive.

When the input clock transits from high to low, the track and hold circuit begins to hold the input voltage. At the same time, the proposed VCO-based VTC is triggered by this falling edge of the input clock to begin its conversion. It converts the held sampled voltage into a proportional time difference, producing

the asynchronous START and STOP signals. The proposed VCO-based VTC completes its conversion before the end of the hold phase (i.e. before the rising edge of the input clock).

The asynchronous START and STOP signals are fed to the SBTDC-II prototype. The START signal asynchronously triggers the SBTDC-II prototype to begin its time quantization of the time difference. The SBTDC-II prototype produces the 9.46-bit digital representation of the time difference after it has completed its time quantization operation. In addition, it produces an asynchronous flag to signal this completion of its operation.

The asynchronous flag from the SBTDC-II prototype triggers the back-end LUT to begin its matching operation. It matches the non-ideal 9.46-bit code to the ideal 8-bit code, thereby producing the final 8-bit output code of the proposed time-mode ADC.

Note that as illustrated by Figure 5.17, the SBTDC-II prototype and the back-end LUT complete their operations much earlier than the beginning of the next hold phase. Therefore, they are not the bottlenecks that limit the maximum sampling rate of the proposed time-mode ADC. Instead, as discussed at the end of Section 5.2.2, the maximum sampling rate of the proposed time-mode ADC is limited by the conversion speed of the proposed VCO-based VTC.

5.6 Measurement Results

The proposed time-mode ADC was fabricated in a standard 40 nm/1.1 V CMOS technology. It uses a V_{DD} of 1.1 V. Its chip micrograph is shown in Figure 5.18. It occupies an area of $0.365 \times 0.06 \text{ mm}^2$. The track and hold circuit, the proposed VCO-based VTC, and the SBTDC-II prototype individually occupies an area of 0.0033 mm^2 , 0.003 mm^2 , and 0.0156 mm^2 , respectively.

Both the SBTDC-II prototype as a stand-alone TDC and the overall proposed time-mode ADC are measured. Their measurement setups are illustrated in Figure 5.19.

The measurement of the SBTDC-II prototype is performed using the same methods that are employed for the BTDC prototype as discussed in Section 4.1.3.

FIGURE 5.18: Chip layout of the proposed time-mode ADC. It occupies an area of $0.365 \times 0.06 \text{ mm}^2$. The track and hold, proposed VCO-based VTC, and SBTDC-II prototype take up 15%, 14%, and 71% of the total area, respectively.

FIGURE 5.19: Measurement setups for measuring the SBTDC-II prototype as a stand-alone TDC and the overall proposed time-mode ADC.

For the static DNL and INL measurements of the SBTDC-II prototype, an input time ramp is used. This time ramp is again generated using two oscillation sources with a slight difference in their frequencies¹. These two oscillation sources are generated using a Keysight 33612A 2-channel arbitrary waveform generator (AFG) with a rated jitter specification of 1 ps. For the single-shot experiment, the fixed input time difference is generated using the phase shift between two synchronized channels of the AFG. The digital outputs of the SBTDC-II prototype are collected using a Keysight 16852A logic analyzer.

For the measurement of the overall proposed time-mode ADC, the input voltages for both static and dynamic measurements are generated using the Keysight 33612A AFG. The input clock is generated using a SRS CG635 clock generator. This clock generator has a rated jitter specification of less than 1 ps. The digital outputs of the proposed time-mode ADC are also collected using the Keysight 16852A logic analyzer.

The measurement results of the SBTDC-II prototype as a stand-alone TDC are first presented.

5.6.1 SBTDC-II Prototype Results

As mentioned at the end of Section 5.3.4, the SBTDC-II prototype achieves a measured TDC time resolution of 4.13 ps at nominal conditions. Therefore, it has a 13-bit measurement range of 33.87 ns.

Code density test is utilized for characterizing the static performance of the SBTDC-II prototype. 56.9×10^6 samples are collected. The code density test is used to average out the jitter noises from both the SBTDC-II prototype and the measurement setup. The measured DNL and INL of the SBTDC-II prototype are plotted in Figure 5.20. The SBTDC-II prototype achieves a maximum/minimum DNL of 1.98 LSB/−0.82 LSB, and a maximum/minimum INL of 1.63 LSB/−1.58 LSB.

In addition, it can be observed from Figure 5.20 that the SBTDC-II prototype does not have large linearity errors in the orders of the coarse TDC resolution (64 LSB) at its coarse-fine interfaces. Hence, the SBTDC-II prototype has smooth transitions at its coarse-fine interfaces and at codes where the arbitration

¹Refer to Section 3.1.3 and Figure 3.11 for this method of generating an input time ramp.

FIGURE 5.20: Measured DNL and INL of the SBTDC-II prototype. It achieves a maximum/minimum DNL and INL of 1.98 LSB/ -0.82 LSB and 1.63 LSB/ -1.58 LSB, respectively. Its expected non-linearity periodicity can be seen from the INL plot.

result of the improved residue generator changes from 1 to 0 or 0 to 1. Therefore, the effectiveness of the improved residue generator is demonstrated.

Furthermore, the expected non-linearity periodicity of the SBTDC-II prototype due to its inherent folding nature can be seen from Figure 5.20. The INL approximately repeats itself with a period of about 2^6 codes.

As discussed in Section 4.1.3, the noise of a TDC can be characterized by its SSP. The measured SSPs of the SBTDC-II prototype for input time differences of up to its full measurement range are shown in Figure 5.21. Note that the 1 ps/channel jitter noise contributed by the AFG has been excluded. It can be seen from Figure 5.21(a) that the SSP increases as expected when the input time difference is larger. This trend is due to the accumulation of the core GRO jitter noise. The SBTDC-II prototype achieves a reasonable maximum SSP of 1.05 LSB within its full measurement range.

FIGURE 5.21: Measured SSP results of the SBTDC-II prototype. It achieves a maximum SSP of 1.05 LSB. (A) SSP against output code. (B) SSP histograms for mean output codes of 181 and 8060.

The noise sources of the SBTDC-II prototype can be categorized into the following components:

- Quantization noise of the SBTDC-II prototype (σ_{qe}).
- Accumulated jitter noise of the core GRO ($\sigma_{GRO,acc}$).
- Other TDC noise sources ($\sigma_{TDC,other}$).

The quantization noise of the SBTDC-II prototype can be calculated as follows.

$$\sigma_{qe} = \sqrt{\frac{\Delta^2}{12}} = 0.29\Delta \quad (5.33)$$

Similarly to the BTDC prototype as discussed in Section 4.1.3, the accumulated jitter noise of the core GRO can be estimated using the method similar to [64]. The following two assumptions are made:

1. The measurement range of the SBTDC-II prototype is sufficiently short such that the slow varying flicker noise can be neglected.
2. The rest of the noise sources are white and uncorrelated. Hence, the noise sources will add in the mean-square.

Therefore, the variance of the accumulated jitter noise can be estimated from the gradient of the linear function fitted to the SSP² curve. The accumulated jitter noise is estimated to be $0.088\Delta/\sqrt{\text{cycle}}$, and is illustrated in Figure 5.21(a) using the SSP curve even though it is calculated from the SSP² curve. It can be calculated that the estimated accumulated jitter noise at maximum range of the SBTDC-II prototype (i.e. 128 cycles of core GRO oscillations) is smaller than the TDC time resolution. Similar to Equation (4.11), this relationship can be expressed as follows.

$$\begin{aligned}\sigma_{GRO,acc} &= \sqrt{128}(\sigma_{GRO,c}) < T_{LSB} \\ \sqrt{128}(0.088\Delta) &= 0.997\Delta < T_{LSB}\end{aligned}\tag{5.34}$$

where $\sigma_{GRO,acc}$ and $\sigma_{GRO,c}$ are the accumulated jitter and single cycle jitter of the core GRO, respectively. In other words, the accumulated jitter noise is sufficiently low to enable the SBTDC-II prototype to achieve its full 13-bit measurement range.

The other noise sources of the SBTDC-II prototype comprise of the rest of the noise sources, including thermal and supply noises. The other noise sources are estimated to be 0.28Δ by subtracting the quantization noise and accumulated core GRO jitter noise in the mean-square from the measured total noise of the SBTDC-II prototype.

The noise breakdown of the SBTDC-II prototype is summarized in Table 5.1.

Although the SBTDC-II prototype operates up to a sampling rate of 16.67 MS/s as part of the proposed time-mode ADC, it has a maximum sampling rate ($F_{S,MAX}$) of 29.53 MS/s. The maximum sampling rate is derived using Equation (4.22).

The power consumption of the SBTDC-II prototype is proportionate to the time difference that it quantizes. The SBTDC-II prototype is only active during a

TABLE 5.1: Noise Breakdown of the SBTDC-II Prototype

Noise Source	RMS Noise
Quantization noise, σ_{qe}	0.29Δ
Accumulated GRO jitter noise, $\sigma_{GRO,acc}$	$0.088\Delta/\sqrt{\text{cycle}}$
Other TDC noise sources, $\sigma_{TDC,other}$	0.28Δ

time quantization, and is disabled at all other times. Therefore, it consumes more power for larger time differences. At a sampling rate of 25 MS/s, the SBTDC-II prototype consumes 1.15 mW of average dynamic power for a near full range time difference of 33.5 ns.

Using Equation (4.23) and Equation (4.24), the effective number of linear bits (N_{linear}) and figure of merit (FoM_{TDC}) of the SBTDC-II prototype are calculated to be 11.6-bit and 14.8 fJ/conv.-step, respectively.

The performance of the SBTDC-II prototype is summarized in Table 5.2. It can be compared with the BTDC and SBTDC-I prototypes, and other recently reported TDCs in the literature. Table 5.2 is a further extension of Table 4.4.

As compared to the other TDCs in the literature, the SBTDC-II prototype does not need to achieve an aggressively fine TDC time resolution. Its required TDC time resolution is relaxed by the time interval amplification capability of the proposed VCO-based VTC. Hence, the SBTDC-II prototype only achieves a comparatively decent TDC time resolution of 4.13 ps.

The power and area consumption of the SBTDC-II prototype are much lower than the SBTDC-I prototype. These outcomes can be attributed to the less aggressive TDC time resolution and the full custom implementation of the SBTDC-II prototype.

In addition, the full custom implementation of the SBTDC-II prototype has improved its INL as compared to the SBTDC-I prototype. The INL has improved from 2.94 LSB to 1.63 LSB. This improvement in INL is in spite of using a lower amount of redundancy for the SBTDC-II prototype. Nevertheless, the DNL and INL of the SBTDC-II prototype at 1.98 LSB and 1.63 LSB, respectively, are on the high side as compared to the other TDCs.

TABLE 5.2: Performance Summary of Proposed TDCs and Other Recently Reported TDCs

TDC:	JSSC 18 [64]	JSSC 14 [62]	JSSC 15 [59]	JSSC 18 [42]	JSSC 18 [45]	TVLSI 16 [49]	JSSC 10 [34]	ISSCC 15 [50]	BTDC	SBTDC I ^g	SBTDC II
Architecture	RNS	Pipeline	1–3 MASH	2 Step + SES	2-D Spiral Vernier	Parallel Sample	Parallel Lines	Stochas	Branch	Stochas Branch	Stochas Branch
Technology	45nm	65nm	65nm	65nm	45nm SOI	65nm	40nm	14nm Fin	40nm	65nm	40nm
Total Bit (bit)	8.94	9	11	8	8	14	14	10	12	14	13
N_{linear} (bit)	7.80	7.57	9.30	6.83	7.58	13.4	13.1	8.28	9.80	12.0	11.6
Resolution (ps)	9.40	1.12	2.64 ^b	0.45	1.25	6.00	5.50	1.17	36.2	0.85	4.13
F_S (MS/s)	215	250	150	50–200	80	1	40	100	5	125	25
DNL (LSB)	0.57	0.60	–	0.65	0.25	0.12 ^d	0.60 ^d	0.80	1.30	0.27 ^h	1.98
INL (LSB)	1.10	1.70	2.24	1.25	0.34	0.50 ^d	0.81 ^d	2.30	3.61	2.94 ^h	1.63
SSP (LSB)	0.74	0.69	0.18	1.70	0.31	1.83	0.80	–	0.75	–	1.05
Power (mW)	24.2	15.4	3.52	3.90 ^c	0.69	0.28	1.80	0.78 ^e	0.28	70.8	1.15
FoM_{TDC} (fJ/C.-s)	505	325	37.1	343	45.1	25.6	4.97	25.1	61.9	136	14.8
Area (mm ²)	0.081	0.140	0.032	0.089	0.040	0.120	0.010	0.036	0.043	0.221	0.016
Resolution Cal. ^a	No	No	No	FG	BG	No	No	No ^f	FG	FG	FG
Linearity Cal. ^a	No	No	No	FG	BG	BG	FG	NR	No	NR	NR

^aNR: Not Required / FG: Foreground / BG: Background.^bEffective resolution based on integration bandwidth of 15 MHz.^cAt F_S of 100 MS/s. TDC part of PLL, excluding VCO & divider powers of coarse TDC.^dMeasured DNL & INL based on their 6-bit [49] or 5-bit [34] fine TDC.^ePower of external 850 MHz clock is not included.^fResolution depends on external clock.^gSimulated results.^hSimulated DNL & INL based on its 8-bit fine TDC.

Overall, the SBTDC-II prototype has achieved a competitive figure of merit of 14.8 fJ/conv.-step. Its figure of merit is second best among the TDCs that are summarized in Table 5.2.

5.6.2 Overall Time-Mode ADC Results

The proposed time-mode ADC is measured at a sampling rate of 15 MS/s instead of 16.67 MS/s. The slightly lower sampling rate is due to the limited number of pads and the limitations of the serial-parallel interface of the fabricated chip. Hence, the proposed time-mode ADC has a bandwidth of 7.5 MHz in this measurement.

The full system performance of the proposed 8-bit time-mode ADC including its back-end LUT is characterized.

The static performance of the proposed time-mode ADC is characterized using the code density test where 8.25×10^6 samples are collected. The code density test is also used to average out the noises of both the proposed time-mode ADC and the measurement setup. The measured DNL and INL of the proposed time-mode ADC with back-end LUT applied are plotted in Figure 5.22. The proposed time-mode ADC achieves good DNL and INL performances with the help of the back-end LUT. It achieves a maximum/minimum DNL of 0.40 LSB/−0.43 LSB, and a maximum/minimum INL of 0.46 LSB/−0.50 LSB.

The dynamic performance of the proposed time-mode ADC is characterized using the single-tone test. The measured output spectrums of the proposed time-mode ADC for a Nyquist input frequency (f_{IN}) of 7.49 MHz before and after applying the back-end LUT are shown in Figure 5.23(a) and Figure 5.23(b), respectively. The output spectrums are obtained using 32768-point fast Fourier transforms (FFT). Note that coherent sampling is applied.

It can be observed from Figure 5.23(a) that before the back-end LUT is applied, the raw linearity of the proposed time-mode ADC is limited by its harmonic distortions. At this input frequency, its total harmonic distortion (THD) is measured to be 27.20 dB. Thereby, limiting its SNDR to 27.03 dB. Its spurious-free dynamic range (SFDR) is limited to 30.07 dB by its second harmonic. The raw resolution of the proposed time-mode ADC is not limited by its SNR at 41.09 dB. The harmonic distortions of the proposed time-mode ADC are mainly due to the

FIGURE 5.22: Measured DNL and INL of the proposed time-mode ADC. It achieves maximum/minimum DNL and INL of 0.40 LSB/ -0.43 LSB and 0.46 LSB/ -0.50 LSB, respectively.

FIGURE 5.23: Measured output spectrums of the proposed time-mode ADC for f_{IN} of 7.49 MHz at F_S of 15 MS/s. The LUT reduces the harmonic distortions of the proposed VCO-based VTC. (A) Before LUT is applied. 27.03 dB SNDR is achieved. (B) After LUT is applied. 39.90 dB SNDR is achieved.

non-linearity of its VCO-based VTC as discussed at the end of Section 5.2.1. In other words, the linearity of the proposed VCO-based VTC is the bottleneck for the overall time-mode ADC. Comparing between Figure 5.7(b) and Figure 5.23(a), it can be seen that the raw linearity of the proposed time-mode ADC is in good agreement with the simulated linearity of the proposed VCO-based VTC.

Comparing between Figure 5.23(a) and Figure 5.23(b), it can be observed that the back-end LUT is able to correct the non-linearities of both the proposed VCO-based VTC and the SBTDC-II prototype. After applying the back-end LUT, the measured THD of the proposed time-mode ADC has been reduced from 27.20 dB to 51.75 dB. The SFDR is now limited by the clock spur to 53.83 dB. However, the redundancy employed in the LUT matching has increased the quantization noise of the proposed time-mode ADC. Thereby, decreasing the SNR from 41.09 dB to 40.19 dB. Overall, the back-end LUT has increased the SNDR of the proposed time-mode ADC. The proposed time-mode ADC achieves a SNDR of 39.90 dB at this Nyquist input frequency.

The SNDR, SNR, and THD of the proposed time-mode ADC before and after applying the back-end LUT are plotted as functions of input frequency in Figure 5.24(a) and Figure 5.24(b), respectively.

FIGURE 5.24: Measured SNDR, SNR, and THD of the proposed time-mode ADC as functions of input frequency. (A) Before LUT is applied. 4.11-bit ENOB is achieved. (B) After LUT is applied. 6.33-bit ENOB is achieved.

Similarly, it can be observed from Figure 5.24(a) that before the back-end LUT is applied, the raw SNDR of the proposed time-mode ADC is limited by its THD. It achieves raw SNDR and ENOB of 26.52 dB and 4.11-bit, respectively. As discussed, the raw linearity of the proposed time-mode ADC is representative of the linearity of its proposed VCO-based VTC. Hence, Figure 5.24(a) also shows that the proposed VCO-based VTC achieves reasonable linearity and resolution for a rail-to-rail input range. The resolution achieved by the proposed VCO-based VTC is comparable with the other inverter based VTCs in the literature that are summarized in Section 2.1.4, Table 2.1. The other inverter based VTCs also have resolutions of only 4 to 5 bits. However, these VTCs do not achieve rail-to-rail input ranges.

Comparing between Figure 5.24(a) and Figure 5.24(b), the latter also shows that the back-end LUT has suppressed the THD of the proposed time-mode ADC. As a result, the SNDR of the proposed time-mode ADC is no longer limited by its THD. Instead, its SNDR is now limited by its SNR, or equivalently, its overall system noise. Overall, the proposed time-mode ADC achieves SNDR and ENOB of 39.90 dB and 6.33-bit, respectively, with the help of its back-end LUT.

However, the proposed time-mode ADC does not achieve the targeted ENOB of 7.2-bit due to its system noise. The main contributor to the system noise being the supply noise. Hence, for future prototypes, an on-chip LDO regulator could be used instead of an external LDO regulator to further suppress the supply noise. The on-chip LDO regulator will be able to circumvent the parasitic inductance of the bonding wire. A differential architecture of the proposed time-mode ADC could also be utilized to suppress the common mode noise of the system.

The SNDR, SNR, and THD of the proposed time-mode ADC for an input frequency of 183 kHz are plotted as functions of sampling rate (F_S) in Figure 5.25. Note that the back-end LUT is applied to the proposed time-mode ADC. Figure 5.25 verifies the dynamic performance of the proposed time-mode ADC across varying sampling rates. It achieves SNDR and ENOB of 39.69 dB and 6.30-bit, respectively, across varying sampling rates.

The total noise of the proposed time-mode ADC (σ_{tot}) is calculated to be 10.04 ps, or equivalently, 0.89Δ from its measured SNR. The noise breakdown of the proposed time-mode ADC is summarized in Table 5.3. Since the proposed

FIGURE 5.25: Measured SNDR, SNR, and THD of the proposed time-mode ADC for f_{IN} of 183 kHz as functions of sampling rate. It achieves SNDR and ENOB of 39.69 dB and 6.30-bit, respectively, across varying sampling rates.

TABLE 5.3: Noise Breakdown of the Proposed Time-Mode ADC

Noise Source	RMS Noise
Total kT/C noise, σ_{kTC}	0.23 ps
Accumulated N-type VCO jitter, $\sigma_{NVCO,acc}$	3.35 ps
Accumulated P-type VCO jitter, $\sigma_{PVCO,acc}$	5.16 ps
Total SBTDC-II noise (with LUT), σ_{TDC}	3.70 ps
– Quantization noise, σ_{qe}	3.27 ps
– Accumulated core GRO jitter, $\sigma_{GRO,acc}$	1.29 ps
– Other TDC noise sources, $\sigma_{TDC,other}$	1.16 ps
Other ADC noise sources, $\sigma_{ADC,other}$	7.01 ps
Total proposed time-mode ADC noise, σ_{tot}	10.04 ps = 0.89 Δ

time-mode ADC operates in the time-domain, its noise sources are expressed in time quantities.

The kT/C noise (σ_{kTC}) arises from both the sampling capacitor (C_S) and the input capacitor of the proposed VCO-based VTC (C_{VTC}). These two capacitors sample the thermal noises of the switches in the track and hold circuit. The kT/C

noise in the time-domain can be expressed as follows.

$$\sigma_{kTC} = A_{VTC} \sqrt{\left(\frac{kT}{C_S + C_{VTC}} \right)} = 0.23 \text{ ps} \quad (5.35)$$

where A_{VTC} is the voltage-to-time gain of the proposed VCO-based VTC, k is the Boltzmann constant, and T is temperature.

The jitter noises of the N-type VCO and P-type VCO accumulate for the 8 cycles of their oscillations. Their accumulated jitter noises ($\sigma_{NVCO,acc}$ and $\sigma_{PVCO,acc}$) can be expressed by Equation (5.20), which is repeated here for convenience.

$$\sigma_{VCO,acc} = \sqrt{8} \sigma_{VCO,c} \quad (5.36)$$

where $\sigma_{VCO,c}$ is the single cycle jitter of the corresponding N-type VCO or P-type VCO. The accumulated jitter noises of the two VCOs can not be directly measured as their outputs are internal signals within the proposed time-mode ADC. Hence, their accumulated jitter noises are estimated from simulations. The maximum accumulated jitter noises of the N-type VCO and the P-type VCO across the rail-to-rail sampled voltage are simulated to be 3.35 ps and 5.16 ps, respectively.

The noise sources of the SBTDC-II prototype are discussed previously in Section 5.6.1 and summarized in Table 5.1.

For the quantization noise (σ_{qe}), note that the back-end LUT matches the $2^{9.46}$ output codes of the SBTDC-II prototype down to the final 2^8 output codes of the proposed time-mode ADC. This matching operation increases the quantization noise by a factor of $2^{1.46}$. Therefore, the quantization noise is increased from 1.19 ps to 3.27 ps. Note that the quantization time step is also increased from 4.13 ps to 11.34 ps.

For the maximum time difference of 3.29 ns produced by the proposed VCO-based VTC, the core GRO oscillates for 12.44 cycles. As discussed in Section 5.6.1, the single cycle jitter of the core GRO ($\sigma_{GRO,c}$) is estimated to be $0.088\Delta/\sqrt{\text{cycle}}$, or equivalently, 364.5 fs/ $\sqrt{\text{cycle}}$. Therefore, similar to Equation (5.34), the accumulated jitter noise of the core GRO ($\sigma_{GRO,acc}$) can be expressed as follows.

$$\sigma_{GRO,acc} = \sqrt{12.44} \sigma_{GRO,c} = 1.29 \text{ ps} \quad (5.37)$$

The other noise sources of the SBTDC-II prototype ($\sigma_{TDC,other}$) are estimated to be 0.28Δ , or equivalently, 1.16 ps as discussed in Section 5.6.1.

The other noise sources of the proposed time-mode ADC ($\sigma_{ADC,other}$) comprise of the rest of the noise sources in the system. These noise sources also include thermal and supply noises. The other noise sources of the proposed time-mode ADC are estimated to be 7.01 ps by subtracting the aforementioned noise sources in the mean-square from the measured total noise.

At a sampling rate of 15 MS/s, the proposed time-mode ADC consumes 562 μ W of average dynamic power for a Nyquist input signal.

The Walden figure of merit (FoM_{ADC}) for an ADC is expressed in Equation (2.29), and is repeated here for convenience.

$$FoM_{ADC} = \frac{Power}{2^{ENOB} F_S} \quad (5.38)$$

The Walden figure of merit for the proposed time-mode ADC is calculated to be 464 fJ/conv.-step using Equation (5.38).

The performances of the proposed time-mode ADC and other recently reported ADCs in the literature are summarized and compared in Table 5.4. The proposed time-mode ADC is compared with the following three types of ADCs:

1. Other non-hybrid time-mode ADCs that also use inverter based VTCs [9–11].
2. Hybrid time-mode ADCs with low to moderate sampling rates [8, 13] or with identical resolution [17].
3. A conventional SAR ADC with similar sampling rate and resolution [89].

As compared to the other non-hybrid time-mode ADCs, only the proposed time-mode ADC achieves more than 6-bit ENOB even though it does not achieve the targeted ENOB of 7.2-bit. In addition, it also achieves rail-to-rail input range, whereas the largest single-ended input range of the other non-hybrid time-mode ADCs is only 30% of V_{DD} . The proposed time-mode ADC is able to overcome the non-linearity of its VTC. Therefore, the input range of the proposed time-mode ADC is not limited by the non-linearity of its VTC, unlike the other non-hybrid time-mode ADCs.

TABLE 5.4: Performance Summary of Proposed Time-Mode ADC and Other Recently Reported ADCs

ADC:	JSSC 19 [89]	TCAS-II 16 [8]	JSSC 16 [13]	TVLSI 18 [17]	JSSC 16 [9]	TVLSI 16 [10]	TCAS-I 17 [11]	This Work
Architecture	Diff SAR	Diff Flash + Cap Dis	Diff SAR + INV	Diff Flash + INV	Diff INV	Diff INV	Diff INV	SE INV
Technology	65nm	0.18 μ m	90nm	65nm	65nm	65nm	65nm	40nm
V_{DD} (V)	1.00	1.80	0.70	1.00	1.30	1.05	1.00	1.10
Resolution (bit)	10	10	10	8	6	5	5	8
F_S (S/s)	20M	40M	4M	900M	10G	5G	5G	15M
Input Range (V)	± 0.80	± 1.80	± 0.70	–	± 0.15	± 0.18	± 0.30	1.10
DNL (LSB)	0.70	0.49	0.47	0.70	0.28	0.30	0.83	0.43
INL (LSB)	1.20	1.16	0.53	0.90	0.49	0.40	0.79	0.50
SNDR at Nyq (dB)	56.8	49.5	54.8	41.9	27.5	26.7	26.2	39.9
ENOB at Nyq (bit)	9.14	7.93	8.81	6.67	4.28	4.14	4.06	6.33
Power (mW)	0.15	6.10	0.00925	3.50	98.0	21.5	7.80	0.56 ^a
FoM_{ADC} (fJ/C.-s)	13.3	625	5.15	37.0	504	243	94.6	464
Area (mm ²)	0.081	1.210	0.041	0.029	0.073	0.170	0.096	0.022 ^a

^aBack-end LUT is not included in power and area consumption.

Since the proposed time-mode ADC is targeted for remote sensors in Internet-of-Things (IoT) applications, it does not need to achieve a high sampling rate. It is targeted to achieve low to moderate sampling rate. Hence, the 15 MS/s sampling rate of the proposed time-mode ADC is comparatively much lower than the 5 GS/s to 10 GS/s sampling rates of the other non-hybrid time-mode ADCs.

In fact, the proposed time-mode ADC sacrifices its sampling rate to achieve its 6.33-bit ENOB. The lower sampling rate of the proposed time-mode ADC allows it to incorporate time interval amplification capability into its proposed VCO-based VTC. The time interval amplification relaxes the required TDC time resolution of the SBTDC-II prototype. Consequently, the rail-to-rail sampled voltage can be easily quantized with 9.46-bit accuracy. This quantization includes 1.46-bit redundancy for the back-end LUT operation. The LUT with redundancy enables the proposed time-mode ADC to achieve its 6.33-bit ENOB.

However, for a single conversion, the proposed VCO-based VTC requires more power to generate an amplified time difference as compared to a non-amplified time difference. In addition, as can be seen from Table 2.1 in Section 2.1.4, the other non-hybrid time-mode ADCs use similar TDC time resolutions as the SBTDC-II prototype (i.e. T_{LSB} of 2 ps to 4 ps). Therefore, as compared to the TDCs of the other non-hybrid time-mode ADCs, the SBTDC-II prototype consumes more power to quantize a longer 9.46-bit time difference range at similar TDC time resolution of 4.13 ps.

Therefore, the proposed time-mode ADC does not have the best figure of merit among the non-hybrid time-mode ADCs. It only achieves a reasonable figure of merit of 464 fJ/conv.-step. In other words, the proposed time-mode ADC also trades off power with resolution.

As compared to the other hybrid time-mode ADCs and the conventional SAR ADC, the proposed time-mode ADC does not outperform them. These other ADCs are able to achieve either higher ENOBs at similar sampling rates [8, 13, 89], or 60 times higher sampling rate with similar ENOB [17]. At the same time, except [8], their figure of merits are much lower than the proposed time-mode ADC.

However, the proposed time-mode ADC does not require or have any analog blocks, unlike the other hybrid time-mode ADCs and the conventional SAR ADC. The proposed time-mode ADC does not have voltage references, reference drivers,

TABLE 5.5: Comparison Between Conventional SAR ADC and Proposed Time-Mode ADC

Conventional SAR ADC	Proposed Time-Mode ADC
✓ FoM_{ADC} in tens of fJ/conv.-step	✗ FoM_{ADC} of 464 fJ/conv.-step
✗ Reference generation	✗ Calibration effort
✗ Analog circuits unavoidable	✓ Highly digital and high scalability
✗ Larger area	✓ Small area

or amplifiers. Instead, it is built with mostly digital building blocks. Therefore, although the proposed time-mode ADC has poorer performance, it is better suited to scale with advancing CMOS technology. The other hybrid time-mode ADCs and the conventional SAR ADC will face challenges to scale with advancing CMOS technology.

5.6.3 Comparison of SAR ADC with Time-Mode ADC

Conventionally, SAR ADC is the preferred architecture for low power applications. In addition, SAR ADC is also very digital friendly and has the best scalability among the conventional ADC architectures. A comparison between the conventional SAR ADC and the proposed time-mode ADC is made in Table 5.5.

SAR ADC is able to achieve very low power consumption, and hence, can achieve excellent figure of merits in tens of fJ/conv.-step. This characteristic of SAR ADC is demonstrated by the conventional SAR ADC [89] and the hybrid time-mode ADC that uses a SAR ADC as its coarse ADC [13]. Their figure of merits are by far the best among all of the ADCs that are summarized in Table 5.4. The proposed time-mode ADC is not able to achieve as low power consumption as compared to a SAR ADC, evident by its figure of merit at 464 fJ/conv.-step.

Although the core of the SAR ADC is very digital friendly, it still requires a reference to be generated. This reference generation will require analog circuits such as a voltage reference and a reference driver. Hence, analog circuits are unavoidable for the SAR ADC. These analog circuits suffer from and become increasingly difficult to implement with advancing CMOS technology. In addition, as the supply reduces with advancing CMOS technology, the voltage size of the least significant

bit will also reduce for the same resolution of an ADC. Therefore, the power required by the reference driver and the size of its capacitor will increase in order to suppress its noise to be lower than the smaller least significant bit size. In other words, the cost and complexity problems of the reference generation will worsen with advancing CMOS technology.

Although the proposed time-mode ADC does not require reference generation for its operation, it requires considerable amount of calibration to correct the non-linearity of its VTC. The complexity, chip area, and implementation effort required for the calibration are non-trivial. The burden of reference generation as compared to VTC calibration can be considered to be similar even though they are two very different problems.

In terms of scalability, the proposed time-mode ADC is better. As discussed, the proposed time-mode ADC is built with mostly digital blocks and does not have any analog circuits. Hence, it will be able to scale with and reap the benefits of advancing CMOS technology. In addition, its digital nature enables it to consume a smaller amount of area as compared to the SAR ADC. This characteristic can be seen from Table 5.4, where the area of the proposed time-mode ADC at 0.022 mm^2 is the smallest among the ADCs that are summarized. The superior scalability and digital nature of the proposed time-mode ADC are its main advantages over the conventional SAR ADC.

Overall, the proposed time-mode ADC is not clearly better than the conventional SAR ADC at the current state-of-the-art. Depending on the requirements of the application and trade-off considerations, SAR ADC could be the better option over time-mode ADC. For example, SAR ADC will be chosen if power consumption is of absolute importance, and both time and effort can be devoted to the complexity of the reference generation. Alternatively, if a reference block is already present as part of an SoC, then SAR ADC will be preferred. However, if there is no need for a reference to be generated, then time-mode ADC will be the better option.

Nevertheless, the proposed time-mode ADC has demonstrated that the time-mode architecture is viable and has the ability to scale with advancing CMOS technology. The prospect of being able to shift a conventionally analog ADC into the digital domain will also continue to fuel research developments in this time-mode ADC architecture.

5.7 Summary

In summary, this chapter has presented the proposed 8-bit highly digital time-mode ADC with rail-to-rail input range. It has been verified in measurement using a sampling rate of 15 MS/s. It comprises of the conventional front-end track and hold circuit, the proposed VCO-based VTC, the 13-bit SBTDC-II prototype, and the back-end LUT.

The track and hold circuit uses a conventional bootstrapped switch to track the 1.1 V rail-to-rail input voltage, and holds it on a sampling capacitor for quantization. The track and hold circuit does not have a buffering amplifier. Hence, the loading of the succeeding VTC is taken into account during the design of the track and hold circuit.

The proposed VCO-based VTC converts the 1.1 V rail-to-rail sampled voltage into a proportionate 2.90 ns time difference. It has a voltage-to-time gain of 2.64 ns/V. It performs the voltage-to-time conversion using both an N-type VCO and a P-type VCO simultaneously. The opposite transfer functions of these two VCOs compensate each other to achieve a relatively linear rail-to-rail conversion. The proposed VCO-based VTC achieves an ENOB of 4.11-bit. In addition, the proposed VCO-based VTC exploits the oscillations of the two VCOs that have differing frequencies to achieve $8\times$ linear time interval amplification. Thereby, relaxing the required TDC time resolution of the succeeding TDC.

The SBTDC-II prototype quantizes the 2.90 ns time difference with a TDC time resolution of 4.13 ps. Therefore, the time difference is quantized into a 9.46-bit digital representation. In general, the SBTDC-II prototype has the same TDC architecture and operational principle as the SBTDC-I prototype. However, the SBTDC-II prototype is a full custom implementation and has an improved residue generator.

The SBTDC-II prototype has an effective interpolation factor of 6.4, where 2^6 stochastic interpolating rising edges are uniformly distributed within an oscillation period of its 10-stage core GRO. It uses a redundancy of only 1-bit.

The improved residue generator of the SBTDC-II prototype selectively delays the core GRO oscillation instead of the STOP signal. Effectively, it locks the fixed

time delay (t_{DEL}) to half of the core GRO oscillation period across PVT variations. Thereby, eliminating the timing margin issue of the proposed residue generator.

The SBTDC-II prototype is measured to achieve DNL, INL, and figure of merit of 1.98 LSB, 1.63 LSB, and 14.8 fJ/conv.-step, respectively, at a sampling rate of 25 MS/s.

The back-end LUT corrects the non-linearities of both the proposed VCO-based VTC and the SBTDC-II prototype. It does so by matching the non-ideal $2^{9.46}$ output codes from the SBTDC-II prototype down to their ideal 2^8 output codes.

Overall, the proposed time-mode ADC is measured to achieve DNL and INL of 0.43 LSB and 0.50 LSB, respectively. At a sampling rate of 15 MS/s, it achieves SNDR and ENOB of 39.9 dB and 6.33-bit, respectively. It consumes 562 μ W of average dynamic power for a Nyquist input signal. Therefore, the proposed time-mode ADC achieves a Walden figure of merit of 464 fJ/conv.-step.

The proposed time-mode ADC is built with highly digital circuitries. It does not require any analog blocks in its analog-to-digital conversion. Therefore, the highly digital nature of the proposed time-mode ADC enables it to scale well with advancing CMOS technology. Consequently, the proposed time-mode ADC can be integrated with other digital systems on a single chip in advanced CMOS technology. Thereby, forming System-on-Chip (SoC) sensors that consume low area and power. These SoC sensors fulfill the requirements of IoT remote sensing applications.

Chapter 6

Conclusion and Outlook

6.1 Conclusion

SENSORS form an ubiquitous part of our modern lives. They collect large amounts of data to be further deciphered by various data processors. This network of sensors and data processors forms part of the IoT. Many of these sensors are remotely operated. Therefore, these remote sensors have low area and power requirements such that they can be easily distributed and do not require heavy duty batteries.

The low area and power requirements can be achieved by integrating the analog front-end (AFE) with the digital systems to form SoC sensors in advanced CMOS technology. However, conventional ADCs do not scale well with advancing CMOS technology due to the reduced supply headroom, larger mismatch issues, and larger leakage currents. On the other hand, a time-mode ADC can be realized using highly digital building blocks, and can avoid the use of analog blocks. Therefore, this research proposes time-mode ADC as a solution that enables ADCs to be implemented in and scale with advancing CMOS technology. The objective of this research is to design and implement such a time-mode ADC that is scalable with advancing CMOS technology. Thereby, demonstrating that time-mode ADC is a feasible solution.

A time-mode ADC comprises of two sub-blocks. Namely, a VTC and a TDC.

In the TDC, arbiters, or equivalently, edge comparators arbitrate whether the START or the STOP signal arrives first at the delay stages of the delay line. An improved edge comparator with an input time hysteresis window of 55 fs is proposed in the first part of Chapter 3. Input time hysteresis for the proposed edge comparator is achieved through the SR latch memory effect, and the two additional NMOS transistors in the two discharge paths of the proposed edge comparator. These two NMOS transistors are connected in a negative feedback manner. Similar to voltage hysteresis in voltage comparator, time hysteresis for the proposed edge comparator enables it to be more robust against noise and jitters in repeated measurements.

A ring oscillator can be used as the delay line in the TDC. The ring oscillator enables the range of the TDC to be easily extended without incurring large additional overheads. The negative skewed delay scheme can be applied to the ring oscillator to increase its oscillation frequency by up to a factor of three. Thereby, enabling the TDC to achieve a finer TDC time resolution. This scheme is analyzed in the second part of Chapter 3. The proposed analysis shows that the oscillation frequency of an NSRO is improved by the coexistence of multiple oscillating edges. In addition, the proposed analysis is able to quickly determine the optimum configuration and oscillation behavior of an arbitrary length NSRO. The extension of the negative skewed delay scheme to differential ring oscillators and the phase noise of NSRO are also investigated. By understanding the negative skewed delay scheme, an optimum configuration of NSRO can be designed for the TDC implementation.

For the TDC implementation of the proposed time-mode ADC, a novel branching TDC architecture is proposed in Chapter 4. The underlying principle behind the proposed branching TDC architecture is to use a delay stage in a branching delay line to produce an additional interpolating rising edge in between two tap-to-tap rising edges from the core ring oscillator. Therefore, the TDC time resolution of the proposed branching TDC architecture can be finer than the tap-to-tap rising edges of the core ring oscillator. The interpolating rising edges can be positioned using a deterministic or a stochastic approach. The former and latter approaches are demonstrated by the 12-bit BTDC prototype and the 14-bit fully synthesized SBTDC-I prototype in the first and second parts of Chapter 4, respectively.

For the BTDC prototype, it has an interpolation factor of 4, and a TDC time resolution of 36.2 ps. At a sampling rate of 5 MS/s, it achieves a figure of merit of 61.9 fJ/conv.-step. For the SBTDC-I prototype, it has an effective interpolation

factor of 85.3, and an expected TDC time resolution of 850 fs. At a sampling rate of 125 MS/s, it achieves a figure of merit of 136 fJ/conv.-step.

In general, both branching TDC implementations have shown that they are able to achieve fine TDC time resolutions with wide measurement ranges. In addition, they are able to scale with advancing CMOS technology due to their highly digital structures. Therefore, the proposed branching TDC architecture is suitable for the proposed time-mode ADC.

Finally, the design and implementation of a 16.67 MS/s, 8-bit highly digital time-mode ADC are presented in Chapter 5. The proposed time-mode ADC is able to accept rail-to-rail voltage input. Its input range is not limited by the reduced supply headroom issue or the non-linearity of a VTC.

The proposed time-mode ADC has a proposed VCO-based VTC and a 13-bit SBTDC-II prototype. The proposed VCO-based VTC uses both an N-type VCO and a P-type VCO simultaneously to convert a rail-to-rail voltage into a proportionate time difference. In addition, the two VCOs also enable the time difference to be amplified by 8 times. The proposed VCO-based VTC achieves a voltage-to-time gain of 2.64 ns/V. The SBTDC-II prototype is a full custom implementation of the SBTDC-I prototype. It has an effective interpolation factor of 6.4, and a TDC time resolution of 4.13 ps. It achieves a figure of merit of 14.8 fJ/conv.-step at a sampling rate of 25 MS/s. The proposed time-mode ADC also uses a simple and straightforward back-end LUT to correct the non-linearities of both the proposed VCO-based VTC and the SBTDC-II prototype. At a sampling rate of 15 MS/s, the proposed time-mode ADC achieves SNDR, ENOB, and Walden figure of merit of 39.9 dB, 6.33-bit, and 464 fJ/conv.-step, respectively.

The proposed time-mode ADC does not have any voltage references or amplifiers in its implementation. It is built with mostly digital building blocks. Therefore, the proposed time-mode ADC has a highly digital structure that enables it to scale well with advancing CMOS technology.

In conclusion, the proposed time-mode ADC has demonstrated that time-mode ADC is a viable and promising solution for enabling ADCs to be continuously implemented in and scale with advancing CMOS technology. Therefore, time-mode ADC is a feasible solution for realizing SoC sensors in advanced CMOS technology. These SoC sensors are suitable for IoT remote sensing applications.

6.2 Prospects of Time-Mode ADC

A time-mode ADC converts an analog voltage signal into the time-domain to exploit the benefits of time-domain processing. However, in the voltage-to-time conversion, RC characteristic cannot be avoided. This RC behavior of VTCs can only be minimized. Therefore, it might be difficult for a time-mode ADC to achieve more than 10-bit resolution. The bottleneck of the time-mode ADC being the linearity of its VTC.

Innovative circuit techniques will be required to linearize the voltage-to-time conversion. For example, in the time-mode VCO-based ADC proposed by Xing and Gielen [12], a second VCO in a separate feed-forward path is used to cancel out the harmonic distortions of the first VCO. Thereby, enabling this VCO-based ADC to achieve an ENOB of 9.59-bit. Alternatively, aggressive calibration schemes will have to be developed to correct and compensate for the non-linearity of the VTC.

If the voltage-to-time conversion can be linearized, time-mode ADCs have the potential to achieve giga-samples per second sampling rates with good resolutions. As demonstrated by [9–11], these time-mode ADCs have sampling rates of 5 GS/s to 10 GS/s.

Nevertheless, time-mode ADCs are currently able to serve specific applications where high sampling rates are required, and can suffice with low resolutions. For example, the time-mode ADC of [10] is perfect for radio-astronomy application. This time mode ADC has a sampling rate of 5 GS/s albeit low ENOB of 4.1-bit. In this example, the high sampling rate of time-mode ADC is especially beneficial as time interleaving is not acceptable for this application. Therefore, time-mode ADCs will continue to thrive for such applications.

In addition, the ability of a time-mode ADC to be built with mostly digital building blocks will continue to attract research interests. The highly digital nature of time-mode ADC enables it to reap the benefits of CMOS scaling. Therefore, time-mode ADC can exploit CMOS scaling to potentially achieve good performance. The same cannot be said for conventional ADCs due to the impairments that affect analog circuits from CMOS scaling.

On a separate note, if the analog signal is already in the time-domain such as in traditional time-of-flight measurement, TDC is well developed to perform this measurement with outstanding performance. The outstanding performances of the state-of-the-art TDCs are shown in Chapter 5, Table 5.2. In particular, the SBTDC-II prototype is able to quantize a time input with a TDC time resolution of 4.13 ps. It can measure up to a range of 13-bit. Furthermore, it has low power consumption such that it achieves a low figure of merit of 14.8 fJ/conv.-step at a sampling rate of 25 MS/s.

6.3 Recommendations for Future Works

6.3.1 Improving Linearity of VTC

In the proposed time-mode ADC, the back-end LUT is used to linearize the proposed VCO-based VTC. Although the LUT approach is simple, it is basic and inefficient.

A known input signal is required for the proposed time-mode ADC to build its back-end LUT. The accuracy of the LUT is dependent on the quality of the known input signal. Therefore, the hardware required to generate the known input signal is burdensome, complex, and expensive. For IoT remote sensing applications, the generation of the known input signal is a serious drawback in terms of cost effectiveness.

Furthermore, the LUT needs to be constantly refreshed to adapt to changes in the environment. Since the LUT is built in the foreground, there will be periodic pauses in the operation of the proposed time-mode ADC to refresh the LUT.

Therefore, a better, more efficient, and more accurate calibration scheme could be developed for the proposed time-mode ADC. Preferably, the improved calibration scheme should operate in the background so as to ensure that the proposed time-mode ADC is always accurately calibrated. The cost effectiveness of the improved calibration scheme should also be evaluated.

In general, as mentioned in the previous section, further researches could be pursued to improve the linearity of a VTC. Innovative circuit techniques or aggressive calibration schemes could be developed to linearize a VTC. Thereby, enabling a time-mode ADC to achieve better resolution.

6.3.2 Improving Linearity of SBTDC-II Prototype

The static DNL and INL of the SBTDC-II prototype at 1.98 LSB and 1.63 LSB, respectively, could be further improved. The linearity of the SBTDC-II prototype could be improved through better layout techniques, or through a better control over the propagation delays of the delay stages in the branching delay lines.

6.3.3 Research on Hybrid Time-Mode ADC

Hybrid time-mode ADC comprises of a coarse conventional ADC and a fine time-mode ADC. Therefore, it is potentially able to reap the best of both worlds. The weaknesses of the conventional ADC could be complemented by the time-mode ADC, and vice versa.

Although it is challenging to build high performance analog circuits in an advanced CMOS technology, it is not impossible. In addition, the time-mode ADC could be used to alleviate the performance requirements of the analog blocks. For instance, redundancy could be designed into the time-mode ADC such that the analog blocks could be less accurate.

At the same time, since the fine time-mode ADC only quantizes the residue from the coarse conventional ADC, the input range of the time-mode ADC is reduced substantially. Therefore, it is easier for the VTC of the time-mode ADC to achieve better linearity. In addition, the time-mode ADC can potentially operate at a lower supply. Thereby, reducing power consumption.

Therefore, other than pure time-mode ADC, hybrid time-mode ADC is also a promising research direction for implementing high performance ADC in advanced CMOS technology.

List of Author's Publications

Journal Articles

- **J. S. Teh**, A. R. Palaniappan and L. Siek, "Analysis of Negative Skewed Delay Scheme for Ring Oscillator With Multiphase Outputs," submitted to *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*.
- **J. S. Teh** and L. Siek, "A 12-bit Branching Time-to-Digital Converter With Power Saving Features and Digital Based Resolution Tuning for PVT Variations," submitted to *Analog Integrated Circuits and Signal Processing*.

Conference Proceedings

- **J. S. Teh**, L. Siek, A. M. Alonso, A. Firdauzi and A. Matsuzawa, "A 14-b, 850fs Fully Synthesizable Stochastic-Based Branching Time-to-Digital Converter in 65nm CMOS," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018, pp. 1-5.
- **J. S. Teh** and L. Siek, "Novel Edge Comparator with Input Time Hysteresis for Improved Edges Arbitration," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018, pp. 1-5.
- **J. S. Teh**, R. P. Arjun, L. Siek and Y. Zheng, "Review of pulse generators for gated ring oscillator based Time-to-Digital converters," *2016 International Symposium on Integrated Circuits (ISIC)*, Singapore, 2016, pp. 1-4.
- **J. S. Teh**, A. Do, T. T. Kim and L. Siek, "A 28.4 pj per conversion ISFET-based pH sensing design for low-energy applications," *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Singapore, 2015, pp. 174-177.

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