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High Robustness Energy- and Area-Efficient Dynamic-Voltage-Scaling 4-phase 4-rail Asynchronous-Logic Network-on-Chip (ANoC)

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Abstract —We propose an 18-bit 5-interface asynchronous-logic Network-on-Chip (ANoC) router based on the quasi-delay-insensitive (QDI) realization approach for high secured cryptography applications. There are four key features of the proposed ANoC router. First, it embodies the novel high-speed low-power Sense-Amplifier Half Buffer 4-rail cells. Second, it is designed based on QDI protocol, and hence is highly robust against process-voltage-temperature (PVT) variations. Third, it is functional for full dynamic voltage scaling from nominal ($V_{DD}=1.2V$) to sub-threshold ($V_{DD}=0.3V$) regions, and is potentially excellent for low power management applications. Fourth, it embodies a distributed-based XY routing algorithm to utilize a 4-bit header of flow control unit (flit) for routing up to 4×4 cluster, hence minimizing the routing overhead. We realize the proposed ANoC router (@65nm CMOS), and benchmark it against the reported ANoC router embodying the conventional Weak-Conditioned Half-Buffer (WCHB) QDI realization approach. Both our proposed and reported designs feature the high operation robustness, but our design is 41% more energy-efficient, and 21% more area-efficient than the reported counterpart. The prototype of ANoC router occupies only 0.105 mm² and can operate down to 0.3V. At $V_{DD}=0.3V$, it dissipates 44 fJ per bit and operate 105 ns per flit.

I. INTRODUCTION

Designing a System-on-Chip (SoC) [2] realized by Network-on-Chip (NoC) [3]-[9] is a promising research area applicable to many applications, including defense and security applications. The basic premises for NoC-based SoCs include good scalability/routability (due to duplication of μP and NoC), improved speed (due to parallel processing) and high energy-efficiency (due to effective routing and computations). For our security application, we illustrate in Fig. 1 our targeted NoC-based SoC, comprising 9 processing units which are connected through their respective NoC routers. Among the 9 processing units, 6 are programmable microprocessors (μP_0 to μP_5) that can be programmed for processing various algorithms. The remaining processing units are a crypto- μP (to encrypt/decrypt data), a secured non-imprinting SRAM (to store sensitive data) and a globally shared SRAM. Each processing unit embodies its individual power supply. The supply voltage can be adjusted for Dynamic-Voltage-Scaling (DVS) [11].

To design such low power yet reliable NoC-based SoC, one of the main issues is the design of NoC routers (and the associated power management controller). To-date, there are many NoC routers reported [3]-[9], including those based on fully synchronous-logic (sync) and those in part based on asynchronous-logic (async). The design of sync NoC routers, however, becomes increasingly more challenging due to the timing issues for operation correctness. The timing issues are further compounded in view of wider Process-Voltage-Temperature (PVT) variations [2] in deep-submicron fabrication processes. Conversely, the design of async NoC

(ANoC) routers [3]-[9] has increasingly become attractive in accommodating timing and data synchronization issues because their operations are essentially self-timed. Their self-timed operation can often be utilized for low power dissipation such as with the techniques associated to DVS and/or leakage power reduction [9],[11].

Fig. 1: Proposed NoC-based SoC for our security application

Of many reported ANoC routers, they can be generally realized using the bundled-data approach or the Quasi-Delay-Insensitive (QDI) approach [12]. The ANoC routers using the bundled-data approach include MANGO [4], SCAFFI [5], ASPIN [6], and QNoC [7]. These bundled-data ANoC routers are undesirably relied on timing assumptions, and are somewhat not robust towards PVT variations. In contrast, the ANoC routers using the QDI approach include ALPIN [3], QoS [8], and FAUST [9]. These QDI ANoC routers were reported to be operationally robust and power-efficient. Of particular interest, the ALPIN ANoC router adopts 4-rail data encoding where each rail matches one direction for data propagation, hence simplifying its implementation. However, the reported ALPIN ANoC router [3] adopts the conventional QDI Weak-Conditional Half-Buffer (WCHB) realization approach which requires a huge amount of C-Muller circuit overheads, hence somewhat compromising the energy-efficiency of the overall NoC router.

In this paper, we propose an 18-bit 5-interface ANoC router with emphases on high robustness and low energy dissipation for our NoC-based SoC security application. Our proposed ANoC router features several significances. First, we leverage on our Sense-Amplifier Half Buffer (SAHB) realization approach [1] to design novel 4-rail async cells structurally appropriate for the realization of our proposed ANoC router. Second, our proposed ANoC abides by QDI, making it robust in accommodating the timing and PVT variations. Third, our proposed ANoC router features full DVS (nominal voltage $\leftrightarrow$ near-threshold voltage $\leftrightarrow$ sub-threshold); reported ANoC routers had only limited DVS (e.g. nominal voltage $\leftrightarrow$ near-threshold voltage). Viewed differently, our proposed ANoC router will be more advantageous for low power management

in the NoC-based SoC. Lastly, we apply the distributed-based XY-algorithm routing [5] for our ANoC router, minimizing the routing overhead to only 4-bit header flit for routing up to 4×4 cluster. The proposed ANoC router is implemented based on the 65nm CMOS process. We benchmark it against the reported ANoC router embodying WCHB. We show that our proposed ANoC is 41% more energy-efficient and 21% more area-efficient than its reported counterpart. The prototype of ANoC router occupies 0.105mm^2 and can operate as low voltage as 0.3V. At $V_{DD}=0.3\text{V}$, it dissipates 44fJ per bit and operates 105ns per flit.

This paper is organized as follows. Sec. II describes our proposed ANoC router and Sec. III presents measurement and comparison results. Finally, the conclusions are drawn in Sec. IV.

II. PROPOSED ASYNC NOC (ANoC)

We adopt a 2D mesh, distributed-based XY algorithm routing [5] for our proposed ANoC router. The following subsections describe the realization of the proposed ANoC router, including its interface architecture, the SAHB 4-rail cell design, and the design implementation.

A. NoC Interface Architecture

In the 2D-mesh NoC topology, an NoC router, as depicted in Fig. 1 earlier, comprises five interfaces, each having an input port and an output port. Four interfaces are used to transfer data to/from four directions (i.e. north (N), east (E), south (S) and west (W)) between two neighboring NoC routers/IOs, and the last interface to transfer data between the NoC router and its respective processing unit. Fig. 2 depicts the block diagram of one router interface where the input and output ports are depicted in (a) and (b) respectively. In Fig. 2, the bold dark lines represent the data packet, the straight lines represent the control signals and the dotted lines represent the acknowledge signals. In the input and output ports, every data packet and control signal is accompanied by an acknowledge signal for one complete async operation.

The input port consists of a virtual channel (VC) Demux, and two identical input VCs (i.e. IVC0 and IVC1). The VC Demux first selects either IVC0 or IVC1 for propagating the data packet, depending on the select signals $Send0$ and $Send1$. The select signals are triggered by the traffic conditions in the NoC router according to the routing mechanism [3]. In each input VC, the Path Generator decodes the destination information (in the header data packet) to produce the routing direction. Next, the Signal Packet triggers Pkt_i ($i = N, E, S$ or W directions) and allows the data packet to propagate to the designated output port (one of the 4 directions). As the control signals are required to transmit over two pipeline stages (i.e. the Path Generator and the Signal Packet), two Buffers, forming another two pipeline stages, are used to synchronize the data packet. Once the designated output port processes the sent data packet, Acc_i is triggered and the Gather Accept combines Acc_i from all directions to generate $Acc0/Acc1$ to acknowledge handshake operation.

The output port consists of a Signal Accept, a VC Arbiter, a VC switch, and two identical output VCs (i.e. OVC0 and OVC1). In each output VC, the Direction Switch selects the prioritized data packet sent from the input port. The Direction Arbiter runs the arbitration among the various incoming Pkt_i and decides the direction for prioritized data packet. This is to allow the first comer to continuously occupy the traffic channel such that the late comers have to wait until all flits of the first comer are all propagated. The Buffers synchronize and propagate the data packet and the control signal.

The Signal Accept collects the output control signals from the Direction Switch and triggers Acc_i to be sent to the input port. The VC Arbiter runs the arbitration among OVC0 and OVC1 and generates the VC prioritizing signal. The VC Switch selects the prioritized data packet to be sent out to the succeeding NoC router, and triggers $Send0/Send1$, depending on the input control signals $Acc0/Acc1$.

Fig. 2: ANoC Router Interface (a) Input port, and (b) Output port

Fig. 3: Proposed SAHB Buffer Cell

B. Sense-Amplifier Half Buffer (SAHB) 4-rail Cell Design

The functions [3] described in the input and output ports can be easily realized by buffering, multiplexing and demultiplexing. Hence, for our async ANoC router, the most critical cells are the buffers, multiplexers and de-multiplexers. We leverage on our SAHB realization approach, and design async cells for 4-rail encoding; the original SAHB cells are based on the dual-rail encoding [10]. The SAHB 4-rail cells are designed at transistor-level. For illustration, Fig. 3 depicts the SAHB 4-rail buffer cell, which comprises 4 functional blocks, two control-logic-cum-sense-amplifier (CLSA) blocks, and a completion detection. The functional blocks take in a set of the 4-rail input signals ($L.0$ to $L.3$) and generate a set of 4-rail output signals ($R.0$ to $R.3$); the acknowledgement signal from the succeeding pipeline ($Rack$) is integrated for on/off operation. The CLSA blocks control the sequence of async operation, and help amplifying the output and thereafter latching the output. The completion detection generates the acknowledgement signal to the preceding pipeline ($Lack$) from the 4-rail output signals through the NAND gate. The supply voltages V_{DDA} (for functional blocks) and V_{DD} (for remaining blocks) can be different. For proper operation, $V_{DD} \geq V_{DDA}$.

Our proposed 4-rail SAHB cells are designed to be QDI, hence inherently accommodating timing and PVT variations. For ease of comparison, Fig. 4 depicts the reported async 4-rail QDI WCHB cell used in the ALPIN router [3]. From operational modality viewpoint, the SAHB and WCHB 4-rail cells are functional equivalent. However, the reported WCHB realization approach is not efficient in terms of speed and power since it utilizes high-overhead C-Muller circuits to validate the signal completion. The number of C-Muller circuits increase significantly when the number of input sets ≥ 2 and thus further worsen the performance.

Fig. 4: Reported WCHB Cell

Table I compares the three most critical cells embodying SAHB and WCHB. The results are normalized to the cells embodying SAHB. The WCHB cells, on average, dissipate

1.7× more power, suffer 1.3× longer delay and occupy 1.15× more transistor-count than the SAHB cells.

TABLE I. COMPARISON OF THE SAHB AND WCHB CELLS FOR ANoC IMPLEMENTATIONS; NORMALIZED TO THE READINGS @ SAHB

	Power @ 1V, 1GHz		Delay @ 1V		Transistor-Count	
	SAHB	WCHB	SAHB	WCHB	SAHB	WCHB
Buffer	1× (9.2μW)	1.21×	1× (174ps)	1.17×	1× (63)	1.02×
1:2 De-Mux	1× (10.6μW)	2.31×	1× (235ps)	1.40×	1× (182)	1.19×
4:1 Mux	1× (25.8μW)	1.59×	1× (420ps)	1.32×	1× (298)	1.23×
Average	1×	1.70×	1×	1.30×	1×	1.15×

C. Design Implementation

The proposed ANoC router is implemented based on the 65nm standard-threshold-voltage CMOS process ($V_t \approx 0.5V$). We adopt a full-custom approach to implement the ANoC router. The layouts of all library cells, including the SAHB cells and standard single-rail library cells, are first hand-drafted using the Cadence Virtuoso Layout tool. For SAHB cells, many building blocks (i.e. function block, CLSA, and completion detection blocks) are similar, hence we standardize those similar building blocks for layout implementation. Some building blocks of the SAHB buffer cell are depicted in Fig. 5. The extracted library-exchange-format (LEF) files of all library cells are generated using the Cadence Abstract Generator tool. From the Verilog files, the SAHB ANoC router layout is placed and routed using the Cadence First Encounter tool. Eventually, the SAHB ANoC router layout is simulated and verified using the Synopsys Nanosim tool. The layout view and the microphotograph of the proposed ANoC router are shown in Fig. 6(a) and (b) respectively.

Fig. 5: Layout View of the Proposed SAHB Buffer Cell

Fig. 6: Proposed ANoC Router (a) Layout View, and (b) Microphotograph

III. RESULTS AND COMPARISONS

Fig. 7(a) depicts the measurement result of the proposed ANoC router @ the sub-threshold voltage of 0.3V. From the operation perspective, the ANoC router takes 840ns to complete 8 operations with 7.5 μ W. Hence the energy dissipation per-operation per-bit for the ANoC router is about 44fJ/bit. To demonstrate full-scale DVS, Fig. 7(b) depicts the operation of the proposed ANoC router under supply voltage scaling within the nominal (1.2V) to sub-threshold (0.3V) regions. We show that our ANoC router is functionally robust against the voltage variation and hence is suitable for applications require DVS.

Fig. 7: Measurement Results (a) $V_{DD} = 0.3V$ and (b) DVS ($0.3V \leftrightarrow 1.2V$)

Fig. 8 depicts the measured energy dissipation per-operation per-bit of the proposed ANoC router when $V_{DD} = 0.3V-1.2V$. Its lowest energy point occurs at 0.4V. Viewed differently, when the system throughput is not critical, we can enable DVS to save up to 89% of energy dissipation.

Fig. 8: Energy Dissipation per-bit of the Proposed ANoC Router

Table II tabulates the measurement result of the proposed ANoC router and its benchmarking against the reported WCHB counterpart. Particularly, our design occupies 21% smaller chip area than the reported counterpart when they are designed for 18-bit operation. Furthermore, our design is 41%

more energy-efficient than the reported counterpart @1.2V. This is mainly due to the lesser spurious switchings and lower leakage energy in the proposed novel SAHB 4-rail realization approach. In addition, the lower routing overheads in the proposed ANoC router also minimize the overall energy dissipation.

TABLE II. COMPARISON OF THE PROPOSED AND REPORTED ANoCs

	Proposed	Reported [3]
NoC topology	2D mesh	
Router port	5-interface router	
Flowing protocol	Async handshake 4-phase/4-rail QDI	
Flit size	18-bit	32-bit
Library cell	SAHB	WCHB
Area (mm ²)	0.105 (-21%)	0.134*
Energy/op*bit (fJ/bit) @ 1.2V	390 (-41%)	940*
Energy/op*bit (fJ/bit) @ 0.3V	44	NIL

*results after scaling to 18-bit operation based on transistor-count ratio

IV. CONCLUSIONS

We have proposed an energy-efficient high robustness ANoC router based on QDI high-speed low-power sense-amplifier half buffer approach. We have designed and implemented the proposed ANoC router (@ 65nm CMOS), and benchmarked it against the reported ANoC featuring WCHB approach. Although both designs are highly robust towards PVT variations, our design is ~41% more energy efficient and ~21% smaller area than the reported design.

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