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Triplet Spike Time Dependent Plasticity in a Floating-Gate Synapse

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Abstract—Synapse plays an important role of learning in a neural network; the learning rules which modify the synaptic strength based on the timing difference between the pre- and post-synaptic spike occurrence is termed as Spike Time Dependent Plasticity (STDP). The most commonly used rule posits weight change based on time difference between one pre and one post spike and is hence termed doublet STDP (D-STDP). However, D-STDP could not reproduce results of many biological experiments; a triplet STDP (T-STDP) that considers triplets of spikes as the fundamental unit has been proposed recently to explain these observations. This paper describes the compact implementation of a synapse using single floating-gate (FG) transistor that can store a weight in a nonvolatile manner and demonstrate the triplet STDP (T-STDP) learning rule by modifying drain voltages according to triplets of spikes. We describe a mathematical procedure to obtain control voltages for the FG device for T-STDP and also show measurement results from a FG synapse fabricated in TSMC 0.35 μ m CMOS process to support the theory. Possible VLSI implementation of drain voltage waveform generator circuits are also presented with simulation results.

Index Terms—SNN, STDP, BCM, floating gate, long term potentiation, long term depression, spike triplet, computational neuroscience.

I. INTRODUCTION

Over the past ten years, numerous experimental studies [1]–[4] have shown that the synaptic strength varies as a function of the precise spike timing difference $\Delta t = t_{post} - t_{pre}$ between the firing times t_{pre} and t_{post} of the presynaptic and postsynaptic neurons respectively. This synaptic plasticity rule, called Spike Time-Dependent Plasticity (STDP), has evolved as one of several unsupervised plasticity rules that play an important role in learning and memory in the brain. The mathematical model of STDP based on a pair of pre- and post-synaptic spike is referred as doublet STDP (D-STDP) while the one based on triplet of synaptic spikes [5]–[8] i.e either pre-post-pre synaptic spike or post-pre-post synaptic spike is referred to as triplet STDP (T-STDP). Several variants of these rules have also been proposed for pattern classification tasks [9], [10].

Experimental results [11] indicate that D-STDP model based on pairs of spikes are not sufficient to explain synaptic changes due to triplets or quadruplets of spikes. D-STDP model also fails to reproduce frequency effects. However, T-STDP model can reproduce frequency effects along with the explanation of synaptic changes due to triplets and quadruplets

of spikes. It is also important to be able to replicate rate based plasticity experiments. It has been demonstrated that the Bienenstock-Cooper-Munro (BCM) learning rule [12] based on firing rates can be obtained from D-STDP when pre-synaptic and post-synaptic neurons fire uncorrelated or weakly correlated Poisson spike trains, and only nearest-neighbor spike interactions are taken into account [13]. However, it is not possible to make a strict theoretical mapping from the nearest-spike interactions D-STDP models to the BCM rule [11] whereas T-STDP allows for such theoretical mapping. Apart from these experimentally observed benefits of T-STDP model, there are some computational advantages as well [14]. It has been shown that T-STDP can detect input correlations higher than the second order ones to which D-STDP is sensitive. Hence, it has been shown to drive direction and orientation selectivity [14]. Further, it can be shown to reproduce a more generalized version of BCM overcoming the limitations of the original one. Though there are several models of plasticity with varying degrees of bio-realism [15], T-STDP is a good compromise between simplicity and richness of function. Its simplicity also lends itself to easy analysis making it a good choice for a plasticity rule with functionality beyond D-STDP.

Recently STDP became so popular in computational neuroscience that neuromorphic engineers who try to emulate brain function using VLSI have also tried to emulate this behaviour in silicon. However, implementing a compact learning synapse continues to be one of the big challenges in the field [16]. Several recent papers have reported D-STDP implementations [17]–[21] and T-STDP implementation [22]; however, these synapses could either only store states in a transient fashion (using charge on a capacitor) or only hold two states in the long term. The size of these synapses are also large hindering scalability of these designs. A promising solution for non-volatile analog weight storage in very small area is provided by a floating-gate (FG) device [16], [23]–[30]. This concept was utilized recently to show weight storage and adaptation due to quantum phenomena based on input signal timing [30].

Compared to other work, here we demonstrate for the first time the implementation of the T-STDP rule in a FG synapse by appropriately modifying the drain voltage pulse based on spike triplets. From chip measurement results, we show that FG synapse in Fig. 3(b) can reproduce (1) D-STDP learning window and (2) T-STDP results when appropriate control signals are applied on its terminals. Some initial results for triplet experiment based on this work were presented in [31]. In this paper, we present results for quadruplet experiments and frequency effects as well as a new drain voltage generation scheme. We also present circuits for VLSI implementation of the drain voltage waveforms.

The paper is organized as follows: Section II provides a brief

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Fig. 1: STDP learning window; theoretical implementation of D-STDP: The plot is based on equation (1) with the parameters $A^+ = 4.6 \times 10^{-3}$ and $A^- = 3 \times 10^{-3}$

explanation of STDP models, D-STDP and T-STDP. Section III introduces the working of floating gate synapse, relation between FG synapse and D-STDP rule and then, finally arrive at the relation between FG synapse phenomenon and T-STDP rule. The experimental results are included in section IV. Section V presents a hardware implementation of the drain voltage waveform generator along with the simulation results. Finally the paper is concluded with discussions on consolidated work.

II. STDP SYNAPTIC MODIFICATION RULE

In biology, synapses are specialized structures that permit the transfer of signals between two neurons with an associated synaptic strength or weight. Learning typically implies the modification of synaptic weight due to the activities of the pre- and post-synaptic neurons. The STDP models are explained in detail next.

A. Doublet STDP (D-STDP) Model

In D-STDP, potentiation occurs when a postsynaptic spike succeeds a presynaptic spike; otherwise depression happens. The weight changes can be governed by a temporal learning window. The temporal learning window for STDP can be expressed as [11], [22]

$$\Delta w = \begin{cases} \Delta w^+ = A^+ e^{\left(\frac{-\Delta t}{\tau_+}\right)} & \text{if } \Delta t \geq 0 \\ \Delta w^- = -A^- e^{\left(\frac{\Delta t}{\tau_-}\right)} & \text{if } \Delta t < 0 \end{cases} \quad (1)$$

where $\Delta t = t_{\text{post}} - t_{\text{pre}}$ is the time difference between a post-synaptic and pre-synaptic spike, τ_+ and τ_- are the time constants of the learning window, and A^+ and A^- are the maximal weight changes for potentiation and depression, respectively. The theoretical graph for the above equation is simulated using MATLAB and is shown in Fig. 1 with the parameters being obtained by data fitting as explained in [11]. As mentioned in [2], τ_+ and τ_- are taken as 16.8ms and 33.7ms respectively for the simulation.

B. Triplet STDP (T-STDP) Model

Previous studies [7], [32] show that the D-STDP model fails to reproduce the experimental outcomes involving higher

order spike patterns such as triplet and quadruplets of spikes and furthermore, fails to account for the observed weight dependence on repetition frequency of pairs of spikes. To resolve the above mentioned issues, the D-STDP model was extended in [11] to include spike triplets resulting in T-STDP model which could sufficiently reproduce physiological experiments.

The T-STDP rule is written as a function of difference in spike timings as, [11], [22]

$$\begin{aligned} \Delta w^+ &= e^{\left(\frac{-\Delta t_1}{\tau_+}\right)} (A_2^+ + A_3^+ e^{\left(\frac{-\Delta t_2}{\tau_y}\right)}) \quad \text{if } t = t_{\text{post}} \\ \Delta w^- &= -e^{\left(\frac{\Delta t_1}{\tau_-}\right)} (A_2^- + A_3^- e^{\left(\frac{-\Delta t_3}{\tau_x}\right)}) \quad \text{if } t = t_{\text{pre}} \end{aligned} \quad (2)$$

where A_2^+ and A_2^- denote the amplitude of the weight change whenever there is a pre-post pair or a post-pre pair respectively. Similarly, A_3^+ and A_3^- denote the amplitude of the triplet term for potentiation and depression, respectively.

$\Delta t_1 = t_{\text{post}}(n) - t_{\text{pre}}(n)$, $\Delta t_2 = t_{\text{post}}(n) - t_{\text{post}}(n-1)$ and $\Delta t_3 = t_{\text{pre}}(n) - t_{\text{pre}}(n-1)$ are time difference between combinations of pre and post-synaptic spikes as shown in Fig. 2. τ_- , τ_+ , τ_x and τ_y are time constants for the above spike pairings.

In [11], though the T-STDP rule above is introduced first, it is shown later that not all terms are needed to explain biological data. Thus two different minimal models are defined later: (1) $A_2^+ = 0$ and $A_3^- = 0$ for visual cortex data and (2) $A_3^- = 0$ for hippocampal culture data set. Hippocampal culture data set [7] is used for obtaining the results for triplets of spikes whereas visual cortex data [32] is used for showing the frequency effects of T-STDP rule. For visual cortex data set, equation (2) simplifies to,

$$\Delta w(t) = \begin{cases} \Delta w^+ = A_3^+ e^{\left(\frac{-\Delta t_2}{\tau_y}\right)} e^{\left(\frac{-\Delta t_1}{\tau_+}\right)}; & t = t_{\text{post}} \\ \Delta w^- = -e^{\left(\frac{\Delta t_1}{\tau_-}\right)} (A_2^-); & t = t_{\text{pre}} \end{cases} \quad (3)$$

On the other hand, for hippocampal culture data set, equation (2) simplifies to,

$$\Delta w(t) = \begin{cases} \Delta w^+ = e^{\left(\frac{-\Delta t_1}{\tau_+}\right)} (A_2^+ + A_3^+ e^{\left(\frac{-\Delta t_2}{\tau_y}\right)}); & t = t_{\text{post}} \\ \Delta w^- = -e^{\left(\frac{\Delta t_1}{\tau_-}\right)} (A_2^-); & t = t_{\text{pre}} \end{cases} \quad (4)$$

For both cases, Δw^- is exactly same as the case of long term depression (LTD) in D-STDP as shown in equation (1). Hence, to implement the triplet rule in circuits, we only need to modify pre-existing FG design to add the extra term in the potentiation case.

III. FLOATING GATE SYNAPSE

Fig. 3(a) shows the architecture of a single floating gate synapse in prior work [30]. It has three main terminals for programming as shown in the dashed box. The terminals are named as gate, drain and tunnel terminals with the respective voltages denoted as V_g , V_d and V_{tun} . A “non-STDP” behaviour seen in this work is ameliorated in our previous work [25], [26] along with detailed analysis of the operation of the D-STDP learning rule in a floating gate synapse. In previous works [25], [26], [30], the quantum mechanism of tunneling

Fig. 2: Timing diagram of T-STDP rule: The timing specifications of data points (x-axis) for triplet experiments: protocol 1 and 2. A comparison of the temporal notations in this paper and [11] (mentioned as Pfister Paper in figure) is shown.

is spread across a larger time scale (illustrated in Fig. 4(a) and (b)) which makes it difficult to analyze the effect of triplets and quadruplets of spikes in a floating gate synapse. Similar to an approach in [28], [29], the effect of tunneling can be localized at the occurrence of pre-synaptic spikes with the modification (red blocks) shown in the architecture of Fig. 3(b) making it easier to mathematically analyze the weight change for triplets. In the new architecture, whenever a pre-synaptic spike occurs, a triangular gate voltage waveform is generated which will create an exponential excitatory post-synaptic current (EPSC), similar to biology, because of the exponential relationship between the gate voltage and drain current of the MOS transistor in subthreshold region. The current at the maximum gate voltage is nearly zero. Similarly, whenever a post-synaptic spike arrives, a global triangular tunnel voltage waveform and an inverted pulse drain voltage waveform is generated. The global triangular tunnel voltage waveform is then sampled at the occurrence of pre-synaptic spike with the help of pulse extender block and the multiplexer. This creates a voltage waveform, V_{tun_eff} at the tunnel terminal. Thus, in the new architecture, during pre-synaptic spike, a gate voltage, V_g and a tunnel voltage, V_{tun_eff} waveforms are generated and during post-synaptic spike, a drain voltage, V_d waveform is generated. Whereas, in the previous architecture, a gate voltage waveform is generated during pre-synaptic spike and both drain voltage and tunnel voltage waveforms are generated during post-synaptic spike.

The equation for drain current of a subthreshold saturated pFET whose well is tied to V_{dd} is given by [30]

$$I_d = I_{s0} e^{\kappa(V_{dd} - V_{fg})/U_T} \quad (5)$$

where U_T is the thermal voltage and κ is the gate coupling coefficient.

Weight modification in a FG synapse uses a combination of hot-electron injection (HEI) and Fowler-Nordheim tunneling [30]. HEI adds electrons on to the floating gate node, which reduces the floating gate voltage resulting in more current through the transistor hence increasing the weight of the synapse. On the other hand tunneling removes electrons from

Fig. 3: Floating Gate (FG) synapse: (a) The architecture used in previous work. (b) The architecture of a FG synapse used in this work with different input terminal voltage waveforms. The additional blocks used in the architecture is shown in red.

the FG node to reduce the synaptic weight. In our previous paper [25], for the case of D-STDP, a gate voltage waveform is generated at every pre-synaptic spike while at every post-synaptic spike, a tunneling voltage and a drain voltage is generated as illustrated in Fig. 4(a). This shows that at every pre-synaptic spike only tunneling happens while at every post-synaptic spike there is both injection and tunneling. The occurrence of both tunneling and injection at the post-synaptic spike arrival necessitates the effect of injection to be greater than tunneling to obtain potentiation as in the traditional D-STDP learning window. Moreover since the effect of tunneling is spread over a long time, mathematical analysis or intuitive understanding of the effect due to multiple pre- and post-synaptic spikes becomes difficult. In contrast, the mathematical versions of both STDP models have potentiation and depression of weights localized at pre- and post-synaptic events. Hence, to relate the mathematical analysis of FG synapse with the T-STDP model easily, we also decided to localize the effect of tunneling and injection at pre- and post-synaptic pulses respectively. A similar technique has also been used in [28], [29].

An illustration for this is shown in Fig. 4(b) where a tunneling voltage waveform is still created at every post

Fig. 4: Timing diagram and voltage specifications of FG synapse: (a) D-STDP model, cases of long term potentiation (LTP) and long term depression (LTD), where effect of injection and tunneling is present in LTP where as only tunneling effect is present for LTD. These waveforms are used in our previous paper (b) The details of timing and voltage specifications used for testing the FG synapse for both triplet protocols is shown here. The modification of tunneling voltage, V_{tun_eff} (shown in red) sampled from V_{tun} is shown. (c) Different cases of drain voltage waveform, V_d for different experiments like pairing protocol, triplets and quadruplets.

synaptic pulse as in earlier work [25], [30] but is not applied directly to the tunneling junction of the FG. Instead, it is sampled by the pre-synaptic pulse through a multiplexer to create a new waveform V_{tun_eff} , which is applied to the FG (refer to Fig. 3). Figure 4(b) also shows the specifications of terminal voltage waveforms for the case of triplets of spike. The well for the high voltage PMOS in the multiplexer can be shared with tunneling junction; nevertheless, this incurs an area penalty motivating us to look at possibilities of using non-localized tunneling for T-STDP in future. The governing equations for injection and tunneling are given as [30], [33]

$$I_{inj} = I_{inj0} (I_d / I_{s0})^\alpha e^{-\Delta V_{ds} / V_{inj}} \quad (6)$$

$$I_{tun} = I_{tun0} e^{(V_{tun} - V_{fg}) / V_{ox}}$$

where I_d is the drain current, $\alpha = 1 - U_T / V_{inj}$, V_{ox} and V_{inj} are process dependent parameters.

A. D-STDP Model on a Floating Gate Synapse (FG D-STDP)

The weight of the synaptic device can be defined as [30]:

$$w = e^{\frac{-\kappa V_{fg}}{U_T}} \quad (7)$$

Hence, equations to predict the change in FG voltage effectively predict the change in weight. The following assumptions are made in deriving the theoretical equations [25]:

- 1) To ensure small change in weight at very large negative and positive values of Δt , V_{g_init} has to be high enough so that $V_{tun_max} - V_{g_init}$ is small enough for negligible tunneling. Similarly $\Delta V_g = V_{g_init} - V_{g_min}$, should be small enough so that $V_{tun_init} - V_{g_min}$ is small enough for negligible tunneling.
- 2) Strong coupling from gate to floating gate node where as a weak coupling from tunneling node to floating gate node. This is justified since typically gate capacitance, $C_g \gg$ tunneling capacitance, C_{tun} .
- 3) The gate voltage waveform falls to its minimum value instantaneously. In other words, $S_1 \gg S_2, S_3$ as shown

in Fig. 4(a).

One difference from the earlier case in [25] is that now we only have injection for $\Delta t > 0$ and only tunneling for $\Delta t < 0$ due to the localization of tunneling effects.

We can now derive the slow time scale equation [30] for change in FG voltage due to tunneling and injection as:

$$C_T \frac{d\overline{V_{fg}}}{dt} = I_{tun} - I_{inj} = C_T \frac{d\overline{V_{fg,tun}}}{dt} - C_T \frac{d\overline{V_{fg,inj}}}{dt} \quad (8)$$

where C_T is the total capacitance on the FG node and $\overline{V_{fg}}$ denotes change on a slow time scale.

1) *Case 1: $\Delta t > 0$* : First, we consider the case of $\Delta t > 0$ i.e the positive axis of STDP curve and combine equations (6) and (5) to get:

$$C_T \frac{d\overline{V_{fg,inj}}}{dt} = -I_{inj0}(e^{\kappa(V_{dd}-V_{fg})/U_T})^\alpha e^{-\Delta V_{ds}/V_{inj}} \quad (9)$$

where $\overline{V_{fg,inj}}$ is the slow time scale change in V_{fg} due to injection only. Since change in V_{fg} on the RHS happens due to coupling from the gate voltage, we can write:

$$V_{fg} = V_{fg,min} + \frac{C_g}{C_T} S_2 t \quad (10)$$

where S_2 is positive slope of V_g and C_g is the capacitance connected between the gate terminal and the floating gate terminal. Here $V_{fg,min}$ is not same as $V_{g,min}$ due to initial charge stored on the FG. Substituting equation (10) in equation (9), we get

$$C_T \frac{d\overline{V_{fg,inj}}}{dt} = -A e^{-Xt} \quad (11)$$

where

$$\begin{aligned} A &= I_{inj0}(e^{\alpha\kappa(V_{dd}-V_{fg,min})/U_T})(e^{-\Delta V_{ds}/V_{inj}}) \\ X &= \frac{\alpha\kappa C_g S_2}{C_T U_T} \end{aligned} \quad (12)$$

Referring to Fig. 4(a), significant amount of injection happens in the time from Δt to $\Delta t + T_d$ (circled in red), where ΔV_{ds} is constant and significant. Also, since T_d is very small compared to T_g , we can assume that V_g is constant during the drain pulse. Hence, we finally get:

$$C_T \Delta \overline{V_{fg,inj}} = -A T_d e^{-X\Delta t} \quad (13)$$

For more details of the derivation, we refer the interested readers to [25].

With reference to Fig. 4(b), since we have modified the tunneling voltage waveform from V_{tun} to $V_{tun,eff}$ the effect of tunneling is not present in $\Delta t > 0$. Hence, we have $\Delta \overline{V_{fg}} = \Delta \overline{V_{fg,inj}}$.

2) *Case 2: $\Delta t < 0$* : Now we consider the case of $\Delta t = (t_{post} - t_{pre}) < 0$ i.e the negative axis of STDP curve. Similar to what we have done above, let us see the effect of tunneling and injection separately.

For the contribution of injection to $\overline{V_{fg}}$, we could see that injection happens only during the initial small period, T_d of time axis where the drain current of the MOS is almost zero. So we can completely neglect the effect of injection on $\overline{V_{fg}}$ in this case.

Now let us consider the contribution of tunneling to $\overline{V_{fg}}$. Similar to the analysis above, using assumption 1, we have:

$$C_T \int_0^{\Delta \overline{V_{fg,tun}}} dV_{fg} = \int_{-\Delta t}^{T_{tun}} I_{tun} dt \quad (14)$$

Also, similar to the case of positive Δt , here we have:

$$\begin{aligned} V_{fg} &= V_{fg,min} + \frac{C_g}{C_T} S_2 (t - (-\Delta t)) \\ V_{tun} &= V_{tun,max} + S_3 (t - T_{tun,delay}) \\ V_{tun,eff} &= \begin{cases} V_{tun}; & -\Delta t < t < -\Delta t + T_{tun,pulse} \\ V_{tun,init}; & \text{for other values of } t \end{cases} \end{aligned} \quad (15)$$

Substituting equations (15) and (6) into equation (14), we get

$$\begin{aligned} C_T \Delta \overline{V_{fg,tun}} &= B e^{\frac{-C_g S_2 \Delta t}{C_T V_{ox}}} \int_{-\Delta t}^{-\Delta t + T_{tun,pulse}} e^{Yt} dt \\ &= B' (e^{Y(T_{tun,pulse} - \Delta t)} - e^{-Y\Delta t}) e^{\frac{-C_g S_2 \Delta t}{C_T V_{ox}}} \end{aligned} \quad (16)$$

where

$$\begin{aligned} Y &= \frac{S_3 - \frac{C_g S_2}{C_T}}{V_{ox}} \\ B &= I_{tun0} (e^{\frac{V_{tun,max} - S_3 T_{tun,delay} - V_{fg,min}}{V_{ox}}}) \\ B' &= B/Y \end{aligned} \quad (17)$$

Since injection is negligible for $\Delta t < 0$, we have $\Delta \overline{V_{fg}} = \Delta \overline{V_{fg,tun}}$.

B. T-STDP Model on a Floating Gate Synapse (FG T-STDP)

Comparing equation (1) with equation (2), the extra term in T-STDP compared to the D-STDP model is $A_3^+ e^{\frac{(-\Delta t_2)}{\tau_y}} e^{\frac{(-\Delta t_1)}{\tau_+}}$, which occurs at the arrival of post-synaptic spike. Intuitively, for the case of triplet of spikes, we can see that there should be some modification to the drain voltage pulse compared to the doublet case since it is related to potentiation and is generated at the post-synaptic spike. There are two ways in which we can have more potentiation due to injection: (1) increase ΔV_{ds} or (2) increase injection pulse width T_d . Based on this, we propose the following two drain voltage waveform that accounts for triplet spike interactions:

- 1) *Single-pulsed V_d* : This case implements the entire potentiation term in equation (4) by a single pulse of width T_d at t_{post} (Fig. 4(d)) – however, the voltage V_d depends on the time difference Δt_2 between successive post spikes. So from Fig. 4(d) expression for V_d becomes:

$$V_d = \begin{cases} V_{d,min} - \Delta V_d^s(\Delta t_2); & t_{post}(n) < t < t_{post}(n) + T_d \\ V_{d,init}; & \text{for other values of } t \end{cases} \quad (18)$$

Note that to satisfy the results of the doublet case, $\Delta V_d^s(\Delta t_2) \rightarrow 0$; as $\Delta t_2 \rightarrow \infty$.

- 2) *Double-pulsed V_d* : The double-pulsed V_d waveform (Fig. 4(d)) implements the doublet term with the first

pulse of width T_d and amplitude same as in FG D-STDP. It then creates the extra triplet term with the following pulse again of width T_d but with different amplitude. The entire waveform is given by:

$$V_d = \begin{cases} V_{d.min}; & t_{post}(n) < t < t_{post}(n) + T_d \\ V_{d.min} - \Delta V_d^d(\Delta t_2); & t_{post}(n) + T_d < t < t_{post}(n) + 2 * T_d \\ V_{d.init}; & \text{for other values of } t \end{cases} \quad (19)$$

Again, note that to satisfy the results of the doublet case, $V_{d.min} - \Delta V_d^d(\Delta t_2) \rightarrow V_{d.init}$; as $\Delta t_2 \rightarrow \infty$ i.e second pulse in double-pulsed V_d vanishes as $\Delta t_2 \rightarrow \infty$.

As can be seen above, both cases of drain voltage waveform will require some different method to calculate $\Delta V_d^s(\Delta t_2)$ and $\Delta V_d^d(\Delta t_2)$ to match results from the T-STDP model with desired parameters. So, next we do a comparison of the FG phenomenon and T-STDP model to understand the kind of modification to be done. Here, we consider only the FG phenomenon of injection that happens at post-synaptic pulses, since our modification has localized tunneling to pre-synaptic events. Then, we can equate this to the weight change from T-STDP model for any specific case (e.g. hippocampal culture data set in [11]) to extract the exact parameters of the pulse drain waveform. Here, we will express the weight change for T-STDP normalized to D-STDP for ease of understanding; this is intuitively good since T-STDP has modifications on top of D-STDP. Let us consider this case by case.

1) Case 1: FG T-STDP for spike doublet inputs

The FG phenomenon on doublets of spike is exactly similar to the derivation shown in previous subsection III-A for single and double pulsed V_d cases. Therefore,

$$\overline{\Delta V_{fg.inj}^{doublet}} = A e^{-X \Delta t} e^{(V_{dd} - V_{d.min})/V_{inj}} \quad (20)$$

where

$$A = \frac{I_{inj0}(e^{\alpha \kappa (V_{dd} - V_{fg.min})/U_T})(e^{-X T_d} - 1)}{C_T X} \quad (21)$$

$$X = \frac{\alpha \kappa C_g S_2}{C_T U_T}$$

2) Case 2: FG T-STDP for spike triplet inputs

a) Single-pulsed V_d : Similar to the mathematics in case 1, we get:

$$\overline{\Delta V_{fg.inj}^{triplet}} = A e^{-X \Delta t} e^{\frac{\Delta V_d^s(\Delta t_2)}{V_{inj}}} e^{\frac{(V_{dd} - V_{d.min})}{V_{inj}}} \quad (22)$$

where A and X are same as above.

The ratio of change in weight due to FG T-STDP on triplets and doublets of spike is given as,

$$Y_{fg} = \frac{\Delta W_{inj}^{triplet}}{\Delta W_{inj}^{doublet}} = \frac{\overline{\Delta V_{fg.inj}^{triplet}}}{\overline{\Delta V_{fg.inj}^{doublet}}} = e^{\frac{\Delta V_d^s(\Delta t_2)}{V_{inj}}} \quad (23)$$

b) Double-pulsed V_d : Again, similar to the mathematics in case 1, we get:

$$\overline{\Delta V_{fg.inj}^{triplet}} = \overline{\Delta V_{fg.inj}^{doublet}} (1 + e^{-X T_d} e^{\frac{\Delta V_d^d(\Delta t_2)}{V_{inj}}}) \quad (24)$$

where X is same as above. Here, the term $e^{-X T_d}$ arises since the gate voltage has changed a little bit at the start of the second pulse compared to the first. Since $e^{-X T_d} \approx 1$ due to small value of T_d , the ratio of change in weight due to FG T-STDP on triplets and doublets of spike can be written as:

$$Y_{fg} = \frac{\Delta W_{inj}^{triplet}}{\Delta W_{inj}^{doublet}} = \frac{\overline{\Delta V_{fg.inj}^{triplet}}}{\overline{\Delta V_{fg.inj}^{doublet}}} = 1 + e^{\frac{\Delta V_d^d(\Delta t_2)}{V_{inj}}} \quad (25)$$

3) T-STDP rule for spike doublets and triplets

For the case of T-STDP and D-STDP models the ratio Y can be obtained directly from equation (4) as:

$$Y_{theory} = \frac{\Delta W_{triplet}^+}{\Delta W_{doublet}^+} = 1 + \frac{A_3^+ e^{\frac{(-\Delta t_2)}{\tau_y}}}{A_2^+} \quad (26)$$

Now, we can equate the Y_{fg} values in equations (23) and (25) with the Y_{theory} value in equation (26) to get the desired drain voltage parameters.

a) Single-pulsed V_d :

$$Y_{fg} = Y_{theory}$$

$$\Rightarrow e^{\Delta V_d^s(\Delta t_2)/V_{inj}} = 1 + \frac{A_3^+ e^{\frac{(-\Delta t_2)}{\tau_y}}}{A_2^+}$$

$$\Rightarrow \Delta V_d^s(\Delta t_2) = V_{inj} \ln(1 + \frac{A_3^+ e^{\frac{(-\Delta t_2)}{\tau_y}}}{A_2^+}) \quad (27)$$

b) Double-pulsed V_d :

$$Y_{fg} = Y_{STDP}$$

$$\Rightarrow e^{\Delta V_d^d(\Delta t_2)/V_{inj}} = \frac{A_3^+ e^{\frac{(-\Delta t_2)}{\tau_y}}}{A_2^+} \quad (28)$$

$$\Rightarrow \Delta V_d^d(\Delta t_2) = V_{inj} \ln(\frac{A_3^+ e^{\frac{(-\Delta t_2)}{\tau_y}}}{A_2^+})$$

C. Parameter Translation from Theory to FG model

Given values of parameters such as A_2^+ or A_3^+ of the theoretical model, it should be possible to use the above equations (27) and (28) to find the values of ΔV_d^s and ΔV_d^d . However, in our case, the measurement setup restricted the temporal width of voltage waveforms to a maximum value of 300ms (note the maximum time duration used for T_{tun}). Hence, compared to the learning window τ^+ (refer to Fig. 1) shown in [11], our learning window τ_{fg}^+ (Fig. 5) has lesser width. This implies that we need to apply a compression factor on the time scale to match our results with those in [11]. We define the compression factor r as follows:

$$r = \frac{\tau^+}{\tau_{fg}^+} \quad (29)$$

For the present case, we get the value of $r \approx 2$. Thus, to replicate the weight changes in [11], we need to reduce all the temporal dimensions in our case by the factor of r . This can be formally written as:

$$\begin{aligned} \Delta V_d^s(\Delta t_2/r) &= V_{inj} \ln(1 + \frac{A_3^+ e^{\frac{-\Delta t_2}{\tau_y}}}{A_2^+}) \\ \Delta V_d^d(\Delta t_2/r) &= V_{inj} \ln(\frac{A_3^+ e^{\frac{-\Delta t_2}{\tau_y}}}{A_2^+}) \end{aligned} \quad (30)$$

Next, we show this translation explicitly for the three experimental protocols considered in [11].

1) Triplet experiments:

For the different parameters of hippocampal culture data set from table 4 in [11] i.e $A_3^+ = 9.1 \times 10^{-3}$, $A_2^+ = 4.6 \times 10^{-3}$ and $\tau_y = 48\text{ms}$, we can obtain from equation (27) for the case of single-pulsed V_d waveform $\Delta V_d^s(\Delta t_2) \approx 0.24\text{V}$ for the case of $\Delta t_2 = 10\text{ms}$ and $\Delta V_d^s(\Delta t_2) \approx 0.21\text{V}$ for $\Delta t_2 = 20\text{ms}$. Similarly, for the case of double-pulsed V_d waveform, we can obtain from equation (28); $\Delta V_d^d(\Delta t_2) \approx 0.12\text{V}$ for the case of $\Delta t_2 = 10\text{ms}$ and $\Delta V_d^d(\Delta t_2) = 66\text{mV}$ for $\Delta t_2 = 20\text{ms}$. The definitions of $(\Delta t_1$ and $\Delta t_2)$ here are similar to [22] and are different compared to the notations given in [11]. For clarity, the difference is shown in Fig. 4(c). As an example, the data points chosen in protocol 2 are given by $(\Delta t_1/r, \Delta t_2/r)$ where $(\Delta t_1, \Delta t_2) \Rightarrow (-5, 5)$, $(-10, 10)$, $(-5, 15)$ and $(-15, 5)$ ms corresponds respectively to data points in [11].

2) Frequency effects of pairing protocol:

In [11], Δt used for the case of frequency effects is 10ms which is halved to 5ms for obtaining the measurement results in this paper. Also, ρ Hz mentioned in frequency effects of pairing protocol results of [11] will be equal to $r \times \rho$ Hz in our measurement results.

3) Quadruplet experiments:

Quadruplet experiments contain two temporal variables Δt and T as shown in Fig. 4(d). $\Delta t = 5\text{ms}$ in [11]—hence, we have used $\Delta t = 2.5\text{ms}$ for measurements. Then the chip measurement values for quadruplets are taken for different values of T/r up to 80ms. For comparing these measurement results with mathematical model, we simulated the mathematical model for double the value of T i.e up to 160ms.

IV. RESULTS

The measurement results shown in this section is obtained from a single FG synapse fabricated in TSMC $0.35\mu\text{m}$ CMOS process with $C_g = 5.5\text{pF}$. Though not optimized for synaptic density, the results here do serve as a proof of concept for our FG T-STDP implementation.

A. FG D-STDP learning window

The first set of testing on FG synapse is to check whether the FG T-STDP can reproduce D-STDP learning window. Fig. 5 shows the D-STDP learning window obtained from FG synapse. Thus for obtaining the result, we set $V_{d.min}$ as 0.3V

Fig. 5: FG D-STDP learning window: The curve shows learning window obtained from FG synapse using T-STDP rule. Here, $A_{fg}^+ \approx 0.26$, $A_{fg}^- \approx -0.15$, $\tau_{fg}^+ \approx 25\text{ms}$ and $\tau_{fg}^- \approx 22\text{ms}$

(here, $\Delta V_d(\Delta t_2) = 0$) w.r.t the mathematical analysis done in the section III-B and other voltage specifications are as given in Fig. 4(b) i.e $V_{dd} = 5.2\text{V}$, $V_{g.init} = 3.3\text{V}$, $V_{g.min} = 2.5\text{V}$, $T_g = 100\text{ms}$, $V_{tun.init} = 5.4\text{V}$, $V_{tun.max} = 16.5\text{V}$, $T_{tun} = 300\text{ms}$, $T_{tun.delay} = 1\text{ms}$, $T_{tun.pulse} = 2\text{ms}$, $V_{d.init} = 5\text{V}$ and $T_d = 500\mu\text{s}$.

B. Failure of FG D-STDP

We applied D-STDP rule on FG synapse to the pre- and post-synaptic spike pairs as done in [11]. For obtaining the measurement results in Fig. 6, we set the voltage and timing parameters as given in Fig. 4(b) i.e, same as mentioned in subsection IV-A.

1) *FG D-STDP fail to reproduce frequency effects:* For obtaining measurement results, we have set $\Delta t = \pm 5\text{ms}$ as shown in Fig. 4(d). The measurement results are plotted as weight change in D-STDP rule as a function of frequency, ρ . The measurement results (red lines) shown in Fig. 6(d), almost follows the mathematical D-STDP model (blue lines) in [11]. As mentioned in [11], this can be attributed to the following reasons. First, As pointed out in [32], at low repetition frequency, ρ , there is no potentiation. This cannot be captured by FG D-STDP, because pulsed drain voltage waveform, V_d at the occurrence of a post-synaptic spike after a pre-synaptic spike by few milliseconds induces LTP. Second, In experiments, for $\Delta t > 0$, potentiation increases when frequency increases. This trend can also not be reproduced by FG D-STDP. In D-STDP model, as soon as the frequency increases, the pre-post spike pairs approach each other and the post-synaptic spike of the first spike pair interact with the pre-synaptic spike of the subsequent spike pair. With increase in frequency, the post-pre spike interaction increases and therefore depress the synapse, which is not observed in experiments.

2) *FG D-STDP fail to reproduce triplet experiments:* In triplet experiments, as shown in Fig. 6(a) and (b), there is a clear asymmetry between two protocols mentioned (black bars). 60 repetitions of pre-post-pre triplet yields less weight change, whereas 60 repetitions of post-pre-post triplet yields a weight change of $\sim 30\%$ (black bars). However, FG D-STDP shown in red bars, predicts almost same result for both protocols, because the mechanism of potentiation and depression happening due to the generation of different voltage

Fig. 6: Failure of FG D-STDP: In all four subgraphs, black bars denote experimental data (taken from [11]), blue bars and lines, mentioned as D-STDP correspond to mathematical model proposed in [11] and red lines correspond to measurement results. (a) The bar graphs shows the comparison of results obtained from FG D-STDP (red) with the biological experimental results (black) and mathematical model (blue) for two cases of triplets, case 1: Pre-Post-Pre ($|\Delta t_1|/r, \Delta t_3/r$) and (b) case 2: Post-Pre-Post ($\Delta t_1/r, \Delta t_2/r$). FG D-STDP model (red bars) cannot replicate the experimental results shown in black bars. (c) FG D-STDP fails to reproduce quadruplet experiments. (d) Weight change in FG D-STDP rule as a function of frequency, $r \times \rho$. Note that, thick line correspond to $\Delta t = 5\text{ms}$ and dash line correspond to $\Delta t = -5\text{ms}$.

waveforms at pre- or post-synaptic spikes are similar in both protocols. Therefore, triplet results cannot be explained by a sum of pre-post injection mechanism and a post-pre tunneling mechanism.

3) FG D-STDP fail to reproduce quadruplet experiments:

The asymmetry present in the quadruplet experiments, as shown in Fig. 6(c), also causes some problem for FG D-STDP. A quadruplet consists of a pre-post-post-pre sequence where, $T < 0$ or a post-pre-pre-post sequence where, $T > 0$ as shown in Fig. 4(d). Here, $|T|$ denotes the interval between the first and last pair of spikes within the quadruplet. Sequence, pre-post-post-pre consists of two pre-post interactions and a post-pre interaction whereas; for the sequence, post-pre-pre-post, the opposite occurs i.e two post-pre interactions and only one pre-post interaction. This clearly leads to an asymmetry which is not seen in experiments [11].

C. Success of FG T-STDP

FG T-STDP is implemented with the help of a drain voltage waveform generator, explained in next section V. As mentioned in the previous section III-B, the mathematical analysis provides an intuitive understanding of utilization of V_d pulse waveform to obtain the extra triplet term in the T-STDP rule (equation (2)). As the extra triplet term can be achieved with the two cases of proposed pulse drain voltage waveform, here, we have shown measurement results for both the cases of V_d waveform. The measurement results obtained for both the case of drain voltage waveform satisfy the behavior seen

in experimental results [11]. The timing specifications for frequency effects of pairing protocol, triplets of spike and quadruplets are shown in Fig. 4(c) and (d).

1) *FG T-STDP can reproduce triplet and quadruplet experiments:* T-STDP model on floating gate synapse does not only reproduce the learning window (Fig. 5), but also it can reproduce most of the triplet and quadruplet experiments as shown in Fig. 7(a),(b) and (c) and Fig. 8(a),(b) and (c). The voltage and timing parameters for the case of single-pulsed drain voltage waveform are given in Fig. 4(b) i.e, same as mentioned in subsection IV-A. Here, $V_{d,min} = 0.3\text{V}$ is set with respect to $\Delta V_d(\Delta t_2)$ value (equation (27)), for parameters of Nearest-Spike minimal model, hippocampal culture data set, from table 4 in [11] i.e $A_3^+ = 9.1 \times 10^{-3}$, $A_2^+ = 4.6 \times 10^{-3}$ and $\tau_y = 48\text{ms}$. For the case of double-pulsed drain voltage waveform, voltage and timing parameters are also same as in the case of single pulse but, $\Delta V_d(\Delta t_2)$ is calculated using equation (28). In the triplet measurement results the red bars can almost capture the experimental black bars i.e more potentiation in the case of protocol 1 and less potentiation in the case of protocol 2. The blue bars shows the result of the mathematical model in [11]. The quadruplet measurement results also replicate the symmetry seen in the experimental results [11].

2) *FG T-STDP model can reproduce frequency effects:* FG T-STDP shown in red lines in Fig. 7(d) and Fig. 8(d) ameliorated the results obtained with FG D-STDP (Fig. 6(d)). The trend of increase in potentiation with frequency is seen for both cases of pulse drain voltage waveform: single and

Fig. 7: FG T-STDP using single-pulsed drain waveform: In all four subgraphs, black bars denote experimental data (taken from [11]), blue bars and lines, mentioned as T-STDP correspond to Nearest-Spike minimal triplet model proposed in [11] and red lines correspond to measurement results. (a) The bar graphs shows the comparison of results obtained from FG T-STDP (red) with the biological experimental results (black) and mathematical model (blue) for T-STDP protocol 1:Pre-Post-Pre ($|\Delta t_1|/r, \Delta t_3/r$). Similar to (a), results for T-STDP protocol 2:Post-Pre-Post ($\Delta t_1/r, \Delta t_2/r$) is shown in (b). FG T-STDP (red bars) can replicate the experimental results shown in black bars. (c) FG T-STDP can also reproduce quadruplet experiments. (d) Weight change in T-STDP rule as a function of frequency, $r \times \rho$. FG T-STDP can reproduce frequency effects compared to FG D-STDP. Note that, thick line correspond to $\Delta t = 5$ ms and dash line correspond to $\Delta t = -5$ ms.

Fig. 8: FG T-STDP using double-pulsed drain waveform: In all four subgraphs, black bars denote experimental data (taken from [11]), blue bars and lines, mentioned as T-STDP correspond to Nearest-Spike minimal triplet model proposed in [11] and red lines correspond to measurement results. (a) The bar graphs shows the comparison of results obtained from FG T-STDP (red) with the biological experimental results (black) and mathematical model (blue) for T-STDP protocol 1:Pre-Post-Pre ($|\Delta t_1|/r, \Delta t_3/r$). Similar to (a), results for T-STDP protocol 2:Post-Pre-Post ($\Delta t_1/r, \Delta t_2/r$) is shown in (b). FG T-STDP (red bars) can replicate the experimental results shown in black bars. (c) FG T-STDP can also reproduce quadruplet experiments. (d) Weight change in T-STDP rule as a function of frequency, $r \times \rho$. FG T-STDP can reproduce frequency effects compared to FG D-STDP. Note that, thick line correspond to $\Delta t = 5$ ms and dash line correspond to $\Delta t = -5$ ms.

double pulse. The voltage and timing parameters for the case of single-pulsed drain voltage waveform are also same as mentioned in subsection IV-A but, with a difference of $V_{d,min} = 0.5V$ instead of $0.3V$. $V_{d,min}$ is set with respect to the $\Delta V_d(\Delta t_2)$ value, (equation (27)), for parameters of $A_3^+ = 28.7 \times 10^{-3}$, $A_2^+ = 4.6 \times 10^{-3}$ and $\tau_y = 48ms$. Note that, we have used $A_3^+ = 28.7 \times 10^{-3}$, which is almost thrice compared to $A_3^+ = 9.1 \times 10^{-3}$ of the hippocampal culture data set, to ensure more potentiation with increase in frequency. Also note that, the measurement results for frequency effect of pairing protocol is obtained with the help of hippocampal culture data set instead of visual cortex data set mentioned in [11]. Again, for the case of double-pulsed drain voltage waveform, voltage and timing parameters are same as in the case of single pulse but, $\Delta V_d(\Delta t_2)$ is calculated using equation (28), for parameters of $A_3^+ = 28.7 \times 10^{-3}$, $A_2^+ = 4.6 \times 10^{-3}$ and $\tau_y = 48ms$. As in [11], here also we have a limitation i.e the absence of potentiation at low frequency is not observed in the measurement results in the case of single-pulsed and double-pulsed drain waveform (Fig. 7(d) and Fig. 8(d)). This is because the single pulse at the first post-synaptic spike itself is enough to generate some injection.

V. DRAIN VOLTAGE GENERATOR: VLSI IMPLEMENTATION

The drain voltage waveform generator is the important block for generating the voltage pulses according to spike timing as shown in Fig. 3. The input to the generator is a post-synaptic pulse from a neuron as shown in Fig. 11. The output pulse from the generator is fed back to the drain terminal of FG synapse. The number of drain waveform generators in a system depend on the number of neurons present in that neural network architecture. We propose circuits for single- and double-pulsed drain voltage waveform generator below along with their SPICE simulation results.

A. VLSI implementation of single-pulsed drain voltage waveform

From equation (27), we need to create an exponentially decaying voltage trace for $\Delta V_d^s(\Delta t_2)$ for large values of Δt_2 . Also, $V_{d,min}$ is the default value of V_d when there is no post synaptic pulse for a long time ($\Delta t_2 \rightarrow \infty$). In order to create the exponential voltage trace, we can use a capacitor, C and a switched capacitor resistor, R_{sc} , where the capacitor charges from the lowest voltage, $V_{d,min} - \Delta V_{dmax}$ to $V_{d,min}$ through the resistor (Fig. 9(a)). Here, ΔV_{dmax} is given by the equation (27), where $\Delta t_2 \rightarrow 0$. The operation of the circuit is as follows: at every post-synaptic pulse denoted as CLK in Fig. 9(a), the voltage across the capacitor V_c^s is sampled as V_d through the multiplexer. At other times, the multiplexer enforces $V_d = V_{d,init}$. A delayed pulse CLK_d is also generated after the clock pulse such that it does not overlap with CLK . At this pulse, V_c^s is pulled down to $V_{d,min} - \Delta V_{dmax}$. After this, V_c^s decays back to $V_{d,min}$ by discharging through the resistor R_{sc} . The decay constant of this circuit is set by the parameter τ_y in the equation (27).

Fig. 9: VLSI implementations: Circuit implementation of (a) single-pulsed drain voltage waveform and (b) double-pulsed drain voltage waveform.

Thus, the resistance of switched capacitor and capacitance, C are designed as $R_{sc} C = \tau_y$.

The simulation result of $\Delta V_d^s(\Delta t_2)$ obtained from the VLSI circuit is shown in Fig. 10(a) with comparison to the ideal theoretical plots. For simulation results, we have used $C = 1pF$, $V_{d,min} = 0.3V$, $V_{d,init} = 5V$ and $V_{d,min} - \Delta V_{dmax} = 25mV$ for $A_3^+ = 9.1 \times 10^{-3}$ and $A_2^+ = 4.6 \times 10^{-3}$. For designing switched capacitor resistor, R_{sc} we have:

$$\begin{aligned} R_{sc} &= \frac{T_{sc}}{C_{sc}} \\ R_{sc} C &= \tau_y \\ \Rightarrow \frac{C}{C_{sc}} &= \frac{\tau_y}{T_{sc}} \end{aligned} \quad (31)$$

Here, C_{sc} is the switched capacitor and $1/T_{sc}$ is the frequency of non overlapping clocks used in switched capacitor. T_{sc} is limited by the desired time resolution for Δt_2 , which is around 2ms. Thus, $C/C_{sc} = 24$ and $C_{sc} \approx 42fF$ for $\tau_y = 48ms$. It can be seen that the circuit simulation does not exactly match the theory for moderate values of Δt_2 due to our approximation of equation (27) by an exponential.

B. VLSI implementation of double-pulsed drain voltage waveform

Fig. 9(b) shows the circuit implementation of double-pulsed drain voltage waveform according to equations (28) and (19). The circuit operation is exactly similar to single pulsed drain waveform generator except that $\Delta V_d^d(\Delta t_2)$ is linearly dependent on Δt_2 . Hence, the resistor is replaced with a current source, I_p . Since, we need to create double pulse, an extra clock is used here. $CLK1$ is to create the first pulse, during which $V_d = V_{d,min}$ and $CLK2$ is to sample the voltage, V_c^d across capacitor, C on to the output node, V_d in order to create

Fig. 10: SPICE Simulation results: (a) The simulation result of the single-pulsed drain voltage waveform circuit. The result shows the variation of $\Delta V_d^s(\Delta t_2)$ with respect to Δt_2 . The ideal MatLab simulation result is also included for comparison. (d) The simulation result of the double-pulsed drain voltage waveform circuit.

the second pulse. Whenever there is no post-synaptic spike, V_d is held at $V_{d,init}$ through the switch controlled by NOR of CLK1 and CLK2. For deciding the value of I_p ; simplifying equation (28), we get:

$$\Delta V_d^d(\Delta t_2) = V_{inj} \ln\left(\frac{A_3^+}{A_2^+}\right) - V_{inj} \frac{\Delta t_2}{\tau_y} \quad (32)$$

also from capacitor charging,

$$C \frac{dV}{dt} = I_p \quad (33)$$

Thus equating both the slopes of equations (32) and (33), we get:

$$\frac{I_p}{C} = - \frac{V_{inj}}{\tau_y} \quad (34)$$

Hence, $I_p = -5.2$ pA for $\tau_y = 48$ ms and $V_{inj} = 0.25$ V. The simulation result of $\Delta V_d^d(\Delta t_2)$ obtained from the VLSI circuit is shown in Fig. 10(b) with comparison to the ideal MATLAB plots. For simulation results, we have used $C = 1$ pF, $V_{d,min} = 0.3$ V, $V_{d,init} = 5$ V and $V_{d,min} - \Delta V_{d,max} = 125$ mV for $A_3^+ = 9.1 \times 10^{-3}$ and $A_2^+ = 4.6 \times 10^{-3}$. It is easily seen that there is a much better match between the circuit and MATLAB simulation in this case due to the simpler functional form of ΔV_d^d .

VI. DISCUSSION

An important consideration for synapse designs is scalability to large arrays. Figure 11 shows the system level architecture of a neuromorphic hardware device with N neurons, M inputs and $M \times N$ synapses (number of synapses outnumbered compared to number of neurons). It shows the connection

Fig. 11: System level architecture: The system level implementation of a network with $M \times N$ synapses and N neurons.

between FG synapses and neurons and gives an idea about the number of different voltage waveform generators to be used for generating the terminal voltages for the FG synapse shown in Fig. 3. Here, for the entire system shown, we need only N drain voltage, N tunnel voltage and M gate voltage waveform generators. Thus the synaptic area overhead compared to earlier implementations [23] is only the added multiplexer for switching tunneling voltages.

Table I compares this work with other reported implementations of plastic synapses—a detailed review of these circuits can be found in [37]. It can be seen that our work is the first that combines high resolution non-volatile storage with sophisticated plasticity rules. The term normalized area is used to denote the ratio of the synapse area to the square of the process technology. It is a normalized metric to compare the size of a synapse circuit independent of process technology—smaller numbers refer to more compact designs. The floating-gate device used in our test chip is quite large. However, this is not a fundamental problem since we have earlier demonstrated STDP in much smaller floating-gate devices [23]—the only difference of this work with our earlier one is in terms of peripheral circuits to control drain and tunnel waveforms. Hence, after this proof of concept work, we can make a dedicated chip with floating-gates occupying $\approx 100 \mu m^2$ area. Some emerging devices like memristors are also showing promise as a compact learning synapse [38] for spiking systems. Though we are not yet aware of reports of dense arrays of memristive STDP synapses integrated with CMOS neurons in hardware, this seems like a promising area in future when scaling of flash memory or floating gates become limited.

One of the important aspects of a circuit implementation of a learning rule is the ease with which its parameters can be tuned. We showed in Section III-B how the parameter A_3^+ can be tuned based on ΔV_d . Other learning rule parameters are also directly related to parameters of the control voltage waveforms. For example, τ_+ can be modified using T_g , τ_-

TABLE I: Comparison of Learning Synapses in VLSI

Reference	Process technology (nm)	Synapse area (μm^2)	Normalized Area ^a	Weight storage (precision)	Plasticity rule	Chip measurement
This paper	350	6337	51730	Floating gate (> 10 bits)	T-STDP	Yes
[22]	350	-	-	Capacitor (Analog)	T-STDP	No
[23]	350	133	1088	Floating gate (> 10 bits)	STDP	Yes
[34]	350	400	3265	Capacitor (Analog)	STDP	Yes
[30]	350	100	816	Floating gate (> 10 bits)	STDP	Yes
[35]	250	5000	80000	Capacitor (Analog)	STDP	Yes
[20]	600	72000	200000	Capacitor (Analog)	STDP	Yes
[18]	800	4495	7023	Capacitor (bistable)	STDP	Yes
[17]	250	238	3810	SRAM (1 bit)	STDP	Yes
[36]	180	108	3338	SRAM (4 bits)	STDP	Yes
[10]	350	3000	24490	Capacitor (bistable)	SDSP	Yes

^aNormalized area is termed as the ratio of the synapse area to the square of the minimum transistor dimension in that process technology.

using T_{tun} and A_2^- using T_{tun_pulse} and V_{tun_max} . This is evident from the mathematical analysis of section III. Similarly, from equation (27) and equation (28), A_2^+ , A_3^+ and τ_y can be tuned using ΔV_d^s or ΔV_d^d , keeping two of them constant at a time. Some results for the variation of learning window to different parameters can be seen in our previous paper [26]. Also, other minor changes to the learning rule can be done by modifying the circuits at the neuron and periphery that generate the gate, drain and tunnel waveforms.

After this proof of concept, we will continue the work by simulating a spiking neural network (SNN) using SPICE simulations to understand the difference between T-STDP and D-STDP learning rules and then extend our work in future by fabricating chips with thousands of neurons and millions of learning synapses to do tasks like rapid and robust pattern recognition [39], [40]. Such neuromorphic chips that incorporate noise and heterogeneity are useful to understand the principles used by our brain to compute using imprecise elements [41], [42] as well as for accelerated simulations of neural networks [43], [44]. Moreover, we hope to use neuromorphic systems as the “brain” for real-time behaving systems like robots [41] where both low-power dissipation and real-time operation are necessary. In these cases, using a traditional computer for the implementation is inefficient due to the mismatch between Von-Neumann computing model of digital computers and the massively parallel analog computing of the brain where memory and computing are closely intermixed [45]. Hence, it is useful to be able to mimic biological neural networks closely in circuits to enable experimental paradigms as well as low-power intelligence.

VII. CONCLUSION

We have presented a spike triplet based learning rule using a single FG transistor as the synapse for VLSI spiking neural networks. The spike triplet affects the setting of drain voltage—we presented a single pulse and a double pulse drain voltage method to obtain the desired dependence of weight on spike timing. We presented a method to calculate the parameters of the drain voltage pulse to obtain results matched to the original theoretical T-STDP rule. We also show FG measurement results in comparison with the biological experimental observations for (1) original doublet protocol, (2) two protocols of spike triplets, (3) frequency effects of

pairing protocol and (4) quadruplet experiments. The failure of FG D-STDP rule in replicating the biological results is also included. Possible hardware implementations of drain voltage waveform generator are also proposed and verified through SPICE simulation results. It was shown that the voltage waveform for double pulse case can be generated more accurately due to its simplistic nature.

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REFERENCES

- [1] H. Markram, J. L'ubke, M. Frotscher, and B. Sakmann, “Regulation of synaptic efficacy by coincidence of postsynaptic APs and EPSPs,” *Science*, vol. 275, no. 5297, pp. 213–215, 1997.
- [2] G.-Q. Bi and M.-M. Poo, “Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type,” *The Journal of Neuroscience*, vol. 18, no. 24, pp. 10464–10472, Dec. 1998.
- [3] L. Zhang, H. Tao, C. Holt, W. Harris, and M. M. Poo, “A critical window for cooperation and competition among developing retinotectal synapses,” *Nature neuroscience*, vol. 395, pp. 37–44, Sep. 1998.
- [4] L. F. Abbott and S. B. Nelson, “Synaptic plasticity: taming the beast,” *Nature neuroscience*, vol. 3, pp. 1178–1183, Nov. 2000.
- [5] G.-Q. Bi and H.-X. Wang, “Temporal asymmetry in spike timing-dependent synaptic plasticity,” *Physiology and Behavior*, vol. 77, pp. 551–555, 2002.
- [6] R. Froemke and Y. Dan, “Spike-timing-dependent synaptic modification induced by natural spike trains,” *Nature*, vol. 416, pp. 433–438, 2002.
- [7] H. Wang, R. Gerkin, D. Nauen, and G. Bi, “Coactivation and timing-dependent integration of synaptic potentiation and depression,” *Nature neuroscience*, vol. 8, pp. 187–193, 2005.
- [8] R. Froemke, I. Tsay, M. Raad, J. Long, and Y. Dan, “Contribution of individual spikes in burst-induced long-term synaptic modification,” *Journal of Neurophysiology*, vol. 95, no. 3, pp. 1620–1629, 2006.
- [9] J.J. Wade, L.J. McDaid, J.A. Santos, and H.M. Sayers, “SWAT: A Spiking Neural Network Training Algorithm for Classification Problems,” *IEEE Transactions on Neural Networks*, vol. 21, no. 11, pp. 1817–1830, Nov. 2010.
- [10] S. Mitra, S. Fusi, and G. Indiveri, “Real-time classification of complex patterns using spike-based learning in neuromorphic vlsi,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 3, no. 1, pp. 32–42, Feb. 2009.
- [11] J.-P. Pfister and W. Gerstner, “Triplets of spikes in a model of spike timing-dependent plasticity,” *The Journal of Neuroscience*, vol. 26, no. 38, pp. 9673–9682, Sep. 2006.
- [12] E. Bienenstock, L. Cooper, and P. Munro, “Theory for the development of neuron selectivity: orientation specificity and binocular interaction in visual cortex,” *Journal of Neuroscience*, vol. 2, no. 1, pp. 32–48, Jan. 1982.

- [13] E. Izhikevich and N. Desai, "Relating STDP to BCM," *Neural Computation*, vol. 15, no. 7, pp. 1511–1523, 2003.
- [14] J. Gjorgjieva, C. Clopath, J. Audet, and J.-P. Pfister, "A triplet spike-timing dependent plasticity model generalizes the Bienenstock-Cooper-Munro rule to higher-order spatiotemporal correlations," *Proceedings of the National Academy of Sciences*, vol. 108, no. 48, pp. 19383–19388, 2011.
- [15] C. Mayr and J. Partzsch, "Rate and pulse based plasticity governed by local synaptic state variables," *Frontiers in Computational Neuroscience*, vol. 2, no. 33, 2010.
- [16] J. Hasler and B. Marr, "Finding a roadmap to achieve large neuromorphic hardware systems," *Frontiers in neuroscience*, vol. 7, no. 00118, Sep. 2013.
- [17] J. Arthur and K. Boahen, "Synchrony in silicon: The gamma rhythm," *IEEE Transactions on Neural Networks*, vol. 18, no. 6, pp. 1815–1825, Nov. 2007.
- [18] G. Indiveri, E. Chicca, and R. Douglas, "A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity," *IEEE Transactions on Neural Networks*, vol. 17, no. 1, pp. 211–221, Jan. 2006.
- [19] J. Wijekoon and P. Dudek, "VLSI circuits implementing computational models of neocortical circuits," *Journal of Neuroscience Methods*, vol. 210, no. 1, pp. 93 – 109, Sep. 2012, Special Issue on Computational Neuroscience.
- [20] T. J. Koickal, A. Hamilton, T. S. Lim, J. A. Covington, J. W. Gardner, and T. C. Pearce, "Analog VLSI circuit implementation of an adaptive neuromorphic olfaction chip," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 1, pp. 60–73, Jan. 2007.
- [21] B. Linares-Barranco, T. Serrano-Gotarredona, A. L. Camuas-Mesa, A. J. Perez-Carrasco, C. Zamarreo-Ramos, and T. Masquelier, "On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex," *Frontiers in Neuroscience*, vol. 5, no. 26, 2011.
- [22] M. R. Azghadi, S. Al-Sarawi, D. Abbott, and N. Iannella, "A neuromorphic vlsi design for spike timing and rate based synaptic plasticity," *Neural Networks*, vol. 45, pp. 70–82, 2013.
- [23] S. Brink, S. Nease, P. Hasler, S. Ramakrishnan, R. Wunderlich, A. Basu, and B. Degnan, "A learning-enabled neuron array ic based upon transistor channel models of biological phenomenon," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 1, pp. 71–81, Feb. 2013.
- [24] M. Pankaala, M. Laiho, and P. Hasler, "Compact floating-gate learning array with STDP," in *Proceedings of the International Joint Conference on Neural Networks*, Atlanta, GA, Jun. 2009, pp. 2409–2415.
- [25] R. Gopalakrishnan and A. Basu, "Robust doublet STDP in a floating-gate synapse," in *Proceedings of the International Joint Conference on Neural Networks*, Beijing, China, Jul. 2014, pp. 4296–4301.
- [26] R. Gopalakrishnan and A. Basu, "On the Non-STDP Behavior and Its Remedy in a Floating-Gate Synapse," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 26, no. 99, pp. 2596–2601, Feb. 2015.
- [27] A. M. Haas, "Compact circuits and adaptation techniques for implementing adaptive neurons and synapses with spike timing dependent plasticity (STDP)," *Patent US20090292661*, Nov. 26, 2009.
- [28] S.-C. Liu and R. Mockel, "Temporally learning floating-gate VLSI synapses," in *Proceedings of the International Symposium on Circuits and Systems*, Seattle, WA, May. 2008, pp. 2154–57.
- [29] A.W. Smith, L.J. McDaid, and S. Hall, "A compact spike-timing-dependent-plasticity circuit for floating gate weight implementation," *Neurocomputing*, vol. 124, pp. 210 – 217, 2014.
- [30] S. Ramakrishnan, P. Hasler, and C. Gordon., "Floating gate synapses with spike-time-dependent plasticity," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 3, pp. 244–252, Jun. 2011.
- [31] R. Gopalakrishnan and A. Basu, "Triplet spike time dependent plasticity in a floating-gate synapse," in *Proceedings of the International Symposium on Circuits and Systems*, Lisbon, Portugal, May. 2015, pp. 710–713.
- [32] P. Sjostrom, G. Turrigiano, and S. Nelson, "Rate, timing, and cooperativity jointly determine cortical synaptic plasticity," *Neuron*, vol. 32, no. 6, pp. 1149–1164, Dec. 2001.
- [33] P. Hasler, A. Basu, and S. Koziol, "Above threshold pfet injection modeling intended for programming floating-gate systems," in *Proceedings of the International Symposium on Circuits and Systems*, New Orleans, LA, USA, May. 2007, pp. 1557–1560.
- [34] S.A. Bamford, A.F. Murray, and D.J. Willshaw, "Spike-timing-dependent plasticity with weight dependence evoked from physical constraints," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, no. 4, pp. 385–398, Aug. 2012.
- [35] H. Tanaka, T. Morie, and K. Aihara, "A CMOS spiking neural network circuit with symmetric/asymmetric STDP function," *IEICE Transactions on Fundamentals of Electronics Communications and Computer Sciences*, vol. E92-A, no. 7, pp. 1690–1698, Jul. 2009.
- [36] J. Schemmel, A. Grubl, K. Meier, and E. Mueller, "Implementing synaptic plasticity in a VLSI spiking neural network model," in *Proceedings of the International Joint Conference on Neural Networks*, Vancouver, BC, Jul. 2006, pp. 1–6.
- [37] M.R. Azghadi, N. Iannella, S.F. Al-Sarawi, G. Indiveri, and D. Abbott, "Spike-based synaptic plasticity in silicon: Design, implementation, application, and challenges," *Proceedings of the IEEE*, vol. 102, no. 5, pp. 717–737, May. 2014.
- [38] Z.Q. Wang, H.Y. Xu, X.H. Li, H. Yu, Y.C. Liu, and X.J. Zhu, "Synaptic learning and memory functions achieved using oxygen ion migration/diffusion in an amorphous ingazno memristor," *Advanced Functional Materials*, vol. 22, no. 13, pp. 2759–2765, 2012.
- [39] J. Hu, H. Tang, K.C. Tan, H. Li, and L. Shi, "A spike-timing-based integrated model for pattern recognition," *Neural Computation*, vol. 25, no. 2, pp. 450–472, Feb. 2013.
- [40] Y. Qiang, H. Tang, K.C. Tan, and H. Li, "Rapid feedforward computation by temporal encoding and learning with spiking neurons," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 24, no. 10, pp. 1539–1552, Oct. 2013.
- [41] E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri, "Neuromorphic Electronic Circuits for Building Autonomous Cognitive Systems," *Proceedings of the IEEE*, vol. 102, no. 9, pp. 1367–1387, Sep. 2014.
- [42] B. V. Benjamin, P. Gao, E. McQuinn, S. Choudhary, A. R. Chandrasekaran, J.-M. Bussat, R. Alvarez-Icaza, J. V. Arthur, P. A. Merolla, and K. Boahen, "Neurogrid: A mixed-analog-digital multichip system for large-scale neural simulations," *Proceedings of the IEEE*, vol. 48, no. 8, pp. 1943–1953, Aug. 2014.
- [43] J. Wijekoon and P. Dudek, "VLSI circuits implementing computational models of neocortical circuits," *Journal of Neuroscience Methods*, vol. 210, no. 1, pp. 93–109, 2012.
- [44] E. Painkras, L. A. Plana, J. Garside, S. Temple, F. Galluppi, C. Patterson, D. R. Lester, A. D. Brown, and S. B. Furber, "Spinnaker: A 1-w 18-core system-on-chip for massively-parallel neural network simulation," *IEEE Journal of Solid-State Circuits*, vol. 102, no. 5, pp. 699–716, Apr. 2013.
- [45] C. Mead, "Neuromorphic electronic systems," *Proceedings of the IEEE*, vol. 78, pp. 1629–1636, Oct. 1990.