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High Performance Low Overhead Template-based Cell-Interleave Pipeline (TCIP) for Asynchronous-Logic QDI Circuits

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Abstract—We propose a novel Template-based Cell-Interleave Pipeline (TCIP) approach for generating high performance and yet low overhead asynchronous-logic (async) quasi-delay-insensitive (QDI) circuits. Our TCIP approach exploits the characteristics of the four prevalent QDI cell templates, namely Weak-Conditioned Half-Buffer (WCHB), Pre-Charged Half-Buffer (PCHB), Autonomous Signal-Validity Half-Buffer (ASVHB), and Sense-Amplifier Half-Buffer (SAHB), and then strategically interleave these template cells to form a composite pipeline. There are three main features in our TCIP approach. First, all QDI cell templates are first standardized with the same interface signals, and their corresponding cells are characterized in terms of transistor count, cycle time and energy dissipation for ease of comparison/selection/replacement. Second, our TCIP approach prioritizes the speed requirement when forming the initial pipeline circuits, and then subsequently reduces circuit overheads by interleaving various template cells without compromising the speed significantly. Third, the final optimized QDI pipeline circuit inherently features high robustness against process-voltage-temperature (PVT) variations, hence suitable for dynamic-voltage-scaling (DVS) operation. By means of 65nm CMOS process, we demonstrate a 4-bit pipeline tree adder based on the proposed TCIP approach, and benchmark it against the WCHB, PCHB, ASVHB and SAHB counterparts. These five designs feature same high operational robustness, nonetheless the design based on our TCIP approach is more competitive. Particularly, the designs based on reported approaches are, on average, $\sim 1.22\times$ more transistor count, $\sim 1.21\times$ slower and $\sim 1.22\times$ higher energy dissipation. Furthermore, under DVS operation from 1.2V to 0.3V, our proposed TCIP adder can reduce up to 88% energy for non-speed critical applications.

I. INTRODUCTION

Recent advancement of networking technologies enables numerous emerging applications, e.g. network-on-chip based multiprocessors implemented using advanced nano-scaled fabrication processes. However, as the feature size of fabrication processes continues to scale downwards, process-voltage-temperature (PVT) variations [1] become increasingly larger. Consequently, designing digital circuits based on the ubiquitous synchronous-logic (sync) approach [2], whose synchronization is based on a global clock or its variant, becomes increasingly challenging. The usual methods to accommodate the PVT variations include adopting a conservative clock rate (when the conditions are more benign), time-tolerant techniques, strict operating conditions, etc [3].

An alternative design approach for robust operation is the esoteric asynchronous-logic (async) approach [4]. Particularly, async quasi-delay-insensitive (QDI) circuits can tolerate arbitrary gate/wire delays (with isochronic fork assumption [5]), hence inherently accommodating PVT variations. This is

because the QDI circuits detect the computation delays according to different workloads/operating conditions. Nevertheless, the drawback of QDI is the increased hardware overhead, for example, due to its dual-rail modality [5], a near doubling of the hardware compared to the single-rail designs.

Besides dual-rail modality, another consideration for the async QDI circuits is the pipeline structure [6]. There are generally two pipeline structures, namely fine-grain gate-level and coarse-grain block-level structures. The coarse-grain block-level structure comprises multi-cascading cells into single block for every pipeline stage, hence suffering from long data propagation delay, and is not suitable for high speed applications. In contrast, the fine-grain gate-level structure embeds only one single cell for every pipeline stage, hence potentially featuring shorter delay. However, its drawback is higher circuit overhead due to the individual acknowledgement circuitry in each single pipeline cell.

In this paper, we propose a high performance and yet low overhead Template-based Cell-Interleave Pipeline (TCIP) approach by leveraging on four reported QDI cell templates, namely Weak-Conditioned Half-Buffer (WCHB) [7], Pre-Charged Half-Buffer (PCHB) [8], Autonomous Signal-Validity Half-Buffer (ASVHB) [9], and Sense-Amplifier Half-Buffer (SAHB) [10]. Our TCIP approach exploits the characteristics of these four prevalent QDI cell templates, and then strategically interleave these template cells to form a new composite pipeline which features high performance and yet low overhead attributes [11]. In our TCIP approach, we standardize the interfaces of various QDI templates, characterize their corresponding library cells (for comparison/selection/replacement), prioritize the speed requirement, replace low overhead cells in non-critical paths (without significantly affecting speed), and maintain QDI protocol to accommodate PVT variations. To demonstrate the advantages of our proposed TCIP approach, we design a 4-bit pipeline tree adder (@ 65nm CMOS), and benchmark it against the WCHB, PCHB, ASVHB and SAHB counterparts. The tree adder based on our TCIP approach is highly competitive in terms of overall transistor-count, speed and energy dissipation. Particularly, the reported counterparts are, on average, $\sim 1.22\times$ more transistor count, $\sim 1.21\times$ slower and $\sim 1.22\times$ higher energy dissipation than the design based on our TCIP approach. Our proposed TCIP adder is functional from 1.2V to 0.3V, appropriate for dynamic-voltage-scaling (DVS) operation.

This paper is organized as follows. Section II presents the proposed TCIP approach. Section III presents simulation results of our adder based on the TCIP approach and finally, conclusions are drawn in Section IV.

II. PROPOSED TCIP APPROACH

A. Standardization of Interface Signals

Our proposed TCIP approach leverages on four reported QDI cell templates, namely WCHB [7], PCHB [8], ASVHB [9] and SAHB [10]. However, their interface signals are not exactly the same. Hence, we standardize the interface signals of the four templates to ease the cell-interleaving process in the proposed TCIP design flow. Fig. 1 depicts the standard model of async QDI cell-level block, accompanied by the standardized interface signals, comprising input signal *Data-In*, output signal *Data-Out*, acknowledge handshake signal *Lack* to the preceding pipeline, and *Rack* from the succeeding pipeline.

Fig. 1: Standard Model of Async QDI Cell-level Block

Figs. 2(a) to (d) depict the buffer cells based on WCHB, PCHB, ASVHB, and SAHB respectively. The WCHB buffer cell demonstrates the basic building blocks of a QDI pipeline, consisting of an input completion detection (ICD), a functional block (FB), a latch and an output completion detection (OCD). The ICD validates the input completeness of *A.T/A.F*. The functional block evaluates/resets the validated data. The latch propagates the evaluated data when *Rack* is asserted, or reset *Q.T/Q.F* when *Rack* is de-asserted. The OCD validates the output completeness of *Q.T/Q.F* and assert/de-assert *Lack*.

The PCHB, ASVHB and SAHB cells have the same operational modality but with different implementations. The

PCHB cell uses the Differential Cascode Voltage Switch Logic to integrate the FB and the latch together. The ASVHB uses independent circuits to form the true-rail FB and the false-rail FB, making them as latched FB. The SAHB adopts an evaluation block and a sense-amplifier block to form the latched FB. In these designs, their ICD and OCD are modified accordingly.

Due to different implementations, the four QDI cell templates possess different characteristics, as tabulated in Table I. In overall, they abide by QDI protocol, eliminating timing assumptions and inherently accommodating PVT variations. Therefore they are suitable for full-range DVS operation. Besides, they are designed in fine-grain gate-level pipeline structure, hence are generally speed-efficient. Their differences are how different building blocks are integrated. WCHB requires ICD, OCD and external latch. PCHB only requires ICD and OCD. Both reported ASVHB and SAHB only requires OCD, but in this approach they require an additional ICD and an additional input buffer respectively, for standardization of interface signals.

TABLE I
CHARACTERISTICS OF VARIOUS QDI TEMPLATES

Characteristics	WCHB	PCHB	ASVHB	SAHB
Timing Approach	QDI			
PVT variations	Accommodating			
DVS	Full-range			
Pipeline Structure	Fine-grain Gate-level			
ICD	Required	Required	Required*	Not Required
OCD	Required	Required	Required	Required
Input Buffer	Not Required	Not Required	Not Required	Required*
External Latch	Required	Not Required	Not Required	Not Required

*for standardization of interface signals

Fig. 2: Pipeline Buffer Cell for QDI Approaches (a) WCHB, (b) PCHB, (c) ASVHB and (d) SAHB

B. Characterization of Library Cells

We further characterize the library cells based on the four QDI templates, for comparison/selection/replacement in the TCIP approach. The characterized library cells are 1-bit BUFFER, 2-bit AND/NAND, 2-bit XOR/XNOR and 3-bit AO/AOI. Table II tabulates the transistor count, cycle time and energy dissipation per operation for four library cells based on four QDI templates. Transistor count is the number of transistors to construct a library cell. Cycle time is the total delay for the library cell to complete a local cycle [5]. Cycle time constitutes to the operating speed of the async QDI pipeline. The operating speed is the total of worst case cycle time and delay of async “fork” nodes completion detection [5]. Energy dissipation per operation is the product of power dissipation and cycle time. Since the operating speed of async QDI pipeline is data dependent, we use energy dissipation, instead of power dissipation which depends on operating frequency, for characterization of library cells.

From table II, in term of transistor count, WCHB 1-bit BUFFER, SAHB 2-bit AND/NAND, ASVHB 2-bit XOR/XNOR and SAHB 3-bit AO/AOI form the lowest overhead combination. This shows that within the same QDI template, the number of transistors varies largely for different library cells, due to the circuit structure. Hence a QDI template may feature lower number of transistor in some library cells (but not all) compared to other QDI templates. In term of cycle time, all library cells generally feature high operating speed, whose cycle time is smaller than 1ns, except WCHB 3-bit AO/AOI (cycle time = 1.02ns). This is because all the library cells are designed in fine-grain pipeline structure, hence are speed-efficient in nature. In term of energy dissipation, WCHB features the lowest amongst four templates for four library cells, due to smaller number of transistor switchings. In contrast, PCHB dissipates the highest energy dissipation, due to the dynamic power dissipated from DCVSL circuit structure (with state-holding feedback inverters).

C. Proposed TCIP Design Flow

We will now describe our proposed TCIP design flow to strategically interleave the characterized template cells to form a new composite pipeline which features high performance and yet low overhead attributes. Fig. 3 depicts the TCIP design flow to generate an optimized async QDI TCIP circuit. First, from the behavioral Verilog coding, we run the synthesis to generate async pipeline architecture with cell-level blocks (standard model as depicted in Fig. 1). Second, we determine the operating speed requirement for our targeted application. Third, from the four QDI templates, we identify the library cells that are qualifying for the preset speed requirement. Fourth, we search those speed-qualifying library cells with the lowest overhead, amongst four QDI templates. Finally, in the pipeline architecture, we replace the cell-level blocks with our selected lowest overhead speed-qualifying library cells. After the library cells replacement, the final product from our design flow is the optimized async QDI TCIP circuit, which is also

operational robust and functional for DVS operation.

Fig. 3: Proposed TCIP Design Flow

III. SIMULATION RESULTS

We demonstrate the advantages of our proposed TCIP approach by constructing an adder circuit. Fig. 4 depicts the pipeline architecture of 4-bit Kogge-Stone tree adder (i.e. 4-bit pipeline adder). The 4-bit pipeline adder consists of 15 BUFFER cells, 6 AND/NAND cells, 8 XOR/XNOR cells, and 5 AO/AOI cells. Based on our proposed TCIP approach, we apply WCHB BUFFER, SAHB AND/NAND, ASVHB XOR/XNOR and SAHB AO/AOI to form the 4-bit adder (i.e. proposed TCIP adder).

Fig. 4: Architecture of 4-bit Pipeline Kogge-Stone Tree Adder

For fair comparison, we benchmark our proposed TCIP adder to the reported WCHB, PCHB, ASVHB and SAHB counterparts. Table III tabulates the normalized transistor count, cycle time and energy dissipation of the 4-bit pipeline adder using various approaches. From Table III, our proposed TCIP adder features the lowest transistor count. The other adders are on average $\sim 1.22\times$ more transistor count. This is due

TABLE II
CHARACTERIZATION OF LIBRARY CELLS BASED ON VARIOUS QDI APPROACHES @65NM CMOS, 1.2V

	Transistor Count				Cycle Time (ns)				Energy Dissipation per operation (fJ)			
	WCHB	PCHB	ASVHB	SAHB	WCHB	PCHB	ASVHB	SAHB	WCHB	PCHB	ASVHB	SAHB
1-bit BUFFER	32	46	38	42	0.41	0.59	0.51	0.50	14.5	36.2	20.8	28.6
2-bit AND/NAND	88	66	58	56	0.78	0.67	0.64	0.61	32	51.8	32.9	39.1
2-bit XOR/XNOR	92	68	60	70	0.76	0.72	0.66	0.74	30.6	53.4	33.8	51.1
3-bit AO/AOI	144	86	86	71	1.02	0.81	0.87	0.73	43.8	65.6	50.7	55.2

to the cell-interleave of library cells (from four QDI templates) with the lowest transistor count. Our proposed TCIP adder also features the highest speed. The other adders are on average $\sim 1.21\times$ slower. This is because the cell-interleave concept improves the worst-case delay in particular library cells from four QDI templates. Our proposed TCIP adder dissipates lower energy than the PCHB, ASVHB and SAHB counterparts due to the reduced number of transistor switchings, and large improvement of operating speed. Nonetheless, WCHB adder features insignificant $0.93\times$ lower energy advantage than ours. On average, the reported counterparts are $\sim 1.22\times$ higher energy dissipation than ours.

TABLE III

SIMULATION RESULTS OF 4-BIT PIPELINE ADDER BASED ON VARIOUS APPROACHES @65NM CMOS, 1.2V; NORMALIZED TO THE READINGS OF PROPOSED TCIP DESIGN

4-bit Pipeline Adder	Transistor Count	Cycle Time	Energy Dissp. per op.
WCHB	1.43×	1.43×	0.93×
PCHB	1.22×	1.19×	1.55×
ASVHB	1.09×	1.14×	1.05×
SAHB	1.12×	1.08×	1.34×
Proposed TCIP	1× (1,875)	1× (0.91ns)	1× (1063fJ)

Fig. 5 depicts the transistor count breakdown for various QDI templates in the proposed TCIP 4-bit adder. Since we apply WCHB BUFFER, SAHB AND/NAND, ASVHB XOR/XNOR and SAHB AO/AOI to achieve the lowest overhead design, the proposed TCIP adder consists of $\sim 37\%$ SAHB cells, $\sim 26\%$ ASVHB cells, $\sim 26\%$ WCHB cells and $\sim 11\%$ single-rail standard cells. Nonetheless, the distribution of the transistor breakdown for various QDI templates varies depending on the number of their respective library cells in the constructed architecture.

Fig. 6 depicts the DVS for the proposed TCIP adder from 1.2V to 0.3V. When the supply voltage is reduced, the energy dissipation decreases as the dynamic power dissipation decreases significantly. The minimum energy point occurs at 0.4V, in which the proposed TCIP adder can save $\sim 88\%$ energy when compared to the nominal operation at 1.2V. This low voltage low energy operation is suitable for those applications when the operating speed is not critical. From 0.4V to 0.3V, the energy dissipation increases slightly since the leakage power dominants within this region.

IV. CONCLUSIONS

We have proposed a novel TCIP design approach to generate an async QDI circuit with emphases on high performance and low overhead by cell-interleave optimization. The generated and optimized QDI circuit is inherently operational robust towards PVT variations. When demonstrated in 4-bit pipeline tree adder, our proposed TCIP design is better in terms of transistor count, speed and energy dissipation, than the WCHB, PCHB, ASVHB and SAHB counterparts. The reported counterparts are, on average, $\sim 1.22\times$ more transistor count, $\sim 1.21\times$ slower and $\sim 1.22\times$ higher energy dissipation than our proposed TCIP design. Under DVS operation, our proposed TCIP adder can reduce up to 88% energy dissipation from 1.2V to 0.3V.

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Fig. 5: Transistor Count Breakdown for Proposed TCIP Adder

Fig. 6: DVS (1.2V to 0.3V) for Proposed TCIP Adder

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