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Ultra-low Power High Efficient Rectifiers with 3T/4T Double-gate MOSFETs for RFID Applications

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Abstract— Recently, multi-gate MOSFETs such as double-gate MOSFETs have been identified as inevitable inclusion for future nano-scale circuit design. This paper explores the scope of tied-gate (3T), independent gate (4T), symmetric and asymmetric features of double-gate MOSFETs (DGMOSFETs) for ultra-low power and high efficient rectifiers for RFID applications. Various widely used rectifier topologies such as simple conventional rectifier, self- V_{th} cancellation (SVC) rectifier and differential drive rectifier etc, have been designed to investigate the better candidate for DGMOSFET technology. Analysis reveals that 3T differential drive rectifier topology shows the maximum power conversion efficiency (PCE) and higher DC output voltage level generation. Second part of the work further explores the effects of 3T/4T and symmetric/asymmetric features of DGMOSFETs on the performance of differential drive rectifier. Among the various DGMOSFET configurations for RFID rectifiers, symmetric tied-gate DGMOSFETs have the best power conversion efficiency and the lowest power consumption.

Key words— Double-gate MOSFETs, Ultra-low power, RFID rectifiers.

I. INTRODUCTION

Long-range passive microwave transponders (tags) for RFID systems do not have an on-board battery and therefore must draw the power required for their operation from the electromagnetic field transmitted by the reader. The main concern in designing the passive RFID tag is to consume as low power as possible. Decreasing the power consumption decreases the RF power needed from the reader and thus increases the operation range of the RFID tag. Rectifier circuits for the RFID tags are usually designed either by Schottky diodes [1][2] or CMOS transistors [3-7]. Schottky diode rectifiers generally achieve a better performance due to the small turn-on voltage of the diodes. However, Schottky diodes are not readily supported in all CMOS technologies and therefore are not suited for CMOS implementations [3]. On the other hand, in CMOS technology the voltage drop of a diode-connected transistor is about the threshold voltage (V_{th}) of the device. This voltage drop can be reduced either by including a fixed voltage source between the drain and gate of diode connected transistors to reduce their turn-on voltage (static V_{th} cancelation) [5][6] or in more advanced

technologies by using zero or low- V_{th} devices [7]. Both approaches increase the reverse leakage of transistors when the transistors must be turned off and thus reduce the efficiency of the rectifiers. In [3], a four-transistor-cell CMOS rectifier is proposed which outperforms CMOS diode-based rectifiers, even when static V_{th} -cancelation technique is used to reduce the turn-on voltage of the diodes. One drawback of the four transistor cell rectifier is that it does not perform well when the received RF power is weak (e.g, a few μ W).

Much of the work has been done on using CMOS front-ends and CMOS technology for RFID. Very few have considered double gate MOSFETs for ultra-low power RFID tag design. The usefulness of non-classical underlap channel architecture to enhance both gain and bandwidth of an OTA, alleviating gain-bandwidth trade-off associated with analog design, has been demonstrated in [8]. A. Kumar et al, [9] explores the application of independently driven double-gate MOSFETs for low-power low voltage analog integrated circuit design. In [10], P.Freitas et al, investigate new capabilities brought on by independently driven double gate CMOS transistors for analog baseband design. Since the gates are disconnected, the corresponding channels are coupled resulting in a dynamic threshold voltage tuning. This operation mode is exploited to create new analog functions and low-voltage circuits. A current mirror is redesigned using of independently driven double-gate MOSFETs and shown that this structure performs an efficient differential function relating to the potentials applied to the back gates. N. Mohankumar et al, study the influence of both channel and gate engineering on the analog and RF performances of double-gate MOSFETs for system-on-chip applications [11]. The gate engineering technique used here is the dual metal gate technology, and the channel engineering technique is the conventional halo doping process.

However, not many have explored the effect of various configurations of DGMOSFETs for ultra low power rectifier design for RFID applications. The rest of paper is organized as follows. Various DGMOSFET configurations and rectifier topologies implemented with 3T/4T DGMOSFETs are described in section II. Section III presents the simulation results and discussion on results. Finally, conclusions are presented in section IV.

II. THEORETICAL BACKGROUND

A. Various Double-gate MOSFET (DGMOSFET) Configurations

DGMOSFETs can have either a three-terminal (3T) configuration, where both the gates are shorted, or a four-terminal (4T) configuration, where the back-gate bias is fixed and the front gate acts as a control electrode. If the two gates in the DGMOSFETs are tied (3T), an identical voltage can be applied to both the gates. Conversely, when the two gates are independent (4T), different voltages can be applied.

The implementation of symmetry and asymmetry configurations in the DGMOSFETs can be realized in a number of ways. For example, it can be implemented by applying different gate voltages to the front and back gates, by assigning variations in oxide thickness at the front and back gates. An alternative way is varying gate material with different work functions. In this work, the asymmetric nature of the DGMOSFETs is brought by taking the variation in the gate oxide thickness for the front and back gates. The asymmetric feature of the DGMOSFETs offers more flexibility and freedom to circuit designers in the device control point of view.

In the following studies, we will primarily consider the four DGMOSFET structures that are shown in Fig. 1: 3T symmetric DGMOSFET (3TSDG) device ($V_{fg} = V_{bg} = V_{dd}$ and $T_{fox} = T_{box} = 1.4\text{nm}$), 3T asymmetric DGMOSFET (3TADG) device ($V_{fg} = V_{bg} = V_{dd}$ and $T_{fox} \neq T_{box}$), 4T symmetric DGMOSFET (4TSDG) device ($V_{fg} = V_{dd}$, $V_{bg} = 0$ and $T_{fox} = T_{box} = 1.4\text{nm}$), and 4T asymmetric DGMOSFET (4TADG) device ($V_{fg} = V_{dd}$, $V_{bg} = 0$ and $T_{fox} \neq T_{box}$).

Fig. 1. Schematic of various configurations of DGMOSFETs.

B. Various RFID Rectifier Topology Implementations with 3T/4T DGMOSFETs

As a RFID tag is a passive system, DC voltage must be generated to bias the circuits of the tag, which is done by a rectifier. The rectifier converts received RF signal into DC

voltage. The main challenge in designing the RFID rectifier is to generate the required DC power using the low voltage amplitude of the input RF signal with acceptable power conversion efficiency. Power conversion efficiency (PCE) of a rectifier is defined by the output power divided by the input power. The PCE of a rectifier circuit is affected by various parameters such as circuit topologies, diode-device parameters, input RF signal frequency and amplitude, and output loading conditions. Since the input RF signal of RFIDs in long-range operations is extremely small, low turn-on voltage is the most important factor for the diode devices. Schottky diodes have been extensively utilized in previous rectifiers with a multi-stage configuration, because of its low turn-on voltage. The rectifier circuit using the Schottky diode achieves a high PCE, but it is not compatible with conventional CMOS technology and requires costly fabrication processing.

Four different rectifier configurations with 3T and 4T DGMOSFETs are illustrated in Fig. 2. Fig. 2 (a) shows a simple rectifier circuit widely used in RFID implemented with 3T DGMOSFETs. Diode-connected n-channel and p-channel MOSFETs are connected in series and the internal node is connected to RF input terminal through the coupling capacitor (C_C). The PCE for a rectifier using a diode-connected MOSFET is generally worse than that of the Schottky diode based one due to its higher threshold voltage (V_{th}), but when V_{th} cancellation techniques are utilized, the PCE can be improved dramatically. In order to reduce the effective turn-on voltage for achieving larger PCE, several V_{th} cancellation schemes have been proposed [5][12-14]. One uses a switched-capacitor technique to generate DC gate bias voltage from an external power supply [12] and others generate DC gate bias voltage from the output voltage of the rectifiers themselves [5][13][14]. Fig. 2 (b) shows a self- V_{th} -cancellation (SVC) rectifier circuit implemented with 3T DGMOSFETs. It is the same as the conventional rectifier circuit described in Fig. 2 (a), except that the gate electrodes of the n-MOS transistor and p-MOS transistor are connected to the output terminal and the ground terminal, respectively. This connection boosts the gate-source voltages of the n-MOS and p-MOS transistors as much as the output DC voltage. In other words, the threshold voltages of MOS transistors are equivalently decreased by the same amount to the output DC voltage. However, it has been found that “static” V_{th} cancellation schemes have limitation in achieving small ON-resistance and small reverse leakage current at the same time. Differential drive rectifier is an “active” V_{th} cancellation scheme in which V_{th} can be minimized in a forward bias condition and be increased in a reverse bias condition automatically by a cross coupled differential circuit configuration [4]. Fig.2 (c) shows a unit stage of the differential-drive rectifier circuit with the 4T configuration of DGMOSFETs and Fig. 2 (d) shows the same circuit implemented with 3T configuration of DGMOSFETs. The circuits have a cross-coupled differential configuration with a bridge structure. The similar units can be cascaded to produce larger PCE and DC output voltage levels required by other functional blocks.

Fig. 2. Various rectifier configurations with DGMOSFETs.

III. RESULTS AND DISCUSSION

The various DGMOSFET rectifier topologies mentioned above are designed and simulated using HSPICE to analyze the best topology which suits for ultra low power RFID design with highest possible efficiency using DGMOSFET technology. The parameters of the passive devices are as follows: $C_C = C_S = 10\text{pf}$, $R_L = 10\text{k}\Omega$, and $f = 100\text{MHz}$. The W/L ratio for the minimum sized devices and the upsized devices are 2 and 10, respectively. Comparisons of the DC output voltages and the PCEs by the considered rectifier topologies implemented with the minimum sized 3T DGMOSFETs with variations in input RF levels are presented in Fig. 3. The simple and SVC rectifier topologies demonstrate similar output voltage levels, but the output voltage levels of them are substantially lower than that of the differential drive rectifier. As the RF input signal amplitude changes from 0.1V to 0.9V (for a power generation of 0.5-365 μW), the DC output power of the differential drive rectifier changes from 0.5 to 139 μW while that of the SVC rectifier changes from 1.6pW to 1 μW . As a result, larger power conversion efficiency values can be achieved from the differential drive rectifier as presented in Fig. 4. For the same changes in the input voltage levels, the PCEs is in the ranges of 42-38% for the differential rectifier, 0.04-2.1% for the SVC rectifier and 0.2-2.1% for the simple rectifier respectively.

The power consumption comparisons of the above rectifier topologies with minimum sized 3T DGMOSFETs are shown in Fig. 5. The differential rectifier consumes larger power than the simple and SVC rectifier topologies. Fig. 6 demonstrates the impact of sizing on the PCEs of the

Fig. 3. Comparison of DC output voltages in various rectifier topologies with minimum sized 3T DGMOSFETs sweeping RF input voltage.

Fig. 4. Comparison of PCE in various rectifier topologies with minimum sized 3T DGMOSFETs sweeping RF input voltage.

differential drive rectifier. Overall, 4T configuration has lower PCE than 3T configuration, but at very small RF input voltage levels, the 4T configuration shows higher PCE than the 3T one. Fig.7 shows the PCE comparisons of the differential drive rectifier implemented with the 3T/4T, symmetric/asymmetric features of the DGMOSFETs. Overall, the 3T structures have larger DC output levels and PCE than the 4T structure. The effect of the symmetric and asymmetric oxide thickness on the PCE is insignificant except at the input voltage of 0.1V where the asymmetric feature shows a larger PCE value.

Fig. 5. Comparison of power consumption in various rectifier topologies with minimum sized 3T DGMOSFETs sweeping RF input voltage.

Fig. 6. Comparison of PCE of the differential drive rectifier with minimum and up-sized 3T/4T DGMOSFETs sweeping RF input voltage.

Fig. 7. Comparison of PCE of the differential drive rectifier with 3T/4T and symmetric/asymmetric DGMOSFETs sweeping RF input voltage.

IV. CONCLUSIONS

Various rectifier topologies are explored with DGMOSFET technology to suggest a better candidate for the RFID design. The simulation results have shown that the differential drive rectifier with the minimum-sized 3T DGMOSFETs is the most promising candidate for ultra-low power and efficient RFID rectifier design due to the higher power conversion efficiency ranging from 38% to 42%. In the differential rectifier, the 3T rectifier topology generates higher PCE and DC output voltage than the 4T one. Finally, the asymmetric gate oxide thickness has negligible impact on PCE when the input voltage level is high. However, the PCE becomes sensitive to the configuration of the gate oxide thickness when the input voltage is low.

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