A 253mW/channel 4TX/4RX pulsed chirping phased-array radar TRX in 65nm CMOS for X-band synthetic-aperture radar imaging

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A 253mW/channel 4Tx/4Rx Pulsed Chirping Phased-Array Radar TRx in 65nm CMOS for X-band

Synthetic Aperture Radar Imaging

Airborne or spaceborne synthetic aperture radar (SAR) targeted for micro-unmanned aerial vehicle (UAV) or micro-satellite becomes capable of observing large area under all weather conditions with strong penetrations, and finds many emerging applications in defense, geology, urban, oceanography, agriculture and others etc. [1]. Phased-array SAR, operating in three modes of spotlight, stripmap and scanSAR, can significantly improve the spatial resolution and detection SNR by steering the beams to the targets. The existing SAR system is still constrained by power, size, and performance for payload in micro-UAVs/micro-satellites. It is presented to develop an X-band phased-array radar TRx IC to achieve the power of 253mW/channel, die size of 7.8mm² and resolution of <30cm.

Conventional radar systems are narrow band systems and beamforming is achieved using phase shifters. To achieve a wide band phased-array operation, a true time delay is required in each element [2]. In addition, there always exists the trade-off between large angle beamforming and achieving fine angle resolution. To solve above issues, a two-stage delay control with calibration is employed in the transmitter, where a DLL is used to control the coarse true time delay of the baseband chirp and a compact active phase shifter in RF path is used for fine delay tuning. As shown in Fig. 1, DLL based multi-phase synthesizer (MPS) generates the multiphase delayed clocks with precise delay control [2]. Then each clock will be used as a reference clock input to a corresponding direct digital synthesizer (DDS) in baseband chirp generation that then gets phase-reserved up-conversion to an RF wideband chirp by a PLL. By this way, a relative large time delay (tens of ps) in coarse steps between adjacent RF chirp signals can be obtained through the MPS, and fine time delay adjustment (< 1ps) is subsequently achieved with a 6-bit phase shifter. For the beamforming receiver, digital beamforming is a more flexible way to apply advanced algorithms. The receiver is capable to work in two modes: without or with stretch processing [3]. An external reference LO generator chip is developed for both processing. For the former mode, direct down-conversion is applied, and the down-converted IF signals will occupy the same bandwidth as the RF chirps, requiring at least

double of the bandwidth in ADC sampling; For the latter mode, a time of return (TOR) predictor with $<0.1\mu\text{s}$ delay resolution estimates the starting time of the LO chirps with the knowledge of the UAV/Satellite's altitude, and then activates the reference LO chirp of same slope rate as the RF chirp for compressing the signal bandwidth, significantly relaxing the requirement on the ADCs.

The paper presents a 4Tx/4Rx pulsed chirping phased-array TRx for SAR operating at X-band. As shown in Fig. 1, the MPS employing fractional DLLs and a Vernier delay matrix (VDM) [2] provides a maximum clock time delay up to 200ps with 20ps step for coarse delay tuning with jitter of 1.67ps RMS. It resorts to 174ps delay to achieve a maximum beamsteering angle of $\pm 60^\circ$ when antennas are separated by 2λ (6cm) pitch. A compact DDS is employed for tunable baseband chirp generation with frequency from 74.2 to 82.1MHz, chirp duration of 20 μs -1ms and pulse repetition rate of 1ms. The PLLs work as a closed-loop frequency multipliers to obtain 10GHz centred chirps up to 1GHz BW with a linearity of 183kHz-1.1MHz RMSE, which preserve the same relative true time delay between RF chirps as those of MPS outputs and govern a resolution of $<30\text{cm}$ for long range detection. An active phase shifter (PS) is used to attain the fine beamsteering resolution of 1° that requests 5.86° phase shift resolution translation to 1.67ps true time delay. The ripple at Tx output is minimized to $<2\text{dB}$ by employing a saturated power-amplifier (PA), and with the LNA of 0.2dB gain ripple in Rx, no significant paired echo is observed. The Rx baseband (RxBB) is employed after a mixer with interleaved filter and programmable gain amplifier (PGA) stages to improve the linearity to the IP1dB of -5dBm and suppress the antenna leakage and other IF interferences by $>60\text{dB}$.

Fig. 2 shows the key building block circuits. For the 400MHz fractional DLL, a 16-bit, 3rd-order $\Sigma\Delta$ modulator (DSM) selects the outputs of 4 adjacent voltage control delay cells (VCDCs) to form the required fractional delay that is mapped to the VDM to further generate four delayed clocks for the DDSs. The DDS mainly consists of a 20-bit frequency/phase accumulator based digital modulation core and a linear/nonlinear hybrid digital-to-analog convertor (DAC). It achieves 10-bit quarter wave resolution with a 4-bit coarse DAC and a 6-bit fine DAC using 1-bit to generate full sine wave. The PS, implemented as an I/Q vector sum phase shifter after a 2-stage poly-phase filter, employs a compact 6-bit binary weighted current source array (CSA) associate with a 3-bit current bleeding CSA for constant-current calibration and phase trimming. A 3-

stage transformer-coupled PA achieves 25.1dB gain and 15.2dBm saturated output power. A programmable gain (PG) LNA is employed to adapt to echoes' power level. The first stage common-source LNA adopts 96 μ m/60nm transistors to reduce the NF, and the cascade transistor arrays of the second stage are used to program the LNA gain. An on-chip balun is designed to match the single-ended LNA to a following differential neutralized dynamic current injection based Gilbert mixer. The RxBB is composed of a fixed gain stage (GS), coarse GSs, a 5th-order elliptic Gm-C BPF, a fine GS and a linear output buffer. These stages are interleaved to achieve a tunable frequency range of 60-280MHz (for both dechirping and <280MHz chirp down-conversion) and a gain range of 0-60dB in a step of 1dB.

The phased-array TRx chip was fabricated in a 65nm CMOS process (Fig. 7) and consumes 253mW/channel at 1.2V (33.8mW DLL MPS, 21.5mW DDS, 22.9mW PLL, 15.2mW PS, 111.2mW PA, 23.6mW Rx RFFE, 50.2mW RxBB). The chip is mounted on a PCB for testing. The measured spectrum of the Tx output is shown in Fig. 3, with 9.7dBm output power (After the 5dB loss from the PCB, cable and SMA is taken into account, the calibrated Tx is with output power of 14.7dBm), <2dB ripple, 1GHz (10%) BW, 1.69ps DLL RMS jitter and -118.8dBc/Hz PLL PN at 1MHz offset. PS exhibits <1.7° phase RMSE and <0.6dB gain RMSE. In Fig. 4, Rx RFFE attains variable gain of 15.3-28.6dB in 9.5-10.5GHz, <1.1dB ripple, -37dBm IP1dB, and 5.7-6.5dB DSB NF (7.1-7.9dB DSB NF for Rx at 28.6dB RFFE gain). The RxBB gain and frequency responses are shown at three typical settings. The delay-line test shows that the dechirped pulse from RFFE output achieves -12.9dB peak sidelobe ratio (PSLR) for the 33.8kHz tone and phase coherence of 0.45° RMS at the chirp rate of 1MHz/ μ s, similarly applied to other frequencies. The -3dB BW of the mainlobe is measured as 0.52kHz, which translates to a long range resolution of <30cm. An implementation of 8dBi Vivaldi antenna with 6GHz bandwidth is demonstrated, with phased-array synthetic aperture formed, it achieves the azimuth resolution <17cm.

Fig.5 shows a typical TRx radiation pattern co-tested with the 4 by 4 Vivaldi antenna array of -53dB isolation. For Tx beamsteering, the chirp rate of 1-10MHz/ μ s is adopted; For Rx beamforming, the dechirped IF signals are collected to form digital beamforming off-line. With antennas 6cm apart to each other, the Tx can

beamsteer across angles up to $\pm 60^\circ$ with a step of 1° , and the Rx can continuously scan the same range with the resolution of $<1^\circ$, which enhance the spatial resolution in SAR imaging. Performance of the phased-array prototype and some prior arts [3-6] are summarized in Fig. 6. The X-band SAR is widely used for airborne and spaceborne applications though its IC implementations were few reported. The completed design of the phased array radar IC makes it well suited for micro-UAV and micro-satellite applications.

References:

- [1] Christopher F. Barnes, Synthetic Aperture Radar. Barnes, 2015.
- [2] L. Wang et al., "3–5 GHz 4-channel UWB beamforming transmitter with 1° scanning resolution through calibrated Vernier delay line in $0.13\text{-}\mu\text{m}$ CMOS," *IEEE J. Solid-State Circuits*, vol. 47, pp. 3145–3159, Dec. 2012.
- [3] J. Yu et al., "An X-Band radar transceiver MMIC with bandwidth reduction in $0.13\mu\text{m}$ SiGe Technology," *IEEE J. Solid-State Circuits*, vol. 49, pp. 1905–1915, Sept. 2014.
- [4] B. Ku et al., "A 77–81-GHz 16-element phased-array receiver with $\pm 50^\circ$ beam scanning for advanced automotive radars," *IEEE Trans. Microwave Theory and Techniques*, vol. 62, pp. 2823–2832, Nov. 2014.
- [5] P. Chen et al., "A 94GHz 3D-image radar engine with 4TX/4RX beamforming scan technique in 65nm CMOS," *ISSCC Dig. Tech. Papers*, Feb. 2013.
- [6] T. Chu et al., "A short-range UWB impulse-radio CMOS sensor for human feature detection," *ISSCC Dig. Tech. Papers*, Feb. 2011.

Figure 1: The proposed phased array TRX IC architecture.

Figure 2: Circuit schematics of the MPS, DDS, PS, VGLNA and RXBB.

Figure 3: Measured DLL jitter (top left), PLL PN (top right), TX chirp spectrum (bottom left), and PS RMSE (bottom right).

Figure 4: Measured RX RFFE (top left), RXBB (top right), dechirped spectrum and phase coherence (bottom left), and antenna S₁₁ (bottom right).

Figure 5: 4TX beamsteering radiation pattern (top left), 4RX beamforming pattern (top right), and phased array radar prototype (bottom).

TX Performance		RX Performance		Prototype System Performance	
DLL Jitter	1.67ps RMS	Gain	15.3-28.6dB	Range Resolution	<30cm
PLL PN@1MHz	-118.8dBc/Hz	RFFE ripple	<1.1dB	Azimuth Resolution	16.6cm
PS Phase Error	<1.7° RMS	RXBB HPF Cutoff Freq.	1MHz	PSLR	-12.9dB
PS Gain Error	<0.6dB RMS	RXBB LPF Cutoff Freq.	60-280MHz	Phase Coherence	0.45° RMS
TX Ripple	<2dB	RXBB Gain	0-60dB	Low Freq. Interference Rejection	>60dB
Power per Chl.	179.3mW	Power per Chl.	73.7mW		

	JSSC2014 [3]	TMTT2014 [4]	ISSCC2013 [5]	ISSCC2011 [6]	This work
Application	N.A.	Automotive radar	Imaging sensor	Human Feature Detection	Synthetic Aperture Radar
Transceiver Architecture	DDS+PLL+RXFE +RXBB+ADC	RXFE+PS	PLL+Tripler +PS+PA+RXFE	Osc+DLL +RXFE+RXBB	DLL+DDS +PLL+PS +RXFE+RXBB
Channel Num.	TX+RX	16RX	4TX+4RX	TX+RX	4TX+4RX
TX output BW	150MHz (1.8%)	0.5GHz (0.64%)	200MHz	1.6-2.5GHz	1GHz (10%)
Modulation Method	Chirp	FMCW	Pulsed RF	Pulsed RF	Pulsed chirp
Modulation Period	N.A.	N.A.	100ns	100ns	200μs-1ms
Stretch Processing	YES	NO	NO	NO	YES (Dual mode)
Center Freq.	8.5GHz	77GHz	94GHz	0.8-5GHz	10GHz
Beamsteering	N.A.	N.A.	±28°	N.A.	±60°@~1°
Beamforming	N.A.	±50°@~1°	±28°	N.A.	±60°@~1° Digitally
TX P _{out}	N.A.	N.A.	-5dBm	N.A.	14.7dBm
RX RFFE Gain	10.7-44.7dB	22.5dB	27-40dB	12dB	15.3-28.6dB
RX RFFE NF	2.4-4.5 (Sim.)	18dB (Sim.)	N.A.	4.5dB (Sim.)	5.7-6.5dB (DSB)
RX RFFE IP _{1dB}	-35dBm	N.A.	N.A.	N.A.	-37dBm
Power per Chl.	659mW	75mW (RX only)	240mW	695mW	253mW
Technology	0.13μm SiGe	SiGe	65nm CMOS	0.13μm CMOS	65nm CMOS

Figure 6: Performance summary and comparison.

4TX/4RX Phased Array Radar TRX IC

Figure 7: Die micrograph and layout.