A Return-to-zero DAC with Tri-state Switching Scheme for Multiple Nyquist Operations

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\textbf{Abstract}—A return-to-zero (RZ) digital-to-analog converter (DAC) with a tri-state switching scheme is proposed in this paper. The proposed scheme provides a triple weight output for RZ operation by using a conventional differential current switch and simple pseudo-differential F/Fs. The RZ function is realized with only two additional transistors in each F/F cell, which results in a power dissipation increase of less than 5\%. To verify the performance of the proposed method, a 10-bit RZ DAC is fabricated using standard 180-nm CMOS technology. Measured results show that the worst SFDR performances are 60 dBc and 55 dBc in the 1st and 2nd Nyquist bands, respectively, when operating at 650 MHz clock frequency. The total power consumption is 64 mW, and the active area occupies 0.25 mm\textsuperscript{2}.

\textbf{Index Terms}—Return-to-zero (RZ), digital-to-analog converter (DAC), tri-state switching scheme

I. INTRODUCTION

Digital-to-Analog Converters (DACs) are key components of modern communication systems such as wired/wireless transmitters, direct digital synthesizers, and arbitrary waveform generators. Especially in recent RF transmitter systems, wideband DACs with high dynamic performances are increasingly required. However, most DACs in conventional RF transmitter systems offer acceptable performance only in the 1st Nyquist band, i.e., from DC to half of the sampling frequency. One of the approaches used to overcome this limitation is a return-to-zero (RZ) DAC architecture [1-5].

Fig. 1 shows the comparison of the time- and frequency-domain characteristics between non-return-to-zero (NRZ) and RZ signals. It is evident from the time domain waveforms that the time duration of the NRZ DAC output of each quantized signal is twice that of the RZ DAC output. In other words, the RZ DAC output has half the amplitude of the NRZ DAC output at DC in the frequency domain. However, because the SINC envelope \((\sin(x) / x)\) of the RZ DAC has nulls at multiples of twice the sampling frequency (which is double the null frequency of the NRZ DAC), the flatter envelope of the RZ DAC results in less drooping in the 2nd Nyquist band. For example, the signal power loss in the NRZ DAC is 3.9 dB at half of the sampling frequency [1]. In the case of the RZ DAC, the signal power loss at half of the sampling frequency is only 0.9 dB [1]. Consequently, a wideband RF communication system implemented with an NRZ DAC would require an inverse SINC filter or equalizer. However, the RZ DAC results in less drooping for multiple Nyquist bands, which removes the need for a SINC filter or equalizer [1]. Furthermore, the RZ technique can alleviate the nonlinear effect that depends on input codes by decoupling the switching transients from the DAC output and thereby improve the DAC’s dynamic performance [5-8].

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Various RZ DAC architectures have been proposed to expand flat envelope regions and/or improve dynamic performance. The RZ structure shown in Fig. 2 [1, 2] directly connects the RZ circuits (analog switch) to DAC output to force output to be zero every clock. However, the timing mismatch between the control signals for the analog switch and the clock signals for digital latches can cause nonlinearity of the DAC output signal and reduce the output signal power. Multiple-Nyquist DAC architectures presented in [3, 4] overcome this drawback and improve high-frequency performance using a “quad-switch” structure. However, complex digital circuits for controlling current switches including switch drivers and latches increase area and power consumption. In [5, 6], a cascade current switch scheme that exhibits a simpler structure than other switching schemes was proposed for RZ Dacs. However, control signals for cascade switches can cause an additional skew problem. The digital random RZ technique (DRRZ) presented in [7, 8] overcomes this skew problem at the expense of extra digital circuitry for random operations, which causes an increase in power consumption. In this paper, an RZ DAC with a tri-state switching scheme is proposed for multiple-Nyquist operations with better dynamic performance than an NRZ DAC. When compared to other RZ Dacs, the proposed RZ DAC consumes lower power because of simpler structure for RZ operations.

II. TRI-STATE SWITCHING SCHEME

Fig. 3 shows the proposed tri-state switching scheme based on a conventional differential current switch where a digital data input pair (DP, DN) is a pseudo differential signal pair. DP and DN states can have three cases: “High”, “Low”, “High”, and “High.” The table in Fig. 3 summarizes the operating cases of the proposed tri-state switching scheme for three different digital data inputs. The differential output voltage (OP−ON) has three possible states: +Rf1d, −Rf1d, and 0. Fig. 3(a) and (b) depict the operations of a conventional differential current switch pair, whereas Fig. 3(c) shows the RZ operation of a DAC. In this case, the digital input pair (DP and DN are both “High”) is generated every half clock cycle by pseudo differential F/Fs, as shown in Fig. 4(a). In the F/F cell, DP and DN become “High” through transistors MP and MN when CK is “Low,” regardless of Din. In other words, MP forces the output of the F/F (DP and DN) to be “High,” and the MN transistor disconnects the path between the output of the

![Image](image-url)

**Fig. 1.** Comparison of the time- and frequency-domain characteristics between NRZ and RZ signals.

**Fig. 2.** Conventional RZ DAC structure.

![Image](image-url)

**Fig. 3.** Proposed tri-state switch scheme (a) DP=’High’, DN=’Low’, (b) DP=’Low’, DN=’High’, (c) DP=’High’, DN=’High’.

<table>
<thead>
<tr>
<th>Case</th>
<th>INPUT</th>
<th>OP</th>
<th>ON</th>
<th>O_P-O_N</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>H</td>
<td>L</td>
<td>Vdd</td>
<td>+Rf1d</td>
</tr>
<tr>
<td>(b)</td>
<td>L</td>
<td>H</td>
<td>Vdd-Rf1d</td>
<td>−Rf1d</td>
</tr>
<tr>
<td>(c)</td>
<td>H</td>
<td>H</td>
<td>Vdd−(Rf1d)/2</td>
<td>0 (ZERO)</td>
</tr>
</tbody>
</table>
Fig. 4. (a) Pseudo differential F/F, (b) timing diagram example of the proposed tri-state switching scheme, (c) all possible four cases of data transitions for Dp and Dn.

F/F and the ground when CK is “Low.” Therefore, all current switch pairs operate as depicted in Fig. 3(c) and the differential output current of the DAC becomes zero. The proposed switching scheme provides RZ operation with minimal overhead in terms of hardware complexity by adding only two transistors (MP and MN) to each F/F. In other words, NRZ operation can be realized simply by turning off the MP and MN transistors. Fig. 4(b) shows the timing diagram as an example. It should be noted that the proposed pseudo differential F/F does not have timing mismatch issue which may cause glitch at DAC output, because both differential outputs never change at the same time due to the proposed RZ operations. Fig. 4(c) shows all possible four cases of data transition for the pseudo differential F/F outputs (DP and DN).

Fig. 5 depicts the effect of the current mismatch in the differential switch pair for the proposed RZ switch. The current differences in the current switch pairs are added to the DAC output as a DC offset during RZ operation. Because this DC offset repeats every half clock period independent of the input digital codes, it produces a signal which frequency is equal to the sampling frequency (f0). In addition, the different transient behaviors between the with- and without-DC-offset cases can reduce the dynamic performance. Among several causes of increased DC offset, a mismatch of threshold voltages is used to determine the SFDR degradation caused by DC offset. Mismatch simulations are performed using a 4:6 segmented DAC with an R-2R ladder.

Fig. 6 shows the results of post-layout simulation for SFDR degradation caused by a threshold voltage (Vth) mismatch in the current switch pairs when clocked at 650 MHz. As shown in the simulated results, the SFDR degradation between 7.6 MHz and 322 MHz output frequencies in the 1st Nyquist band gradually increases when the Vth mismatch is increased. Note that the SFDR degradation is only about 2.5 dB even with a Vth mismatch of 6%. Therefore, the requirement of Vth mismatch to prevent SFDR degradation is considerably lower than expected. Furthermore, in real implementations, the mismatch can be easily reduced to less than 1% by placing the transistors of the current switch pair very close to each other and making them compact in layout. In addition, the well-known “cross-quad” technique, which is typically adopted in switch layout, results in less mismatch. As a result, a degradation of dynamic performance by the current
that of the NRZ operation near the input frequency of f<sub>RZ</sub>. Consequently, the power consumption of the transitions becomes similar for both the RZ and NRZ operations. However, in the case of fast data transition, as shown in Fig. 7(b), the number of transitions becomes similar for both the RZ and NRZ operations. Consequently, the power consumption of the RZ operation of the proposed DAC becomes similar to that of the NRZ operation near the input frequency of f<sub>Nyquist</sub> / 2 (Nyquist frequency).

Mismatch between the differential switch pairs can be significantly (and easily) suppressed. This V<sub>th</sub> mismatch can be easily obtained by measuring the DC offset, because the amount of DC offset is proportional to V<sub>th</sub> mismatch.

In the proposed scheme, the difference in power consumption in NRZ and RZ operations depends on the number of data transitions of each F/F. Fig. 7 shows examples of slow and fast data transitions. When data transits slowly, as depicted in Fig. 7(a), the RZ operation consumes more power than the NRZ operation because of the continuous data transition. However, in the case of fast data transition, as shown in Fig. 7(b), the number of transitions becomes similar for both the RZ and NRZ operations. Consequently, the power consumption of the RZ operation of the proposed DAC becomes similar to that of the NRZ operation near the input frequency of f<sub>Nyquist</sub> / 2 (Nyquist frequency).

**III. IMPLEMENTATION**

Fig. 8 shows the block diagram of the proposed RZ DAC with the tri-state switching scheme. The proposed RZ DAC is implemented using a partially segmented architecture to optimize power consumption, operating speed, and static/dynamic performance. In this design, the DAC is divided into two sub-blocks: one with unary architecture and the other with a binary method using an R-2R ladder. The 10-bit DAC is fabricated using standard 180-nm CMOS technology with an active area of 0.25 mm². Fig. 9 shows a microphotograph of the proposed RZ DAC. To compensate for symmetrical and gradient errors, the layout of the unary current source array is applied using a common centroid. The size (width by length) of the unit current source cell of 28 mm² is chosen. A cascode transistor between a differential current switch pair and a current source transistor was designed to increase the output impedance; this cascode transistor is designed to be as small as possible to reduce the parasitic capacitance of the source node of switches [9].
IV. EXPERIMENTAL RESULTS

The DAC’s outputs are coupled to a spectrum analyzer through a transformer and a 50-Ω output load is used. The maximum sampling clock frequency of the proposed DAC is measured up to 650 MS/s, which is limited by the operating speed of the test equipment. Fig. 10 shows the measured spectra of RZ and NRZ operation for a 636 MHz signal in the 2nd Nyquist band at 650 MS/s. The output signal power and SFDR in the RZ mode are approximately 23 dBc higher than those in the NRZ mode. Fig. 11 shows the various measured spectra of the proposed RZ DAC in the 1st and 2nd Nyquist bands at 650 MS/s clock frequency. Fig. 11(a)-(c) show the DAC output spectra at 14 MHz, 217 MHz (f_s / 3), and 320 MHz (f_s / 2), respectively, in the 1st Nyquist band. Fig. 11(d) shows the DAC output spectrum of 433 MHz in the 2nd Nyquist band. Fig. 12 shows the SFDR.
performance of the proposed RZ DAC as a function of output frequency up to the 2nd Nyquist band when clocked at 650 MS/s. The measured results exhibit that the RZ mode retains the SFDR over 60 dBc throughout the 1st Nyquist band, and the worst SFDR of RZ mode is 55 dBc in the 2nd Nyquist band. A DC offset of approximately 3 mV is measured, which represents a VTth mismatch of less than 0.5%. The maximum power consumption for the RZ mode in this study is 64 mW, which is only approximately 5% more than that in the NRZ mode. Analog power and digital power consumption are 40 mW and 24 mW, respectively. Fig. 13 shows the DUT board and test environment for the static linearity measurements and Fig. 14 indicates the measured DNL and INL performance, which are +2.8/-0.24 LSB and the INL is +2.43/-2.46 LSB, respectively. The DNL/INL results are worse than the anticipated results. It should be noted that the static performance is not related to the proposed scheme but because of component mismatches. The MSB cells use thermometer-coded current sources while the LSB employs R-2R ladder structure with current sources. And parasitic routing (metal) and contact resistances in R-2R structure as well as DAC current output line resistance at each tab (between current cells) affect the mismatch errors. It is why the peak error repeats every 64 codes, and the INL error gradually becomes larger within 64 code (6-bit LSB region).

In Table 1, the measured results are compared to state-of-the-art high-speed (> 500 MS/s) and high-resolution (> 10 bits) DACs with similar CMOS technologies (> 90 nm). This work shows a wider effective bandwidth (BW) of 650 MHz than previously reported gigahertz-range DACs [4, 7, 11, 12], while retaining an SFDR greater than 55 dBc (despite having a lower sampling rate than these DACs). The BW defined by BW = fS @ {SFDR ≥ 6(N - 1) dB} takes into account an SFDR as a function of the resolution (N), which is governed by the formula introduced in [13] and adopted in [10]. When compared to the RZ DAC in [10], the measured absolute total power consumption and active area are greater. However, the proposed RZ DAC can achieve twice the BW and SFDR improvements by adding only two transistors in the F/F cell and slightly increasing power consumption relative to the NRZ DAC. Additionally, note that the proposed scheme can be easily combined with the random rotation-based binary-weighted selection technique presented in [10]; thereby, a multiple
Nyquist operation and improved dynamic and static performance can be achieved.

V. CONCLUSIONS

An RZ DAC operating at a multiple-Nyquist-frequency band is presented. The proposed RZ DAC with a tri-state switch scheme provides a wideband and high-dynamic range analog output with a minimal increase in power consumption and hardware complexity. The SFDR of the proposed RZ DAC remains higher than 60 dBe throughout the 1st Nyquist band, and the worst SFDR of 55 dBe is achieved in the 2nd Nyquist band.

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REFERENCES

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