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**NANYANG
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SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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ULTRA-LOW POWER DIGITAL INTEGRATED CIRCUIT DESIGN

LE VAN LOI

School of Electrical and Electronic Engineering

**A thesis submitted to the Nanyang Technological
University in partial fulfillment of the requirement for the
degree of Doctor of Philosophy**

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

26 May 2019

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Date

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Le Van Loi

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

26 May 2019

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Date

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Kim Tae-Hyoung

Authorship Attribution Statement

This thesis contains material from 2 papers published in the following peer-reviewed journals where I was the first and/or corresponding author.

Chapter 3 is published as V. L. Le, J. Li, A. Chang, and Tony T. Kim, “A 0.4-V 0.138-fJ/Cycle Single-Phase-Clocking Redundant-Transition-Free 24T Flip-Flop with Change-Sensing Scheme in 40-nm CMOS,” in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 53, pp. 2806-2817, Oct. 2018. DOI: 10.1109/JSSC.2018.2863946

The contributions of the co-authors are as follows:

- Prof. Tony T. Kim and A. Chang provided the initial project direction.
- I designed and implemented the flip-flop under the supervision of Prof. Tony T. Kim, A. Chang, and J. Li.
- I implemented the test chip under the supervision of Prof. Tony T. Kim with the assistance of J. Li and A. Chang at NXP Semiconductors Singapore.
- Prof. Tony T. Kim, A. Chang, and J. Li assisted in patenting the flip-flop design.
- I performed all the test chip measurements at the Centre of Excellence in IC Design, the School of Electrical and Electronics Engineering under the supervision of Prof. Tony T. Kim.
- I prepared the manuscript drafts and revised the manuscript based on reviewers' comments. The manuscript was reviewed and revised by Prof. Tony T. Kim.

Chapter 4 is published as V. L. Le and Tony T. Kim, "An Area and Energy Efficient Ultra-Low Voltage Level Shifter with Pass Transistor and Reduced-Swing Output Buffer in 65-nm CMOS," in *IEEE Transactions on Circuits and Systems-II (TCAS-II)*, vol. 65, pp. 607-611, May 2018. DOI: 10.1109/TCSII.2018.2820155

The contributions of the co-authors are as follows:

- Prof. Tony T. Kim provided the initial project direction.
- I designed and implemented the level shifter under the supervision of Prof. Tony T. Kim
- I performed all the test chip measurements at the Centre of Excellence in IC Design, the School of Electrical and Electronics Engineering under the supervision of Prof. Tony T. Kim.
- I prepared the manuscript drafts and revised the manuscript based on reviewers' comments. The manuscript was reviewed and revised by Prof. Tony T. Kim.

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The contributions of the co-authors are as follows:

- Prof. Tony T. Kim provided the initial project direction.
- I co-designed the system with Dr. Taegeun Yoo under the supervision of Prof. Tony T. Kim. My main work is the digital signal processor, whereas Dr. Taegeun Yoo's work is the image sensor.
- I co-performed all the test chip measurements at the Centre of Excellence in IC Design, the School of Electrical and Electronics Engineering with Dr. Taegeun Yoo under the supervision of Prof. Tony T. Kim.
- Dr. Ngoc Le Ba provided guidance on the initial direction of the digital signal processor.
- Prof. Kwang-Hyun Baek and Ju Eon Kim assisted in the implementation of the image sensor.
- I and Dr. Taegeun Yoo prepared the manuscript drafts and revised the manuscript based on reviewers' comments. The manuscript was reviewed and revised by Prof. Tony T. Kim.

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The contributions of the co-authors are as follows:

- Prof. Tony T. Kim provided the initial project direction.
- I co-designed the system with Dr. Taegeun Yoo under the supervision of Prof. Tony T. Kim. My main work is the digital signal processor with self-adaptive motion detection and noise-tolerant outermost-edge-based feature extraction, whereas Dr. Taegeun Yoo’s work is the low power image sensor.
- I co-performed the test chip measurements at the Centre of Excellence in IC Design, the School of Electrical and Electronics Engineering with Dr. Taegeun Yoo under the supervision of Prof. Tony T. Kim.
- Prof. Kwang-Hyun Baek and Ju Eon Kim assisted in the implementation of the image sensor.
- I and Dr. Taegeun Yoo prepared and revised the manuscript drafts. The manuscript was reviewed by Prof. Tony T. Kim.

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Summary

The insatiable demand for higher chip performance and level of integration has recently encountered a tough challenge in increasing the clock speed due to excessive power consumption which causes thermal issues on silicon and limits chip yield and reliability. Moreover, there has been an increasingly ongoing demand for portable devices and wireless sensor nodes, requiring low power consumption due to their small form-factor. Thus, low-power design has become one of the most critical design constraints that chip designers are required to take into considerations at all design levels.

In the first part of this thesis, we identified several critical circuit components in VLSI systems that typically suffer from large power consumption, proposed new techniques to reduce power significantly as well as improving performance and area efficiency, and demonstrated their effectiveness through test chip measurements. Flip-flops (FFs) are fundamental building blocks in modern processors, dominating the total power of the overall system due to redundant transitions of a large number of internal clocked nodes. The state-of-the-art FFs address this power issue with the expense of area penalty and functional failures at low-voltage operations. In Chapter 3, we proposed a low-power change-sensing flip-flop (CSFF) with low-voltage operations and almost the same area as the conventional transmission-gate FF (TGFF). By utilizing a local change-sensing scheme for eliminating the redundant transitions, CSFF does not consume any dynamic power when there is no data activity. CSFF saves up to 90% power dissipation at 5% data activity compared to TGFF. CSFF also enhances performance and minimum operating voltage. Test chip measurements in 40nm CMOS demonstrate successful operations of CSFF down to 0.19 V and the delay improvement of 37% compared to TGFF. Level shifters are also one of the critical components in voltage-scaled VLSI systems. The conventional current mirror level shifter induces large standby power due to the “mirrored” current during the high input. Recently introduced level shifters eliminate the static power problem at the cost of slow conversion speed and area overhead. In Chapter 4, we proposed an area-efficient level

shifter that addresses the static power issue with fast and energy-efficient operations by utilizing a pass transistor for fall transition and a novel reduced-swing output buffer. The proposed level shifter consists of only 11 transistors occupying $7.45 \mu\text{m}^2$, which obtains the smallest area among the state-of-the-art ultra-low voltage level shifters. Measurement results from a test chip in 65nm also demonstrate that the proposed level shifter reduces the static power and delay by $16.3\times$ and $2.7\times$, respectively, compared to the conventional Wilson current mirror level shifter. The level shifter also accomplishes the maximum switching energy reduction of $8.5\times$ and can convert deep-subthreshold voltage as low as 100 mV to the superthreshold voltage of 1.2 V.

In the second part of this thesis, we addressed the high power and area issues of the state-of-the-art gesture recognition systems for wearable devices and proposed two ultra-low power and area-efficient vision systems for gesture recognition with test chip measurements. Gesture recognition has become one of the most popular human-machine interaction techniques for smart wearable devices in recent years. However, recently introduced gesture recognition systems induce high power and area overhead, which limits their applications for wearable devices. In Chapter 5, we proposed an area-efficient and low-power real-time gesture recognition system for smart wearable devices. This proposed work utilizes a peak-based classification algorithm with less memory and a low-resolution on-chip image sensor for achieving high area efficiency and low-power. Measurement results of a test chip fabricated in 65nm CMOS demonstrate that the proposed system consumes $137.0\mu\text{W}$ at 30fps while occupying only 1.78mm^2 , which achieves the lowest power and smallest area among the recently reported gesture recognition systems. In Chapter 6, with the motivation of further reducing power consumption and as chip area as well as adding more features to the current gesture recognition system, we proposed another ultra-low power gesture recognition system for smart wearable devices. The proposed work exploits a novel highly-efficient outermost-edge-based algorithm for accurately recognizing 24 motion hand gestures with ultra-low memory. The utilization of a self-adaptive motion detector and noise-aware convolution-based feature extraction architecture significantly improves the recognition accuracy. Thus, the proposed system accomplishes accurate motion gesture recognition with an average recognition accuracy of 85% even with noisy gesture images from the on-chip low-power image sensor. Furthermore, feature extraction cores highly exploit parallelisms for accelerating the recognition speed, achieving real-time

gesture recognition with a low latency of 1.056ms. Test chip measurements in 65nm show that the proposed system consumes only 3- μ W dynamic power at 30fps while occupying 0.54-mm², which outperforms recently reported gesture recognition systems in terms of area and power, making it very well-suited for smart wearable devices.

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List of Abbreviations

Abbreviations	Description
ISSCC	International Solid-State Circuits Conference
FF	Flip-Flop
3D	3 Dimension
CSFF	Change-Sensing Flip-Flop
TGFF	Transmission-Gate Flip-Flop
WCMLS	Wilson Current Mirror Level Shifter
SoC	Systems-On-Chip
CMOS	Complementary Metal-Oxide-Semiconductor
CCKFF	Conditional Clocking Flip-Flop
C-Q	Clock-to-Q
CPFF	Conditional Pre-charged Flip-Flop
DMFF	Data Mapping Flip-Flop
ACFF	Adaptive-Clocking Flip-Flop
ACE	Adaptive-Coupling Element
TCFF	Topologically-Compressed Flip-Flop
SSCFF	Static Single-phase Contention-Free Flip-Flop
CICC	Custom Integrated Circuits Conference
JSSC	Journal of Solid-State Circuits
MEMS	MicroElectroMechanical Systems
ASIC	Application Specific Integrated Circuits
ADC	Analog-to-Digital Converter
CNN	Convolutional Neural Networks
VLSIC	Symposium on VLSI Circuits Conference
CVPR	Conference on Computer Vision and Pattern Recognition
TCAS-II	IEEE Transactions on Circuits and Systems - II
VLSI	Very Large Scale Integration
TBC	Test Bench Circuit
DTC	Digital to Time skew Circuit
SCC	Self-Calibration Circuit
CDC	Coarse Delay Control
FDC	Fine Delay Control
DVFS	Dynamic Voltage Frequency Scaling
LS	Level Shifter
EMG	Electromyography
SOM	Self-Organizing Map
DSP	Digital Signal Processor
DAC	Digital-to-Analog Converter
PISO	Parallel-Input-Serial-Output
PWM	Pulse-Width Modulation
PGCE	Peak-based Gesture Classification Engine

MDU	Motion Detection Unit
FEC	Feature Extraction Core
MGCU	Motion Gesture Classification Unit
RC	Row-Column
PDPE	Peak Detection Processing Element
FPNF	Fixed-Pattern-Noise Free
PCB	Printed Circuit Board
QFN80	Quad Flat No-Lead 80-pin Package
FPGA	Field-Programmable-Gate-Array
VGA	Video Graphics Array
DC	Direct Current
HREF	Horizontal Reference Pulse
PCLK	Pixel Clock
VSYNC	Vertical Synchronization
OEGRE	Outermost-Edge-based Gesture Recognition Engine
EDPE	Edge Detection Processing Element
CM	Custom Memory
TLD	Top Left Diagonal
TRD	Top Right Diagonal
BLD	Bottom Left Diagonal
BRD	Bottom Right Diagonal
L/R	Left/Right
U/D	Up/Down
KB	Kilobyte
SAMD	Self-Adaptive Motion Detector
LP	Low Power
GP	General Purpose

Chapter 1

Introduction

1.1. Research Motivations

Figure 1.1: The transistor count trends [1].

In recent decades, the relentless advancement of process technology has tremendously brought massive performance boosts and much more integration to modern digital circuits and systems. Figure 1.1 shows the trends in transistor integration on a single chip over the past two decades in ISSCC [1], reaching up to 15.8 billion transistors in the IBM z14™ microprocessor with a total of 240 physical cores [2]. On the other hand, the clock speed, one of the crucial metrics of system performance, once achieved 5GHz in the Power6™ microprocessor in 2007 [3]; since then, it could not follow the increasing trend observed in the transistor count. It has stayed near-constant

over the last decade, where it appears to be saturated in the range of 5~6GHz as shown in Figure 1.2 [1]. This is mainly because the extremely high clock frequency leads to excessive power consumption that causes thermal issues on silicon and significantly restricts the chip yield, reliability, and performance [4]. Thus, low-power design has become one of the most critical design constraints in integrated circuit design, requiring chip designers to take into considerations the power consumption at all design levels.

Figure 1.2: The clock frequency trends [1].

In addition, there have been increasingly ongoing demands for portable hand-held devices and wireless sensor nodes. Their power budgets are extremely restricted because their small form-factors can only accommodate a limited-size battery. For example, the modular 1mm^3 die-stacked sensing platform in [5], as shown in Figure 1.3, only allows using a $0.6\mu\text{Ah}$ thin-film battery to reliably run the whole system including two ARM® Cortex-M0 processors, sensors, radios, and other circuits. This stringent power budget requires the entire system to consume less than $40\mu\text{W}$ in active mode as well as optimize system management with an ultra-low power consumption of 11nW in sleep mode. Thus, every module in this system must consider the low-power constraint as the topmost requirement while still maintaining the system reliability. In other words, low-power design is not optional anymore; it has progressively become one of the most critical design constraints that mostly all analog/ digital circuits must satisfy.

Figure 1.3: A 1-mm³ die-stacked wireless sensor platform [5].

1.2. Research Objectives

Flip-flops (FFs) are one of the most critical components in typical low-power VLSI systems as illustrated in Fig 1.4. FFs are fundamental building blocks in the digital core; they typically dominate the total area and power of the overall system. For instance, the SPARC T4 processor in [6] contains 2.6 million FFs that are responsible for 20% of the total power of the processor as depicted in Figure 1.5. The main reason behind is that FFs consume substantial dynamic power in systems on chips (SoCs) due to redundant transitions of their large number of internal clocked nodes even when there is no data activity. Many low-power FFs [7]-[12] have been recently proposed for reducing or even eliminating power penalty coming from the redundant transitions. However, they suffer from either area penalty [7]-[8], which is too costly since FFs typically occupy a significant amount of logic area in SoCs, or functional failures at low-voltage operations [8]-[11], which makes these FFs inapplicable for low-voltage applications. Therefore, the objective of this work is to address the trade-off between power, area, and the minimum operating voltage, and to propose new techniques for reducing FF power while maintaining the area, performance, and the minimum operating voltage.

Figure 1.4: A typical architecture of a low-power VLSI system.

Figure 1.5: Power breakdown of the SPARC T4 processor [6].

Figure 1.6: A multi-supply die-stacked sensor platform [5].

Level shifters are also one of the key components in voltage-scaled VLSI systems as highlighted in Figure 1.4 since the supply voltage scaling technique has been widely employed for power reduction in today's circuits and systems. Indeed, processor cores have been voltage-scaled independently, and the number of cores has also been increased significantly [1]. For instance, the Intel IA-32 processor in [13] has 48 cores with eight different core voltages; requiring level shifting between different core voltage domains. Moreover, the low-voltage circuit design has been broadly researched for ultra-low power applications, reaching as ultra-low as 230mV in a recent pipelined microprocessor [14]. Another example is the multi-supply die-stacked sensor platform in [5], as shown in Figure 1.6, which processor's cores operate at ultra-low voltage supply for power reduction, whereas other modules such as radios, sensors, etc. are powered by a 3.6V battery. Thus, it necessitates wide-range level shifters for communicating between the processor cores and other higher-voltage modules. Recently reported low-voltage level shifters [15]–[22] suffer from the trade-off between power, area, delay, and reliability. Previously proposed cross-coupled level converters reduce the contention between very-strong pull-up and weak pull-down networks at the

expense of large area and slow conversion speed, whereas recently introduced current mirror level shifters eliminate static power at the cost of high delay and area overhead. Therefore, the target of this work is to address the trade-off between power, area, delay, and the minimum converting voltage, and to propose new techniques for achieving low-power voltage conversion from deep-subthreshold region to above-threshold region while improving delay and area efficiency.

Gesture recognition has become one of the most popular human-machine interaction techniques for smart wearable devices in recent years. The requirements for gesture recognition in wearable platforms are as follows: low power consumption due to limited battery sizes, high area efficiency because of their small form-factor, and low latency for natural interaction. However, recently proposed gesture recognition systems [23]-[27] typically suffer from large power and area overhead. Capacitive touch screens are one of the most popular techniques for gesture recognition. It is utilized in [23] for enabling 3D gesture recognition with a sensing distance of up to 30cm. Nonetheless, the driver for the oscillating plane consumes relatively high power, and it also requires a large display of $40 \times 40 \text{ cm}^2$ for applying gestures. In addition, ultrasonic [24] and infrared-based [25] techniques have also been exploited for low-power light-insensitive gesture recognition. Nevertheless, the required external excitation source and sophisticated noise filtering for the echo ultrasonic signals [24] also cause extra power and area overhead. On the other hand, due to the low sensitivity of the thermopile array, a complicated analog front-end preprocessing for the infrared signals [25] is required, which results in large area overhead. Gesture recognition using image sensors has also been widely proposed. The neural-network-based vision chip in [26] achieves high-speed gesture recognition of 7 hand gestures, but it induces excessive power and large area. The neural-network-stereo-based system in [27], as shown in Figure 1.7, enables accurate real-time 3D gesture recognition at the expense of 781.5KB on-chip memory, causing high power and area overhead. The large power and the area overhead restrict their applications for smart wearable devices. Therefore, the objective of this work is to present new techniques and systems for achieving low-power low-area real-time gesture recognition, targeting smart wearable devices.

Figure 1.7: Neural-network-stereo-based 3D gesture recognition system for smart mobile devices [27].

1.3. Research Contributions

This research work achieved the following contributions:

1. An extremely low-voltage and low-power single-phase-clocking redundant-transition-free flip-flop (FF), named change-sensing flip-flop (CSFF), has been proposed. By utilizing a local change-sensing scheme for eliminating redundant transitions of internal clocked nodes, CSFF does not consume any dynamic power when there is no data activity. CSFF saves up to 90% power dissipation at 5% data activity without additional transistors compared to the conventional transmission-gate flip-flop (TGFF). CSFF consumes only 0.138 fJ/cycle, which is 84% lower than that of TGFF, at 0.4 V and 10% activity. In addition to the significant improvement in power and energy efficiencies, CSFF also enhances performance and minimum operating voltage. The test chip measurement in 40nm CMOS demonstrates successful operations of CSFF down to 0.19 V and the delay improvement of 37% compared to TGFF in the supply voltage range of 0.4 V to 1.0 V.

2. An ultra-low voltage level shifter with fast and energy-efficient voltage conversion from the deep subthreshold region to the superthreshold region has also been proposed. The proposed level shifter achieves better performance and higher energy efficiency by addressing the reduced swing and the slow fall transition issues in prior arts. A novel reduced-swing buffer design is proposed to attain lower standby power consumption while a pass transistor is utilized for improving the speed of the fall transition. The proposed level shifter consists of only 11 transistors occupying $7.45 \mu\text{m}^2$, which obtains the smallest area among the state-of-the-art ultra-low voltage level shifters. Measurement results from a test chip fabricated in 65-nm CMOS technology demonstrate that the proposed level shifter shows the maximum leakage and speed improvements of $16.3\times$ and $2.7\times$ compared to the Wilson Current Mirror level shifter (WCMLS). The level shifter also accomplishes the maximum switching energy reduction of $8.5\times$ and can convert deep subthreshold voltage as low as 100 mV to the superthreshold voltage of 1.2 V.
3. An accurate, area-efficient and low-power real-time gesture recognition system has been proposed for smart wearable devices. This proposed work utilizes a peak-based gesture classification engine with less memory and a low-resolution and low-power on-chip image sensor for achieving high area efficiency and low-power. Furthermore, the feature extraction architecture removes fixed-pattern-noise from the low power on-chip image sensor for accuracy improvement and employs parallelism for recognition speed enhancement. Thus, the proposed system accomplishes accurate real-time gesture recognition for eight motion hand gestures with the recognition accuracy of 90.6% and latency of 4.228ms. Measurement results of a test chip fabricated in 65nm CMOS demonstrate that the proposed system consumes $137.0\mu\text{W}$ at 30fps while occupying only 1.78mm^2 , which achieves the lowest power and smallest area among the recently reported gesture recognition systems.
4. A new vision chip that further reduces area and power while accurately recognizing 24 motion hand gestures has also been proposed. The proposed system exploits a novel highly-efficient outermost-edge-based gesture recognition algorithm for correctly identifying 24 motion hand gestures with

ultra-low memory. The accuracy is significantly enhanced with the utilization of a self-adaptive motion detector and noise-aware convolution-based feature extraction. Thus, the proposed system accomplishes accurate motion gesture recognition with an average recognition accuracy of $\sim 85\%$ even with noisy gesture images from the on-chip low-power image sensor. Furthermore, feature extraction cores highly exploit parallelisms for accelerating the recognition speed, achieving real-time gesture recognition with a low latency of 1.056ms. Test chip measurements in 65nm show that the proposed system consumes only 3- μ W dynamic power at 30fps while occupying 0.54-mm², which outperforms recently reported gesture recognition systems in terms of area and power, making it exceptionally well-suited for smart wearable devices.

1.4. Thesis Organization

The rest of this thesis is described as follows. Chapter 2 reviews the state-of-the-art design techniques for low-power flip-flops and level-shifters as well as newly introduced gesture recognition systems for smart devices. Chapter 3 presents the comprehensive description of our detailed design approach and principles of the proposed FF with detailed simulation and measurement results in 40nm CMOS. Chapter 4 discusses the static power and delay issues in prior arts and presents the proposed level shifters with extensive simulation results. This chapter also explains the measurement results of a test chip in 65nm CMOS. Chapter 5 describes the main problems of the previously reported gesture recognition systems and presents the proposed peak-based gesture recognition system with system architecture, classification model, algorithm flow, and architecture features. Moreover, the test chip measurement results in 65nm CMOS are also explained. Chapter 6 presents the proposed outermost-edge-based gesture recognition system with overall architecture, proposed classification algorithm, and architecture features. Test chip implementation and measurement results of a test chip in 65nm CMOS are described in this chapter. Chapter 7 concludes this thesis and describes possible future works.

Chapter 2

Literature Review

2.1. Introduction

Recent demand for low-power design especially in portable devices requires chip designers to take into consideration the power constraint for all the circuit components in VLSI systems at all design levels. Various common low-power design techniques have been widely employed for reducing power consumption. Dynamic voltage and frequency scaling is one of the most popular methods for power reduction due to the dependence of power consumption on power supply and switching frequency. However, lowering supply voltage and frequency could reduce performance of the overall system. Dynamic power management is an efficient way for minimizing power in SoCs without performance degradation by turning the devices off when not used and waking them up when needed. Power gating technique is commonly employed for eliminating unwanted current of circuit modules that are not in use. In addition, clock gating is one of the most efficient techniques in reducing dynamic power consumption by removing the redundant clock transitions when there is no data activity. Substrate biasing is also widely utilized for reducing power by dynamically adjusting transistor threshold voltages based on operating modes of the devices.

FFs and level shifters are both critical circuit components in digital circuits and systems, whereas gesture recognition is one of the most popular human-computer interaction techniques in wearable devices. This chapter reviews the state-of-the-art design techniques for low-power flip-flops and level-shifters as well as newly introduced gesture recognition systems for smart devices. The rest of this chapter is described as follows. Section 2.2 discusses low-power design techniques of the recently proposed FFs and their major drawbacks. In Section 2.3, we present the main advantages and shortcomings of the previously reported level shifters. Section 2.4 describes the

available techniques for gesture recognition and challenges when applying for wearable platforms. Section 2.5 concludes this chapter.

2.2. State-of-the-Art Low-Power Flip-Flops

Flip-flops (FFs) are fundamental components in modern digital ICs; they dominate the total area and power of the overall systems. FFs typically consume high dynamic power in systems on chips (SoCs) due to redundant transitions of their large number of internal clocked nodes even when FF input data does not change.

2.2.1. Conventional Transmission-Gate Flip-Flop

The transmission-gate flip-flop (TGFF) is the most popular FF since it is static, contention-free, and robust with voltage scaling; but it consumes excessive power caused by internal clocked nodes CKN and CKI that always toggle as shown in Figure 2.1. This toggling even occurs when there is no data activity.

Figure 2.1: Transmission-gate flip-flop (TGFF).

2.2.2. Previously Reported Low-Power Flip-Flops

In this section, we address the disadvantages of the recently introduced low-power FFs [7-12] in comparison to the conventional TGFF as shown in Figure 2.1.

Figure 2.2 describes the schematic of the conditional-clocking flip-flop (CCKFF) in [7]. By adding logic circuits for monitoring the change in the input data, CCKFF entirely avoids redundant transitions of local nodes when no data change is detected. However, it induces large C-Q delay and area overhead due to the almost doubled transistor count compared to the regular TGFF.

Figure 2.2: Conditional-clocking flip-flop (CCKFF) [7].

The conditional pre-charged flip-flop (CPFF) (Figure 2.3) [8] also deploys a conditional pre-charge circuit for preventing the unnecessary toggling of internal nodes. Nevertheless, the use of clocked pass gates still causes unwanted transitions at node CL during the “low” phase of the input data and at node CR when the input data are consistently held “high,” resulting in high dynamic power. It also induces area penalty and larger delay. In addition, the strong contention at the output latch leads to functional failures at low-voltage operations.

Figure 2.3: Conditional pre-charged flip-flop (CPFF) [8].

Figure 2.4 shows the schematic of the data-mapping flip-flop (DMFF) [9]. DMFF reduces the power dissipation caused by undesired transitions, but it still has a local clock inverter for generating an internal clock CM. This internal clock induces substantial switching power even at low data activity. Moreover, the contention in the output latch requires additional transistors in its transistor stack for reducing contentions and avoiding functional failures at low-voltage operations.

The adaptive-coupling flip-flop (ACFF) [10] could prevent redundant transitions without area penalty by only employing the adaptive-coupling element (ACE) in the master latch and removing the ACE in the slave latch as depicted in Figure 2.5. However, this requires higher operating voltages (≥ 0.75 V) due to the strong contention in the slave latch.

Figure 2.4: Data-mapping flip-flop (DMFF) [9].

Figure 2.5: Adaptive-coupling flip-flop (ACFF) [10].

Figure 2.6: Topologically-compressed flip-flop (TCFF) [11].

The topologically-compressed flip-flop (TCFF) [11] as illustrated in Figure 2.6 removes the unwanted toggling of local clocked nodes without large area overhead by topologically compressing the structure of a combinational type FF. However, it leads to a large number of shared transistors, degrading the cell's robustness and causing functional failures at low-voltage operations (<0.6 V). For example, the shared transistor TS as highlighted in Figure 2.6 causes reduced swing at VD1 and VD2 in the master latch at low-voltage operations. It results in contentions between NMOS and PMOS networks in the master latch, inducing operational failures at low-voltage regimes.

Figure 2.7: Static single-phase contention-free flip-flop (SSCFF) [12].

The static single-phase contention-free flip-flop (SSCFF) in [12] provides robust energy-saving operations over a wide range of supply voltages with the same transistor count as TGFF. However, SSCFF only eliminates unnecessary transitions when input data persistently stay “high.” Indeed, SSCFF still suffers from power penalty due to the undesired toggling of the internal clocked node CN when the input D does not change its state from the logic “low” level as illustrated in Figure 2.7.

2.2.3. Summary

Table 2.1 summarizes the major shortcomings of the aforementioned state-of-the-art low-power FFs [7]-[12]. The FFs in [7]-[8] reduce power at the cost of large area penalty, which is too costly since FFs typically occupy a significant amount of logic area in SoCs. The FFs in [8]-[11] suffer from functional failures at low-voltage operations, which makes these FFs inapplicable for low-voltage applications. SSCFF in [12] partially eliminates the redundant toggling only when input data are at the logic “high” level. No FF can address power penalty, area overhead, and functional failures at low-voltage operations at the same time. Therefore, a new area-efficient and low-voltage FF that removes the redundant transitions for ultra-low power applications is required.

Table 2.1: Shortcomings of the state-of-the-art low-power FFs.

	TGFF Conv.	[7] CICC, 2005	[8] ISSCC, 2006	[9] ISSCC, 2008	[10] ISSCC, 2011	[11] JSSC, 2014	[12] ISSCC, 2014
Device Count	24	40	28	24 ^a	22 ^b	21	24
Low Voltage	YES	YES	NO	NO	NO	NO	YES
Redundant-Transition-Free	NO	YES	NO	NO	YES	YES	NO

^aAdditional transistors required for low-voltage operations, depending on process.

^bBecomes 26 if ACE is employed in the slave latch for low-voltage operations.

2.3. State-of-the-Art Low-Voltage Level Shifters

Voltage scaling is one of the most widely used techniques for reducing power consumption in low-power digital circuits and systems. Digital cores in modern processors have been increasingly voltage-scaled, and the number of cores has also been

significantly increased. This necessitates wide-range level shifters for communicating between the processor cores and other higher-voltage modules.

2.3.1. Previous Cross-Coupled Level Shifters

The major challenge of the conventional cross-coupled level shifter, as shown in Figure 2.8, is the strong contention between pull-up and pull-down networks, which causes functional failures when converting from deep subthreshold to higher voltages. The cross-coupled level shifter in [15] as shown in Figure 2.9 enables robust voltage shifting from 0.188V to 1.2V by employing a two-stage topology with a reduced virtual supply voltage in the first stage for limiting the contention and facilitating the wide-range voltage conversion. However, this results in large delay and area penalty. The level shifter in [16] achieves robust and fast voltage conversion from the deep subthreshold to the above-threshold domain by effectively controlling the contention as depicted in Figure 2.10. However, it suffers from high static power and large area. A self-adapting pull-up structure is exploited in [17] so that the level shifter (Figure 2.11) can convert from the extremely low input voltages to the nominal voltage of 1.8V with low static power, but it comes at the expense of large area and delay.

Figure 2.8: Conventional cross-coupled level shifter.

Figure 2.9: Two-stage cross-coupled level shifter [15].

Figure 2.10: Contention-controlled level shifter [16].

Figure 2.11: Self-adapting level shifter [17].

2.3.2. Previous Current Mirror Level Shifters

The conventional current mirror level shifter as shown in Figure 2.12 avoids the contention by using a current mirror instead of the cross-coupled structure. However, the static current for maintaining the mirrored current results in large standby power when input data consistently stay at the logic ‘high’ level. Several current mirror level shifters [18]-[22] have been proposed to resolve this major drawback. The Wilson current mirror level shifter (WCMLS) [18] (Figure 2.13) uses the feedback transistor M2 to prevent the static current. When the static current is cut off, the voltage swing at node n1 is reduced; this results in high static current at I2. Furthermore, the speed of the fall transition also deteriorates drastically due to the input inverter I1 and the charge sharing from node n2 to n3 via M2. The level shifter in [19] uses a logic error correction circuit instead to eliminate the high static current and achieve low standby power, but it suffers from large delay and area penalty. The revised level shifter in [20] proposes an input-controlled diode chain, as shown in Figure 2.14, to avoid the voltage swing issue in WCMLS for eliminating the static current, but it also induces large area and slow transition speed. A self-controlled current limiter is effectively used in [21] to reduce

the standby current. However, this also comes at the price of high delay and large area. The level shifter in [22] achieves low power by employing a new topology based on the current mirror structure and a level-shifting capacitor as shown in Figure 2.15. Nevertheless, it still induces large delay and area overhead.

Figure 2.12: Conventional current mirror level shifter.

Figure 2.13: Wilson current mirror level shifter (WCMLS) [18].

Figure 2.14: Revised level shifter with an input-controlled diode chain [20].

Figure 2.15: Current mirror level shifter employing a level-shifting capacitor [22].

2.3.3. Summary

Table 2.2 summarizes the main shortcomings of the previous ultra-low voltage level shifters. No level shifter can address the trade-off between power, delay, and area overhead at the same time. Recently reported cross-coupled level converters reduce the contention between very-strong pull-up and weak pull-down networks at the expense of large area and slow conversion speed, whereas newly introduced current mirror level shifters eliminate static power at the cost of high delay and area overhead. Therefore, a new area-efficient and low-voltage level shifters with fast and energy-efficient operations is required.

Table 2.2: Major drawbacks of the previous ultra-low-voltage level shifters.

	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[22]
High Standby Power	NO	YES	NO	YES	NO	NO	NO	NO
Large Delay	YES	NO	YES	YES	YES	YES	YES	YES
Area Overhead	YES	YES	YES	NO	YES	YES	YES	YES

2.4. State-of-the-Art Gesture Recognition Systems

2.4.1. Capacitive-Based Gesture Recognition

One of the most popular techniques for gesture recognition is capacitive touchscreens. The capacitive-based system in [23] as shown in Figure 2.16 enables 3D gesture recognition with the sensing distance of up to 30cm. The distance is obtained using the following method. First, the system performs capacitance sensing via frequency modulation as shown in Figure 2.17 and improves the sensitivity of frequency readout by utilizing high-Q oscillators. Second, the system also eliminates electrostatic coupling between the sensing electrodes and surrounding ground planes for enhancing the capacitance signal. However, it requires a large display size of 40×40cm² for applying gestures. Moreover, it also induces large power consumption due to the oscillating plane driver.

Figure 2.16: Capacitive-based gesture recognition system [23].

Figure 2.17: Frequency modulation for capacitive sensing [23].

2.4.2. Ultrasonic Gesture Recognition

Touchless gesture recognition using sound can provide compact and intuitive features with ambient light insensitivity. The ultrasonic system in [24] allows 3D hand gesture recognition with the sensing range of up to 1 meter. The system utilizes a MEMS transducer chip and an ASIC to sense the location of hands as illustrated in Figure 2.18. The system localizes the hand gestures using pulse-echo time-of-flight methods. Each of the 10 transceiver channels, including a transmitter and a readout circuit, interfaces with the MEMS transducer chip. Then, echoes from the hand gestures arrive with different phase shifts for each element in the array. Finally, the off-chip digital beam former realigns the signal phase to enhance the SNR and identify the location of the hand gestures. However, the required external excitation source and sophisticated noise filtering for the echo ultrasonic signals also cause high power consumption and area overhead.

Figure 2.18: Ultrasonic gesture recognition system [24].

2.4.3. Infrared-Based Gesture Sensing

Gesture recognition using infrared is exploited in [25] for low power consumption, shown in Figure 2.19. A thermopile array is used to generate voltages which are linearly proportional to the temperature difference between hand gestures and the environment. Based on the generated thermal data of hand gestures, the system utilizes a motion history image technique to recognize up to 8 different motion hand gestures. However, due to the low sensitivity of the thermopile array, a complicated analog front-end preprocessing for the infrared signal is required, which causes large area overhead.

Figure 2.19: Infrared gesture sensing system [25].

2.4.4. Gesture Recognition Using Electromyography

Electromyography is also utilized for achieving low-latency and accurate gesture recognition in [29]. The system as shown in Figure 2.20 utilizes conductive solid gel surface electrodes that are located on 4 different muscles for recording neural signals. The analog front-end circuits are used to filter-out noises and amplify the recorded neural signals. Then, an integrated 12-bit ADC samples the amplified neural signals. Finally, the microcontroller performs gesture recognition using the digital sampled

neural signals. Thus, the system enables real-time gesture recognition for ten hand gestures as illustrated in Figure 2.21. However, it suffers from a large device size (850mm^2) and excessive power consumption (189.2mW) due to the employment of complex analog front-end circuits and artificial neural networks.

Figure 2.20: Electromyography-based gesture recognition system [29].

Figure 2.21: 10 hand gestures with different electromyography signal patterns [29].

2.4.5. Vision-Based Gesture Recognition

In addition to sound, infrared, and electromyography, gesture recognition systems [26]-[28] using image sensors have also been widely proposed. However, conventional vision systems for gesture recognition typically endure excessive power and area overhead due to large memory sizes and sophisticated image processing algorithms such

as the convolutional neural network (CNN). The vision chip in [26] as shown in Figure 2.22 can recognize seven gestures at a high frame rate of >1000fps by utilizing a reconfigurable processing element array processor and self-organizing map neural network. Nevertheless, it induces excessive power consumption (630mW) and large chip size (82.3mm²).

Figure 2.22: Vision chip for gesture recognition [26].

The gesture recognition system in [27] as shown in Figure 2.23 accurately enables real-time hand-depth sensing and hand tracking by employing a stereo matching technique with CNN-based feature extraction cores, but it also consumes high power (9.02mW) with a large chip size of 16mm². The embedded system as depicted in Figure 2.24 in [28] implements an effective CNN-based architecture on the IBM TrueNorth chip for obtaining a high gesture recognition accuracy. However, the deployment of CNN leads to excessive power dissipation (169mW) while the use of the TrueNorth chip on the NS1e development board results in a large system size (8625mm²).

Figure 2.23: CNN-stereo-based gesture recognition SoC [27].

Figure 2.24: CNN-based gesture recognition embedded system [28].

2.4.6. Summary

Table 2.3 summarizes the major drawbacks of the state-of-the-art gesture recognition systems [23]-[29]. The requirements for gesture recognition in wearable platforms are low power consumption due to limited battery sizes, high area efficiency because of their small form-factor, and low latency for natural interaction. However, recently proposed gesture recognition systems induce large power and area overhead, which restrains their applications for wearable devices. Therefore, a low-power and area-efficient real-time gesture recognition system for smart wearables is required.

Table 2.3: Major drawbacks of recently introduced gesture recognition systems.

	[23] ISSCC 2014	[24] ISSCC 2014	[25] VLSIC 2016	[26] JSSC 2014	[27] ISSCC 2018	[28] CVPR 2017	[29] TCAS-II 2017
Type	ASIC	ASIC	ASIC	ASIC	ASIC	Embedded	Embedded
Method	Capacitive	Ultrasonic	Infrared	Vision	Vision	Vision	Electro- myography
Low Area	NO	NO	NO	NO	NO	NO	NO
Low Latency	YES	YES	YES	YES	YES	NO	NO
Low Power	NO	NO	YES	NO	NO	NO	NO

2.5. Conclusion

This chapter reviews the state-of-the-art design techniques for low-power FFs and level shifters. Recently proposed low-power FFs reduce power consumption at the expense of large area penalty and functional failures at low-voltage operations, whereas the state-of-the-art level shifters suffer from the trade-off between power, area, delay, and the minimum converting voltages. The available gesture recognition techniques for smart devices are also discussed in this chapter. They typically induce large area overhead and excessive power consumption, which limits their applications for wearable devices.

Chapter 3

Low-Power Change-Sensing Flip-Flop

3.1. Introduction

The relentless advancement of process technology has tremendously brought massive performance boosts and much more integration to modern digital circuits and systems. However, this results in the expense of the increasingly high power consumption. In addition, there have been increasingly on-going demands for portable hand-held devices and wireless sensor nodes. Nevertheless, their small form factors can accommodate only limited-sized batteries, necessitating low-power consumption. Thus, low power has become one of the most critical design constraints in integrated circuits (ICs) design. Flip-flops (FFs) are fundamental components in modern digital ICs; they dominate the total area and power of the overall systems. FFs typically consume high dynamic power in systems on chips (SoCs) due to redundant transitions of their large number of internal clocked nodes even when FF input data does not change. The transmission-gate flip-flop (TGFF) is the most popular FF since it is static, contention-free, and robust with voltage scaling; but it consumes excessive power caused by internal clocked nodes CKN and CKI that always toggle as shown in Figure 2.1. This toggling even occurs when there is no data activity. Several low-power FFs [7]-[12] have been recently proposed for reducing or eliminating power penalty coming from the redundant transitions. However, they suffer from either large area penalty [7]-[8], which is too costly since FFs typically occupy a significant amount of logic area in SoCs, or functional failures at low-voltage operations [8]-[11], which makes these FFs inapplicable for low-voltage applications. Thus, a new area-efficient and low-voltage FF that removes the redundant transitions for ultra-low power applications is required.

In this work, we present a novel FF circuit that eliminates the redundant transitions of local clocked nodes for achieving extremely low-power consumption without extra transistors while further improving performance and minimum operating voltage. This

chapter presents comprehensive descriptions and simulations of the previously reported FFs, our detailed design approach, and principles of the proposed change-sensing FF (CSFF) with detailed simulation and measurement results. The rest of this chapter is described as follows. In Section 3.2, we describe our design approach. Section 3.3 presents the proposed CSFF with a change-sensing scheme and extensive simulation results, followed by the test circuit implementation in Section 3.4. Measurement results are explained in Section 3.5, and Section 3.6 concludes this chapter.

3.2. Design Approach

As discussed in Chapter 2, no FF can address power penalty, area overhead, and functional failures at low-voltage operations at the same time, which is the main goal of this work. With the motivation of reducing power consumption while maintaining the similar cell area, comparable performance, and functionality at low-voltage operations, it is important to eliminate the unnecessary transitions of internal clocked nodes while keeping the same device count without any strong contention in the FF. As discussed in Section 2.2.1, the mainstream TGFF consumes large dynamic power due to the redundant transitions of the always-toggling nodes CKI and CKN, generated by two local clock inverters. To remove one clock inverter and reduce the number of internal clocked nodes, we started with the conventional master-slave FF, but using stacking transistors instead of transmission gates as illustrated in Figure 3.1. This also allows us to reduce the transistor count later by merging logically equivalent transistors. To eliminate the unwanted toggling of the internal clocked node CN caused by the remaining clock inverter while keeping the same transistor count, we developed the proposed FF through the following steps. Firstly, we propose a change-sensing scheme, as shown in Figure 3.2, which detects the change in the FF data and toggles the local clocked node CS for storing new data only if the input data change its state. The proposed change-sensing scheme comprises six transistors and prevents the clocked node CS from toggling if there is no data activity. This redundant-transition-free feature significantly reduces the dynamic power of the FF. However, this still requires four additional transistors. Thus, we investigated the functionality of each device and found several functionally equivalent devices that can be merged. After applying the above steps, we developed an FF circuit as shown in Figure 3.3 that senses the change in the FF data and eliminates the redundant transitions of internal nodes with the same device

count as the typical TGFF. Compared to the external clock gating technique, the proposed FF internally removes the redundant transitions without large area overhead. The detailed operation of the proposed FF is explained in the following section.

Figure 3.1: The conventional master-slave FF using stacking transistors.

Figure 3.2: Change-sensing scheme for eliminating the redundant toggling of CS.

3.3. Proposed Change-Sensing Flip-Flop (CSFF)

3.3.1. Proposed Change-Sensing Scheme

This section explains the principle of the proposed change-sensing scheme for eliminating the unnecessary transitions of internal nodes. Figure 3.3 describes the schematic diagram of the proposed change-sensing flip-flop (CSFF) including a master latch, the change-sensing scheme, and a slave latch. The master latch consists of T1, T2, T3, and its latch (T7, T10, T11, T12, and I1), and the slave latch is composed of T10, T15, T16, T17, I2, and its latch (T9, T22, T23, T24, and I3). The change-sensing scheme (T4, T5, T6, T7, T8, and T9) as highlighted in Figure 3.3 detects the change in the FF data for preventing the redundant transitions of the internal clocked node CS.

Figure 3.3: Schematic of the proposed change-sensing FF (CSFF) with the change-sensing scheme for eliminating unnecessary transitions.

Figure 3.4: Operation details of the change-sensing scheme.

Figure 3.4 illustrates the operation details of the change-sensing scheme. When the clock signal CK is at the logic “low” level, the change-sensing configuration is in the pre-charge phase and the local clocked node CS is pre-charged through $T4$. At the rising edge of the clock, the change-sensing scheme switches to the sensing phase. When the input D changes from the logic “low” to “high” level, CS is discharged through the “low-to-high-sensing” path ($T5$, $T6$, and $T7$). On the other hand, the data change from “high” to “low” discharges CS through the “high-to-low-sensing” path ($T5$, $T8$, and $T9$). Otherwise, the internal node CS is always held “high” by $T4$ in every clock cycle. With the aid of the local change-sensing scheme, the clocked node CS is only toggled when the input D changes its state. When the applied input data are continuously the same as

the previous data stored in the slave latch, no redundant transitions occur. Therefore, the proposed CSFF completely removes the unnecessary toggling, which always happens in the mainstream TGFF.

Figure 3.5 illustrates the transitions of the local clocked nodes in the typical TGFF, DMFF, CPFF, SSCFF, CCKFF, and the proposed CSFF. TGFF and DMFF always show the unnecessary toggling of their internal nodes due to the clock inverters as illustrated in Figure 2.1 and Figure 2.4, respectively, whereas CPFF exhibits redundant transitions at the local nodes CL and CR due to the clocked pass gates as highlighted in Figure 2.3. Undesired toggling also happens in SSCFF at the clocked node CN when the input D persistently stays at the logic “low” level as illustrated in Figure 2.7. The proposed CSFF and CCKFF eliminate redundant toggling of their local clocked nodes when input data does not change regardless of the input data level, whereas ACFF and TCFF remove internal clocked nodes.

Figure 3.5: Transitions of the local clocked nodes in TGFF, CPFF, DMFF, SSCFF, CCKFF, and the proposed CSFF.

3.3.2. Proposed CSFF Operation

Figure 3.6 illustrates the detailed operation of the proposed CSFF. When CK is “low,” the local clocked node CS pre-charges through T4. The master latch is in the transparent mode to pass the new data to the FF, whereas the slave latch is in the hold mode to keep the previous data. When CK goes “high,” the change-sensing scheme switches to the sensing phase. It discharges the internal node CS when the change in the input data is detected. CS is discharged through the “high-to-low- sensing” path when the new data are “low,” whereas the new “high” data discharge CS through the “low-to-high-sensing” path. Then, the discharged CS turns the master latch to the hold mode to keep the new data, whereas the slave latch is switched to the transparent mode to pass the updated data to the output. If the updated level is “low,” QN is held “high” by T10 and T15; thus, the output Q goes “low.” In the case that the stored level is “high,” QN is kept “low” by T16 and T17; then, the output Q goes “high.”

Figure 3.6: Operation of CSFF.

3.3.3. Discussions on Floating Nodes and Race Condition

3.3.3.1. Floating Nodes

The redundant-transition-free feature of the proposed CSFF has three conditional floating nodes including CS, DN, and QN. However, they are not affecting the functionality of the proposed CSFF. The detailed explanations are given as follows.

CS is floating “high” when there is no change in the input data and CK is “high.” However, the degradation of node CS’s voltage during the floating condition does not affect the functionality of the CSFF. In the worst case, if the CS voltage is degraded to “low,” the master latch is turned to the hold mode, and the slave latch is switched to the transparent mode; then, the same data is passed to the output, which is identical to the normal FF operation.

DN and QN are floating “high” when CK is “high,” and the input D does not change its state from the logic “low” level. However, with the aid of the change-sensing scheme with the optimized sizing achieved through extensive simulations, the changes in DN and QN during their floating conditions leading to the corresponding changes of DI and QI are detected. CS is discharged through the change-sensing paths; then, DN and QN are held “high” by T11 and T15, respectively. To speed up the restoring of these nodes, the sizes of the NMOS transistors on the change-sensing paths are increased for shortening the discharging time of CS. In addition, the PMOS transistors including T11, T10, and T15 are also up-sized for quickly recovering the high level of DN and QN once CS is triggered. More importantly, T10 and T15 are strengthened to overpower T9 and T24 for preventing their fighting during the restoring of the QN.

3.3.3.2. Race Condition

A race condition happens when the input D changes from “low” to “high” during the high CK and low data (e.g., DN=1). However, the change-sensing scheme detects the change in D and discharges CS to hold DN and QN for preventing the wrong Q as follows. During DN=1, the high CK and QN turn T5 and T6 on, whereas the low DI keeps T10 on. When D changes from “low” to “high,” the change in D is detected by the change-sensing scheme through T7; then, CS is discharged through T5, T6, and T7. The discharged CS holds DN and QN through T11 and T15, respectively. Thus, QI is kept low, and the wrong Q is prevented.

Figure 3.7 shows the simulated minimum operating voltages of the proposed CSFF and the other FFs at different process corners when sweeping the voltage supply from 0 V to 1 V with a step size of 0.01V. With the aid of the change-sensing scheme, CSFF achieves fully-functional operations in the voltage range of 0.3 V to 1.0 V. With the contention-free and fully-static operations, CCKFF, TGFF, and SSCFF are also fully-functional at low-voltage operations. ACFF, DMFF, TCFF, and CPFF require higher operating voltages due to their strong contentions at low-voltage regimes.

Figure 3.7: Simulated minimum operating voltages of CSFF and the other FFs at different process corners when sweeping the voltage supply from 0V to 1V.

3.3.3.3. Simulation Analysis and Comparison

The recently introduced low-power FFs in [7-12], the mainstream TGFF, and the proposed CSFF are implemented and simulated in 40nm CMOS for fair comparisons.

Figure 3.8 shows the simulated power waveforms of the proposed CSFF and the other FFs at 1.0 V and 100MHz. CSFF, CCKFF, TCFF, and ACFF only consume dynamic power when the input D changes. The power waveforms of the other FFs

correspondingly reflect the redundant transitions of their internal nodes when there are no changes in the input data D as illustrated in Figure 3.5. TGFF and DMFF show dynamic power in every clock cycle due to the local clock inverters. CPFF also exhibits switching power corresponding to the clock toggling because of the clocked pass gates, whereas SSCFF consumes dynamic power whenever the clock toggles during the “low” phase of the input data. CSFF

Figure 3.8: Simulated power waveforms of the proposed CSFF and the other FFs at 1.0V and 100MHz.

Figure 3.9 demonstrates the simulated normalized power of CSFF and the previously reported low-power FFs compared to the conventional TGFF at different activity rates. CSFF, ACFF, and TCFF exhibit the lowest power consumptions among all of the simulated FFs because of their redundant-transition-free characteristics. CCKFF also eliminates unwanted transitions, but the almost double transistor count and a large number of local clocked nodes (e.g., MI, MN, SI, and SN) result in higher power consumption especially when data activities increase. TGFF, DMFF, CPFF, and SSCFF consume more significant power due to the unnecessary toggling of their local clocked nodes as illustrated in Figure 3.5.

Figure 3.9: Simulated normalized power of CSFF and the recently proposed low-power FFs compared to the typical TGFF.

Figure 3.10 shows the simulated C-Q delays of CSFF and the other FFs when sweeping the supply voltage from 0.4 V to 1.0 V. The proposed CSFF, ACFF, and TCFF show smaller C-Q delays with lowest power consumptions, but TCFF and ACFF fail to operate at low-voltage supplies at skewed corners (FS and SF) as simulated in Figure 3.7. The 40nm CMOS chip measurements in [5-6] demonstrate that TCFF and ACFF show the minimum operating voltages of 0.6V and 0.75V, respectively, making it inapplicable for ultra-low-power applications where voltage scaling is required.

Figure 3.10: Simulated C-Q delays of CSFF and the other FFs when sweeping the supply voltage from 0.4V to 1.0V.

Table 3.1: Simulation comparisons of CSFF and the other FFs.

	Device Count	C-Q Delay (ps)	Setup Time (ps)	Hold Time (ps)	Total Power (10% activity)
TGFF	24	83.5	83.4	-10.0	1.000
CCKFF	40	120.0	228.7	26.7	0.646
CPFF	28	101.0	99.1	45.0	0.528
DMFF	28 ^a	131.2	61.6	21.4	1.265
ACFF	22	65.6	177.8	-49.6	0.362
TCFF	21	59.1	346.3	-55.9	0.394
SSCFF	24	67.2	141.3	1.4	0.667
CSFF	24	60.7	141.1	-14.0	0.407

Process: 40nm CMOS

Temperature: 27°C

Condition: Typical

Supply Voltage: 1.0V

C-Q Delay: Average CK-to-Q delay of low and high input D

Setup and Hold Time: Worst case setup/hold time, defined at 10% increase of C-Q delay from stable value

Total Power: Total power including FF's power and its external clock driving power, normalized by TGFF's

^aFour transistors are added to the transistor stack of the output latch for reducing contentions

Table 3.1 includes simulated worst case setup/ hold time of CSFF and other low-power FFs at 1.0 V. The transistor-stacking structure of CSFF requires more setup time compared to the conventional TGFF. Compared to CCKFF, TCFF, and ACFF, the proposed CSFF shows smaller setup time. However, CPFF and DMFF necessitate less setup time than CSFF. In term of hold time as simulated in Figure 3.11, the worst case hold time of CSFF is when D changes from “low” to “high” just after the CK rising edge. The high CK must discharge CS fast enough to turn off T3 before the high D can change the master's stored data; otherwise, hold time failure may occur. The optimized sizing for the change-sensing scheme of CSFF achieved through extensive simulations results in negative hold time in the worst case hold time scenario. TGFF shows lesser

negative hold time than CSFF due to the use of the two clock inverters as highlighted in Figure 2.1 in hold time paths. Compared to CPFF, DMFF, CCKFF, and SSCFF, CSFF also has more negative hold time, whereas TCFF and ACFF achieve better hold time than CSFF.

(a)

(b)

Figure 3.11: Simulated hold time when input data are (a) “low” and (b) “high” at $V_{DD}=1.0V$.

Table 3.1 also includes the total powers of the FFs when including external clock driving powers. With the smaller numbers of total clock-related transistors and the redundant-transition-free features, CSFF, TCFF, and ACFF obtain lowest total power consumptions while CCKFF shows higher power due to the almost double device count and a large number of local clock nodes (e.g., MI, MN, SI, and SN). Table 3.1 also summarizes the simulation comparisons of the proposed CSFF and the other FFs. CSFF is the only FF among all of the compared FFs with the lowest power consumption and smallest delay with fully functional operations at low-voltage regimes and the same transistor count as the regular TGFF.

3.4. Test Circuit Implementation

For comparison, we implemented CSFF, TGFF, and SSCFF in a 40nm CMOS test chip. DMFF, ACFF, and TCFF were not implemented due to their limitations at low voltage operations. CCKFF and CPFF were also not included because of their large area overhead and delay. Following are the test circuits for measuring power consumptions (Figure 3.12) and timing performance (Figure 3.13) of the implemented FFs.

3.4.1. Test Circuit for Measuring Power Consumptions

Figure 3.12 shows the test circuit for measuring power consumptions of the implemented FFs at different activity ratios. The power consumptions of 512 units of each FF are measured at various activity rates, and the average powers are obtained. The activity ratios are set by the activity rate control unit as highlighted in Figure 3.12. When INIT is “low,” the activity rate is initialized by the 20-bit input ID (ID [19:0]). When INIT goes “high,” the activity rate set by ID [19:0] is applied, and the total power consumption of the FFs is measured. It is noted that the external clock driving power is not included in the power measurement of the FFs.

3.4.2. Test Circuit for Measuring Delay/Setup/Hold Time

Figure 3.13 illustrates the test circuit for measuring delay, setup, and hold time, which is based on the structure in [30]. It includes three main modules: Test-Bench Circuit (TBC), Digital to Time skew Circuit (DTC), and Self-Calibration Circuit (SCC). TBC mainly consists of FFs and necessary buffers for measuring C-Q delay, whereas DTC includes Coarse Delay Control (CDC) and Fine Delay Control (FDC) blocks for generating digitally-controlled delay skew T_D between the input data D and the input

clock CK. For controlling T_D with a larger step T_C , the 12-bit input CD_SEL in CDC is adjusted to change the number of the coarse delay units in the data path and the clock path. For T_D control with a smaller step T_F , the 8-bit input FD_SEL in FDC is used. In addition, SCC comprising an FF chain and a ring oscillator creates digitally-controlled delays between FAST and SLOW signals using the 2-bit input RS for measuring the coarse delay T_C and the fine delay T_F .

Once T_C and T_F are known, the setup/hold time of the FFs could be accurately estimated by adjusting the time delay T_D between the clock and the data signals to the setup/hold time pass/fail point as illustrated in Figure 3.14. To measure setup time, we adjust the delay skew T_D between the data and clock signals until the setup time is not enough to make the FF operational. Similarly, we control the delay T_D between the clock and data until the FF fails due to the hold time violation for measuring hold time.

Figure 3.12: Test circuit for power measurements at different data activity ratios.

Figure 3.13: Test circuit for measuring C-Q delay, setup, and hold time.

Figure 3.14: Measuring setup/hold time by adjusting the time delay T_D between the clock and the data signals to the setup/hold time pass/fail point.

3.5. Measurement Results

Figure 3.15 shows the microphotograph of the test chip fabricated in 40nm CMOS technology. It includes the test circuits for measuring power consumptions, setup/hold time, and C-Q delay. In addition, UART is also used for controlling the activity rates of the power testing circuits, whereas the frequency divider is employed to observe the clock frequency of the ring oscillator in the delay/setup/hold time test circuit. Figure 3.16 shows the cell layouts of the proposed CSFF, SSCFF, and conventional TGFF. The proposed CSFF has the same layout size as SSCFF and only 3% layout size increase vs. TGFF, which corresponds to only a one-minimum-poly-pitch increase in 40nm CMOS technology.

Figure 3.15: Microphotograph of the test chip fabricated in 40nm CMOS technology.

Figure 3.16: Cell layouts of the implemented FFs.

Figure 3.17 and Figure 3.18 demonstrate the measured power consumptions of the FFs over different activity rates at 1.0 V and 0.4 V, respectively. By utilizing the internal change-sensing scheme, CSFF almost consumes only leakage power at 0% activity rate, and it also provides more energy-efficient operations over SSCFF and TGFF, especially at low activity rates. The average activity rate of FFs in SoCs is typically from 5% to 15%; CSFF saves up to 84%-to-60% and 90%-to-77% power compared to SSCFF and TGFF, respectively, in this range. From the power measurement, at 10% activity rate, CSFF has 82% and 84% lower power consumption vs. TGFF, at 1.0 V and 0.4 V, respectively. When compared to SSCFF, CSFF exhibits the reduction of 68% and 69%. At 20% activity rate, CSFF shows 71% and 74% improvement in total power consumption vs. TGFF, at 1.0 V and 0.4 V, respectively. Compared to SSCFF, CSFF has 51% and 48% improvement. Figure 3.19 also shows the measured total power of the FFs at 10% data activity when sweeping the supply voltage from 0.4 V to 1.0 V.

CSFF has consistently substantial power reductions of over 80% and 65% compared to TGFF and SSCFF, respectively, across the supply voltage range.

Figure 3.17: Measured total power at $V_{DD} = 1.0V$ and $f_{CK} = 50MHz$.

Figure 3.18: Measured total power at $V_{DD} = 0.4V$ and $f_{CK} = 1MHz$.

Figure 3.19: Measured total power against the supply voltage at 10% activity.

Regarding the energy consumption per cycle at 10% data activity, CSFF exhibits 82% and 84% reduction, compared to TGFF, and 68% and 69% improvement, compared to SSCFF, at 1.0 V and 0.4 V, respectively, as shown in Figure 3.20. At 0.4 V, CSFF consumes only 0.138-fJ/Cycle. Figure 3.21 shows the measured leakage power of the implemented FFs in the supply voltage range of 0.4 V to 1.0 V with the measurement conditions shown in Table 3.2. CSFF has 37% and 10% leakage improvements over TGFF and SSCFF, respectively, across the voltage range. This is because CSFF has more stacking transistors on leakage paths than TGFF and SSCFF. Figure 3.22 shows the measured C-Q delays of the FFs against the supply voltage. CSFF exhibits 37% delay reduction over TGFF in the operating voltage range of 0.4 V to 1.0 V. When compared to SSCFF, CSFF also provides a modest delay improvement of 11%.

Figure 3.20: Measured energy consumption per cycle at 1.0 V and 0.4 V at 10% activity.

Figure 3.21: Measured leakage power versus the supply voltage.

Table 3.2: Measurement conditions for leakage power.

CK	D	Leakage Power
0	0	P_1
0	1	P_2
1	0	P_3
1	1	P_4
Measured Leakage Power		$(P_1 + P_2 + P_3 + P_4)/4$

Temperature: 27°C

Number of Samples: 10

Leakage Power: Average leakage power of 10 samples

Measured Leakage Power: Average measured leakage power at four different measurement conditions.

Figure 3.22: Measured C-Q delays over the supply voltage.

Table 3.3: Comparisons of CSFF and recently proposed low-power FFs.

	CSFF (<i>This work</i>)	SSCFF ISSCC 2014	TGFF Conv. FF	CCKFF [7] CICC 2005	CPFF [8] ISSCC 2006	DMFF [9] ISSCC 2008	ACFF [10] ISSCC 2011	TCFF [11] JSSC 2014
Transistor Count	24	24	24	40	28	24 ^a	22 ^a	21 ^b
Single-Phase Clock	YES	YES	NO ^c	YES	YES	NO ^c	YES	YES
Redundant-Transition-Free	YES	NO ^d	NO ^e	YES	NO ^f	NO ^e	YES	YES
Low-Voltage Operations	YES	YES	YES	YES	NO ^g	NO ^g	NO ^g	NO ^g
Normalized Layout Size	1.03	1.03	1.00	^a Additional transistors are required for low-voltage operations. ^b Fewer transistors, but it has the same layout size as TGFF. ^c Internal inverted clocks are used. ^d Redundant transitions occur when input data persistently stays at the logic ‘low’ level. ^e Unnecessary toggling happens due to the local clock inverters. ^f Unwanted transitions exist due to the clocked pass gates. ^g Functional failures occur at low voltages ^h The measured power only includes internally consumed power and excludes clock driving power. CCKFF, CPFF, DMFF, ACFF, and TCFF were not implemented in this test chip.				
Measured Total Power (nW) ^h @1.0V, 50MHz, 10% Activity	48.8	153	270					
Measured Leakage (pW) @1.0V	176	197	295					
Measured C-Q delay (ps) @1.0V	160	177	238					
Measured Setup Time (ps) @1.0V	266.5	271.5	195					
Measured Hold Time (ps) @1.0V	-63	-54	-18					

Table 3.3 summarizes the measurements results including the measured setup/ hold time of the implemented FFs and shows comparisons with the recently introduced low-power FFs. By utilizing the internal change-sensing scheme, CSFF completely removes unnecessary transitions of local clocked nodes without adding any extra transistor compared to the mainstream TGFF and SSCFF. This redundant-transition-free feature significantly reduces the dynamic power when there are no changes in the FF data. Test chip measurement in 40nm CMOS shows that CSFF achieves 82% and 68% power reductions over TGFF and SSCFF, respectively, at 1.0V and 10% data activity. Regarding performance, CSFF exhibits modest improvement of 5% and 1.5% in total setup time and C-Q delay, compared SSCFF and TGFF, respectively. CSFF also provides better hold time, requiring a lesser constraint for hold buffers in ICs. In addition to the significant power reduction and modest performance improvement, CSFF also enhances minimum operating voltage. Measurement results of the 40nm CMOS test chip demonstrate successful operations of CSFF down to 0.19 V with the maximum frequency of 7.4-KHz. Compared to the previously reported low-power FFs [7]-[12],

CSFF is the only FF with single- phase-clocking, redundant-transition-free and low-voltage operations (≥ 0.19 V) with the smallest area penalty (only one minimum poly pitch) and the same transistor count as the regular TGFF.

3.6. Conclusion

An extremely low-voltage and low-power single-phase-clocking redundant-transition-free 24-transistor FF, CSFF, is proposed by utilizing a change-sensing scheme for eliminating redundant transitions of internal clocked nodes. The proposed CSFF eliminates dynamic power at 0% data activity. The test chip measurement in 40nm CMOS demonstrates that CSFF saves power consumption up to 90% at 5% activity rate, compared to the conventional TGFF. No additional transistors are required. CSFF also provides more energy-efficient operations than TGFF across a wide operating voltage range, especially at low data activities. While achieving better power and energy efficiencies, CSFF further improves performance and maintains functional operations at low-voltage regimes. Measurement results demonstrate the delay improvement of 37% over TGFF and minimum operating voltage of 0.19 V. Compared to the recently introduced low-power FFs [7]-[12], CSFF is the only FF with redundant-transition-free, single-phase-clocking and low-voltage operations with minimum area penalty and the same transistor count as TGFF. Therefore, CSFF could directly replace many FFs in the low-power applications particularly when the input data have relatively low activity rates.

Chapter 4

Area and Energy-Efficient Ultra-Low-Voltage Level Shifter

4.1. Introduction

Dynamic voltage and frequency scaling (DVFS) is one of the most widely used techniques for reducing power consumption in low power digital circuits and systems. In fact, digital cores on today's processors have been increasingly voltage-scaled, and the number of cores has also been significantly increased. For example, the 45nm IA processor in [13] has 48 cores and 8-core voltage domains with 24 frequency islands for enabling variation-aware DVFS; necessitating level shifting between different core voltage domains. In addition, the low-voltage circuit design has been broadly investigated for ultra-low power applications, reaching as ultra-low as 230mV in a recent pipelined microprocessor [14]. Another example is the multi-supply die-stacked sensor platform in [5], which processor's cores operate at ultra-low voltage supply for power reduction, whereas other modules such as radios, sensors, etc. are powered by a 3.6V battery. This necessitates wide-range level shifters for communicating between the processor cores and other higher-voltage modules. Therefore, level shifters have increasingly become one of the major concerns, especially in aggressively voltage-scaled systems. Recently reported low-voltage level shifters [15]-[22] suffer from the trade-off between power, area, delay, and reliability. Previously proposed cross-coupled level converters reduce the contention between very-strong pull-up and weak pull-down networks at the expense of large area and slow conversion speed, whereas recently introduced current mirror level shifters eliminate static power at the cost of high delay and area overhead. Therefore, a new area-efficient and low-voltage level shifters with fast and energy-efficient operations is required.

In this chapter, we propose an area and energy efficient level shifter for wide-range level conversion. The proposed level shifter exploits a novel reduced-swing buffer design to achieve low static power consumption while a pass transistor enhances the speed of the fall transition so that the conversion delay can be significantly improved. In addition, the proposed level shifter has the smallest area compared to the previous ultra-low voltage level shifters [15]-[22]. The rest of the chapter consists of the following. Section 4.2 addresses major drawbacks of the recently introduced level shifters. Section 4.3 presents the proposed level shifter with extensive simulation results. Measurement results are explained in Section 4.4, and Section 4.5 concludes the chapter.

4.2. Static Power and Delay Issues in Prior Arts

As discussed in Chapter 2, the conventional current mirror level shifter avoids the contention in the cross-coupled level converters by using a current mirror instead of the cross-coupled structure. However, the static current for maintaining the mirrored current results in large standby power when input data consistently stay at the logic ‘high’ level. The Wilson current mirror level shifter (WCMLS) [18] as shown in Figure 4.1 uses the feedback transistor M2 to prevent the static current. When the static current is cut off, the voltage swing at node n1 is reduced as simulated in Figure 4.2; this results in high static current at I2. The speed of the fall transition also deteriorates drastically due to the input inverter I1 and the charge sharing from node n2 to n3 via M2. The main goal of this work is to address the static power and delay issues in WCMLS for achieving fast and energy-efficient voltage conversions while improving area efficiency.

Figure 4.1: Wilson current mirror level shifter (WCMLS) [18].

Figure 4.2: Simulated behavior of WCMLS showing the reduced voltage swing and slow fall transition issues.

4.3. Proposed Level Shifter

Figure 4.3 illustrates the schematic of the proposed level shifter for wide-range voltage conversion from deep subthreshold to above-threshold voltages. The key features of the proposed level shifter are highlighted in Figure 4.3. As shown in Figure 4.1, the high static current flows at I2 due to the reduced swing n1. The novel reduced-swing buffer (M6-M11) suppresses the high static current through M8 by stacking a diode-connected transistor (M7) when the output is high. M9 recovers the full voltage swing at node n3 and further speeds up the fall transition. In addition, the proposed level shifter removes the input inverter and uses only one pass transistor (M3) for the fall transition so that the fall transition speed improves significantly. The feedback transistor (M1), added between M2 and ground, prevents the high static current in the current mirror during the high output and avoids the charge sharing problem in WCMLS [18].

Figure 4.3: Proposed level shifter with a reduced-swing buffer for eliminating the high static current at the output buffer and a pass transistor for speeding up the fall transition.

Figure 4.4 shows the operation of the proposed level shifter for L→H transition. When IN goes high, M2 is turned on to generate the mirror current through M5. The mirrored current charges n1, then n3 is discharged through M6, and the output goes high. The discharged n3 turns off M1 to cut the static current through M2 and M4; this leads to the voltage swing reduction at node n1. With the aid of the diode-connected transistor M7 in the reduced-swing buffer, the voltage swing at node n2 is also reduced as same as the voltage swing at node n1 as shown in the simulated behavior of the proposed level shifter (Figure 4.5). Therefore, the high static current flowing through M8 is eliminated, and the proposed level shifter obtains low standby power.

Figure 4.4: Operation details of the proposed level shifter for L→H transition.

Figure 4.5: The proposed reduced-swing buffer design creates a voltage reduction at node n2 as same as the voltage drop at node n1 for preventing the high static current at the output buffer.

Figure 4.6 shows the operation of the proposed level shifter for H→L transition. M2 is switched off to disable the mirror current, and the pass transistor M3 is turned on for quickly discharging n1. Then, n3 is fully charged to VDDH with the aid of M9 in the reduced-swing buffer, and the output goes low. Figure 4.7 compares the simulated behaviors of the proposed level shifter and WCMLS. The zoom-in waveforms highlight the significantly reduced fall transition delay of the proposed level shifter. With the use of the pass transistor and the aid of M9, the fall transition delay of the proposed level shifter is significantly improved compared to WCMLS.

Figure 4.6: Operation details of the proposed level shifter for H→L transition.

Figure 4.7: With the use of the pass transistor and the aid of M9, the fall transition delay of the proposed LS is significantly improved compared to WCMLS.

Table 4.1 shows the 2000-point Monte Carlo simulation results for the transition delay of the proposed level shifter and WCMLS when converting from 0.3 V to 1.1 V. The proposed level shifter achieves 3.3× smaller mean delay with less variation than WCMLS.

Table 4.1: 2000-point Monte Carlo simulation results for the transition delay.

	WCMLS	Proposed Level Shifter
Normalized Mean Delay (μ)	1.00	0.30
Normalized Standard Deviation (σ)	0.50	0.10
Variation (σ/μ)	50.0%	33.3%

Temperature: 27°C

N = 2000 points

VDDL = 0.3 V

VDDH = 1.1 V

Normalized mean delay and standard deviation: ratio normalized by WCMLS's delay

4.4. Measurement Results and Comparisons

The proposed level shifter and WCMLS [18] were implemented in a 65 nm CMOS test chip for comparisons. The microphotograph of the test chip and the layout of the proposed level shifter are depicted in Figure 4.8. The power test circuit is implemented to accurately measure the power of the level shifters without the interference of the power pads, whereas the delay test circuit is employed to measure the delay of the level shifters. Measurement results demonstrate that the proposed level shifter can convert from the deep subthreshold voltages as low as 100 mV to the above-threshold voltage of 1.2 V. Figure 4.9 shows the measured waveform of the proposed level shifter when converting from 200 mV to 1.2 V.

Figure 4.8: Micrograph of the test chip in 65nm and the layout of the level shifter.

Figure 4.9: Measured waveform of the proposed level shifter ($V_{DDL}=0.2V$, $V_{DDH}=1.2V$).

Figure 4.10: Measured delay versus V_{DDL} ($V_{DDH}=1.2V$).

Figure 4.10 shows the measured delay of WCMLS and the proposed level shifter when sweeping VDDL from 0.3 V to 1.0 V and VDDH = 1.2V. With the use of the pass transistor and the aid of M9, the proposed level shifter exhibits 2.3× faster delay than WCMLS when converting from 0.3 V to 1.2 V. When VDDL = 0.6 V - 1.0 V, the proposed level shifter shows up to 2.7× delay improvement compared to WCMLS.

Figure 4.11 exhibits the measured leakage power of the two level shifters versus VDDL at VDDH = 1.2 V. From the leakage power measurement results, the proposed level shifter shows the maximum leakage reduction of 16.3× compared to WCMLS when VDDL = 0.6 V. The leakage improvement is achieved by the aid of the proposed reduced-swing buffer design.

Figure 4.11: Measured leakage power versus VDDL (VDDH=1.2V).

Figure 4.12 and Figure 4.13 show the measured total power and energy per transition of the two level shifters over various VDDL values when $VDDH = 1.2\text{ V}$ and the input frequency $f_{IN} = 1\text{ MHz}$. By exploiting the reduced-swing buffer design and the pass transistor for speeding up the fall transition, the proposed level shifter has shorter transition time than WCMLS without extra transistors. Thus, the proposed level shifter consumes less switching power and energy. The power measurement demonstrates that the proposed level shifter has $5.3\times$ and $8.5\times$ lower power versus WCMLS at $VDDL = 0.7\text{ V}$ and $VDDL = 1.0\text{ V}$, respectively. Regarding the energy per transition, the proposed level shifter exhibits switching energy improvements of $4.5\times$ and $8.5\times$ over WCMLS at $VDDL = 0.3\text{ V}$ and $VDDL = 0.8\text{ V}$, respectively.

Figure 4.12: Measured total power versus VDDL ($VDDH=1.2\text{ V}$).

Figure 4.13: Measured energy per transition versus VDDL (VDDH=1.2V).

Table 4.2 compares the proposed level shifter with the recently reported ultra-low voltage level shifters [16]-[22]. With the smallest number of transistors as in [18] [21] and the smallest area among all the compared state-of-the-art ultra-low voltage level shifters [16]-[22], the proposed level shifter provides the highest level shifting speed. Regarding energy consumption per transition, the proposed level shifter shows the minimum switching energy compared to the level shifters in [17]-[20]. The level shifters in [16] [21]-[22] have lower switching energy than the proposed level shifter, but it comes at the expense of larger delays, areas [16] [21]-[22], and static power [16]. The proposed level shifter obtains lower standby power vs. the level shifters in [16] [18]. Compared to [17] [19]-[22], the proposed level shifter has higher leakage power. One reason is that [17][19][22] were fabricated in much older technologies. Another reason for the high leakage power of the proposed level shifter is the difference between the voltage swing at node n1 and n2. Due to process variations, the voltage swing at node n1 and n2 are not relatively close as simulated. It leads to considerable leakage at the output buffer. One possible solution is to analyze the effect of process variations on the voltage reduction at node n1 caused by the feedback transistor M1 and the reduced swing at node n2 due to the diode-connected transistor M7 through extensive Monte

Carlo simulations. Thus, a better sizing strategy could be achieved for improving the robustness of the similarity between the voltage swing at node n1 and n2 over the process variations, significantly reducing leakage power. The level shifter in [17] shows the lowest static power among all of the compared level shifters. However, it comes at the price of large delay, switching energy, and area. The level shifters in [19]-[22] also have lower static powers compared to the proposed level shifter, but they have slower speeds, larger areas [19]-[22], and higher switching energy [19]-[20].

Table 4.2: Comparisons of the proposed level shifter and recently reported level shifters.

Parameters	Proposed Level Shifter (This work)	TVLSI 2015 [16] <i>*Post layout</i>	TCAS-II 2017 [17]	TCAS-II 2010 [18] <i>*Re-implemented</i>	JSSC 2012 [19]	TCAS-I 2015 [20]	TCAS-II 2016 [21]	TCAS-I 2017 [22]
Technology	65nm	90nm	180nm	65nm	350nm	180nm	65nm	180nm
Conversion Range	0.1V - 1.2V	0.1V - 1V	0.1V - 1.8V	0.1V - 1.2V	0.23V - 3V	0.21 - 3.3V	0.1V - 1.2V	0.33V - 1.8V
Type	Current mirror	Cross coupled	Cross coupled	Current mirror	Current mirror	Current mirror	Current mirror	Current mirror
Strategy	Reduced-swing buffer and pass transistor	Self-adapting pull-up network	Self-adapting pull-up network	Feedback control	Logic error correction	Input-controlled diode chain	Self-controlled current limiter	Level-shifting capacitor
Transistor Count	11	15	14	11	16	18	11	13
Delay (ns) @VDDL	7.5 @0.3V	16.6 @0.2V	31.7 @0.4V	17.5 @0.3V	10000 @0.4V	186.3 @0.3V	13.7 @0.2V	29 @0.4V
Energy per Transition (fJ) @VDDL - f_{IN}	123.8, 103.2 @0.3V, 0.4V 1MHz	77 @0.2V-1MHz	173 @0.4V-0.1MHz	552 @0.3V-1MHz	5800 @0.4V-0.01MHz	954 @0.3V-0.1MHz	90.9 @0.2V-1MHz	61.5 @0.4V-0.5Mhz
Leakage Power (nW) @VDDL	2.64 @0.3V	8.7 @0.2V	0.055 @0.4V	20.4 @0.3V	0.23 @0.4V	0.97 @0.3V	1.24 @0.2V	0.33 @0.4V
Cell Area (μm^2)	7.45	37.3	108.8	9.94	1880	153.01	31.3	229.5

By utilizing the reduced-swing buffer design for preventing the high static current, the proposed level shifter significantly reduces the standby power compared to WCMLS [18]. In addition, the use of the pass transistor considerably shortens the transition delay and minimizes the switching energy. Compared to the recently introduced ultra-low voltage LSs [16]-[22], the proposed level shifter has the highest level shifting speed with the smallest number of transistors and the smallest area.

4.5. Conclusion

In this chapter, we presented a novel fast and energy-efficient level shifter for wide-range voltage conversion from the deep subthreshold voltage as low as 100mV to the above-threshold voltage of 1.2V. By exploiting the reduced-swing buffer design for eliminating the high leakage current and the pass transistor for speeding up the fall transition, the proposed level shifter significantly improves the conversion speed and reduces static power consumption. Measurement results from a test chip fabricated in 65 nm CMOS technology demonstrate that the proposed level shifter achieves the maximum leakage and delay reductions of $16.3\times$ and $2.7\times$ compared to WCMLS [18]. The proposed level shifter also exhibits the maximum switching energy improvement of $8.5\times$. In addition to the power and speed improvements, the proposed level shifter occupies only $7.45\text{ }\mu\text{m}^2$ which is the smallest area among all the compared state-of-the-art ultra-low voltage level shifters [16]-[22]. Therefore, the proposed level shifter is applicable to many low-power digital systems where multiple aggressively scaled voltage domains are employed for power and energy efficiency.

Chapter 5

Low-Power Area-Efficient Gesture Recognition System for Smart Devices

5.1. Introduction

Recent demand for intelligent human-machine interactions has led to the evolution of smart wearable devices, especially for gesture recognition. One of the most popular techniques is capacitive touchscreens [23], but touch-based methods require a large display size for applying gestures, making it inapplicable for wearable mobile devices. On the other hand, touchless gesture recognition using sound [24] or infrared [25] can provide compact and intuitive features with ambient light insensitivity. However, the complicated analog front-end preprocessing for the infrared signals [25] causes large area overhead, while the required excitation source and sophisticated noise filtering for the echo ultrasonic signals [24] induce high power consumption and area overhead. Moreover, electromyography (EMG) is also exploited for achieving low-latency and accurate gesture recognition in [29]. Nevertheless, it also suffers from a large device size (850mm^2) and high power consumption (189.2mW) due to the employment of artificial neural networks. In addition to sound, infrared, and EMG, gesture recognition systems [26]-[28] using image sensors have also been widely proposed. However, conventional vision systems for gesture recognition typically endure excessive power and area overhead due to large memory sizes and sophisticated image processing algorithms such as the convolutional neural network (CNN). The vision chip in [26] can recognize seven gestures at a high frame rate of $>1000\text{fps}$ by utilizing a reconfigurable processing element array processor and self-organizing map (SOM) neural network. Nevertheless, it induces excessive power consumption (630mW) and large chip size (82.3mm^2). The gesture recognition system in [27] accurately enables real-time hand-depth sensing and hand tracking by employing a stereo matching technique with CNN-

based feature extraction cores, but it also consumes high power (9.02mW) with a large chip size of 16mm². The embedded system in [28] implements an effective CNN-based architecture on the IBM TrueNorth chip for obtaining a high gesture recognition accuracy. However, the deployment of CNN leads to excessive power dissipation (169mW) while the use of the TrueNorth chip on the NS1e development board results in a large system size (8625mm²). These power and area overhead limit their applications for IoT and wearable devices in which power and area budgets are extremely critical because of their small form-factor where only a limited-size battery is allowed.

This chapter presents a low-power, area-efficient, and accurate real-time gesture recognition system for smart IoT and wearable devices. The proposed system achieves low-power and area-efficient gesture recognition by utilizing an efficient low-memory peak-based classification engine and an on-chip low-resolution low-power image sensor. In addition, a dual-core feature extraction architecture removes fixed-pattern noises from the on-chip low-power image sensor for improving the recognition accuracy and exploits parallelism for reducing the processing time. Thus, the system obtains real-time gesture recognition with a high recognition accuracy and low latency. The rest of this chapter consists of the following. In Section 5.2, we describe the proposed gesture recognition system with detailed system architecture, classification model, algorithm flow, and architecture features including the peak-based gesture classification engine, the feature extraction cores, and the on-chip image sensor. Test chip implementation and measurement results are explained in Section 5.3, followed by conclusions in Section 5.4.

Figure 5.1: Overall architecture of the proposed gesture recognition system.

5.2. Proposed Gesture Recognition System

5.2.1. System Architecture

Figure 5.1 shows the overall architecture of the proposed gesture recognition system for motion hand-gesture recognition that consists of an on-chip low-resolution low-power image sensor and a low-power and a memory-reduced peak-based digital signal processor (DSP). The on-chip image sensor contains a 32×32 pixel array, an R2R DAC, a row decoder, a timing generator, and parallel-input-serial-output (PISO)

registers. The image sensor utilizes several power reduction techniques including pulse-width modulation (PWM) [31-33], comparator gating, and an R2R-type DAC for achieving low-power near-threshold image capturing. The low-power DSP detects motion hand gestures, extracts image features and performs gesture recognition. It consists of a low-memory peak-based gesture classification engine (PGCE), a motion detection unit (MDU), and a top controller. The motion detection unit with a pixel memory of 1KB, pixel accumulator, and digital comparators performs pixel-change detection and accumulation to determine if a motion hand gesture is detected. The PGCE contains two parallel feature extraction cores (FECs) and an efficient motion gesture classification unit (MGCU). The FEC's local memories of 2KBs save two image frames of a motion gesture after a motion is detected. The row-column (RC) accumulation unit performs RC summing for peak detection, whereas the 2-way parallel peak detection processing elements (PDPEs) identify RC peaks and extract necessary information for motion gesture recognition in the MGCU involving gesture type and direction estimations based on the RC peaks' information. The feature extraction operations are handled by their local control unit, whereas the top controller controls the whole operation of the DSP. The algorithm flow of the whole system as shown in Figure 5.2 is explained in the following sub-section.

5.2.2. System Algorithm Flow

Figure 5.2 explains the algorithm of the whole gesture recognition system for motion hand-gesture recognition. When the system is powered up, the system continuously checks the video data from the on-chip image sensor for motion detection. If a hand gesture is moving, the motion is detected. The top controller saves the next two frames of the hand gesture images into the two frame memories in the FECs. After that, the RC accumulation unit performs RC summation while eliminating the fix-pattern noises. The RC summation results are stored in the RC sum buffers. Next, the 2-way parallel peak detection processing elements execute peak detection operations and send the RC peaks' amplitudes and coordinates to the classification unit. Finally, the classification unit estimates the gesture types and directions using the extracted coordinates and amplitudes. The system outputs the recognition result and returns to the initial stage for detecting the next gestures. The system model for motion gesture classification is described in the following sub-section.

Figure 5.2: Algorithm flow of the system.

5.2.3. System Classification Model

Figure 5.3 illustrates the fundamentals of the classification model utilizing a 3D feature vector based on the RC peaks' amplitudes and coordinates. From extensive simulations, the changes in RC peaks while moving the hand gestures are observed as follows. The vertical gesture type's column peaks are larger than row peaks, whereas the horizontal type's row peaks show larger amplitudes than that of column peaks. On the other hand, the diagonal gesture type shows the relatively identical RC peaks. Regarding gesture directions, the coordinates of the RC peaks correspondingly changes with the moving hand gestures. These observations construct a 3D feature vector $C = [C_T, C_{UD}, C_{LR}]$ for gesture recognition utilizing the RC peaks shown in Figure 5.3.

Figure 5.3: The fundamentals of the system classification model based on a 3D feature vector C utilizing the RC peaks' amplitudes and coordinates.

Figure 5.4 (a) and (b) explains the classification tree and the 3D feature space of the peak-based gesture recognition model, respectively. The type coefficient C_T classifies three gesture types including vertical, diagonal, and horizontal hand-gesture types. In this work, the C_T value is estimated through off-chip training. Once C_T tells the type of the gesture, C_{LR} and C_{UD} determine the final gesture based upon the classification tree in Figure 5.4 (a). For example, if $C_T \geq T_{th}$ and $C_{UD} \geq 1$, the gesture is classified as a horizontal type moving up.

T_{th} : threshold level for gesture type selection obtained from training

(a)

(b)

Figure 5.4: System classification model including the (a) classification tree and (b) 3D feature space for gesture recognition.

By utilizing the 3D feature space as shown in Figure 5.4 (b) for gesture recognition, the peak-based classification engine can recognize up to 8 motion hand gestures including the three gesture types with four different directions. The efficiency of the gesture classification model allows the system to employ a low-resolution low-power image sensor and a low-memory feature extraction architecture for power and area reduction.

Figure 5.5: Imager sensor implementation.

5.2.4. Architecture Features

5.2.4.1. On-Chip Low-Resolution Low-Power Image Sensor

The on-chip low-power image sensor consists of five main blocks as shown in Figure 5.5: a 32×32 pixel array, an R2R DAC, a row decoder, parallel-input-serial-output (PISO) registers, and a timing generator. A pixel employs a 5-T differential-pair type comparator which is biased to achieve less than 1 nA current and gated after an integration period through V_{bias} for power reduction. To generate the reference voltage V_{ramp} for the comparator, an R2R type DAC is adopted because it does not require complex circuit implementation (only resistors) while guaranteeing rail-to-rail output

swing even at extremely low supply voltages. The row decoder decodes signals from the timing generator and provides control signals for a selected row. The PISO registers store parallel data from the selected row and sequentially transfer the data to the DSP.

Figure 5.6: Timing diagram of the imager sensor.

Figure 5.6 shows the detailed pulse-width-modulation readout operation of the pixel. The photodiode voltage (V_{pd}) of the selected row is pre-charged to V_{DD} before the integration period. During the integration operation, V_{pd} , which gradually decreases in proportion to the intensity of light, is compared with the generated reference voltage (V_{ramp}). When V_{ramp} and V_{pd} intersect, the bit line is pulled up to V_{DD} and the latches in each column store the counter value (Counter [0:7]). Since the intersecting time is proportional to the intensity of the light, the stored counter value at that moment represents the pixel image. After the integration period, the PISO registers start data transmission to the DSP. By exploiting the small-array size of 32×32 , reconfigurable biasing and comparator gating techniques and the adopted R2R DAC, the on-chip CMOS image sensor achieves area-efficient low-power near-threshold image capturing.

5.2.4.2. Dual-Core Parallel Feature Extraction Architecture

Figure 5.7 and Figure 5.8 show the dual-core parallel feature extraction architecture with the detailed RC accumulation and peak detection operations, respectively, which performs digital comparisons and updates the RC peaks' amplitudes and coordinates for motion hand-gesture recognition.

5.2.4.2.1. Fixed-Pattern-Noise Elimination in RC Accumulation

After a motion is detected, the next two frames are saved in the local frame memories, and the feature extraction cores are switched to the RC accumulation stage for calculating the RC sums. To eliminate the fixed-pattern noises from the low-power low-resolution image sensor, the pixel data of the previous frame (background) stored in the pixel memory is subtracted from that of the current frame before accumulating as depicted in Figure 5.7. Note that the background frame is reconfigurable and it is automatically updated whenever the recognition is done. Then, the FPNF pixel data of each row or column are summed up and stored in four RC sum buffers for the peak detection in the PDPEs.

Figure 5.7: Fixed-pattern-noise-free RC accumulation.

5.2.4.2.2. Parallel Peak Detection Processing Elements (PDPEs)

Figure 5.8 describes the parallel peak detection and extraction stage of the feature extraction cores with the detailed peak detection operations in the PDPEs. After the RC accumulation stage is finished and the RC sum data are saved in the four RC 32-sum buffers, the two 2-way parallel PDPEs start performing peak detections. The PDPEs parallelly slide digital comparators across these four buffers to detect the RC peak positions while updating the RC peaks' amplitudes and coordinates accordingly. After 32 clock cycles, the peak detection operation is done. The RC peaks' amplitudes ($R_{pk, fr1}$, $R_{pk, fr2}$, $C_{pk, fr1}$, and $C_{pk, fr2}$) and coordinates ($PC_{r, fr1}$, $PC_{r, fr2}$, $PC_{c, fr1}$, and $PC_{c, fr2}$) are detected and extracted for the motion gesture recognition. The fixed-pattern-noise-free characteristic of the feature extraction architecture improves the accuracy of the system while the parallel PDPEs reduce the peak detection latency by $4\times$.

Figure 5.8: Parallel peak detection and extraction operation.

5.2.4.3. Motion Gesture Classification Unit (MGCU)

Figure 5.9 shows the circuit implementation for gesture type estimation in the MGCU. Two digital comparator types including T_{th} -time-greater and T_{th} -time-less comparators are utilized for the gesture type estimation based on the first level of the classification tree in Figure 5.4 (a). The detected row peaks' amplitudes ($R_{pk,fr1}$, $R_{pk,fr2}$) are compared with that of column peaks ($C_{pk,fr1}$, $C_{pk,fr2}$) with a coefficient of T_{th} for estimating the gesture types including horizontal, vertical, and diagonal. If the column peaks of the stored frames are T_{th} times larger than that of the row peaks, the motion gesture type is vertical, whereas a horizontal type is determined when the row peaks are T_{th} times greater than the column peaks. If the row peaks are comparable to the column peaks within the range of $1/T_{th}$ to T_{th} , the gesture type is diagonal.

Figure 5.9: Circuit implementation for gesture type estimation.

The circuit implementation for gesture direction estimation in the MGCU is shown in Figure 5.10. The circuit exploits magnitude comparators for determining the directions of the motion gestures based on the second and third levels of the classification tree. The results of the comparison between the extracted coordinates of the column peaks in frame 1 ($PC_{c,fr1}$) and frame 2 ($PC_{c,fr2}$) determine the left-right direction of the detected vertical gesture. Likewise, the comparison between the row peaks' coordinates of frame 1 ($PC_{r,fr1}$) and frame 2 ($PC_{r,fr2}$) shows the up-down direction of the horizontal gesture. On the other hand, the diagonal gesture type requires both these two comparison results to estimate their combinational directions (up-right, up-left, down-right, down-left). Hence, the comparator-based MGCU enables the proposed system to identify eight directional motion hand gestures accurately.

Figure 5.10: Circuit implementation for gesture direction estimation.

5.3. Implementation and Measurement Results

5.3.1. Test Chip Implementation and Measurement Setup

The proposed gesture recognition system is fabricated in 65nm CMOS LP technology, as shown in Figure 5.11. The test chip contains an on-chip image sensor with a 32×32 pixel array, a motion detection unit, two feature extraction cores, a classification unit, and a top controller. A PCB test board as shown in Figure 5.12 is designed and fabricated with the onboard QFN80-packaged test chip and external lens for testing. The system measurement setup for the test chip is shown in Figure 5.13. The test chip with the lens on the PCB test board is connected with Xilinx FPGA Zed-board for communication with a VGA monitor, displaying the real-time videos captured from the on-chip image sensor. DC power supply provides voltage supplies for the test chip, whereas the function generator operates as the external clock for the image sensor. The outputs of the test chip are readout to the logic analyzer and oscilloscope for testing.

Figure 5.11: Test chip microphotograph and performance summary.

Figure 5.12: The PCB test board including the onboard QFN80-packaged test chip with an external lens for testing.

Figure 5.13: System measurement setup for the test chip with FPGA, VGA Monitor, Logic Analyzer, Oscilloscope, Function Generator, and DC Power supply.

The test chip characteristics are summarized in Figure 5.11. The dynamic range of the low-power 32×32 image sensor is around 48 dB with the pixel size of $10 \times 10 \mu\text{m}^2$ and the DAC resolution of 8 bits. Due to the design of the 12.5%-duty-cycle horizontal reference pulse (HREF) in the image sensor as shown in Figure 5.14, the frame rate of 30fps is achieved at a higher clock frequency (PCLK) of 250 KHz. The supply voltage of the DSP can be scaled down to 0.8 V at 30fps and 250 KHz, whereas the image sensor is fully functional down to 0.5V. By utilizing the 1K-pixel image sensor and low-memory peak-based gesture classification engine, the on-chip memory is significantly reduced to only 3.2KB. Thus, the chip area is considerably minimized to 1.78mm^2 . With a low-memory DSP and small-array-size image sensor employing several power reduction techniques, the total power of the system is only $137 \mu\text{W}$ when processing hand gestures at 30fps. As shown in Figure 5.15, the MDU and the PGCE dominate the total power of the system due to the significant occupying of the pixel memory and local frame memories in MDU and PGCE, respectively. Thanks to several power reduction techniques, the image sensor contributes to only 0.9% total power of the gesture recognition system. Regarding power types, the dynamic power dominates the total power of the system with 98.18%, whereas the leakage contributes only 1.82% of the total power.

Figure 5.14: Captured output waveform of the image sensor. With the 12.5%-duty-cycle HREF, the sensor achieves the frame rate of 30fps (VSYNC) at 250 KHz.

Figure 5.15: System power breakdown by modules and types.

5.3.2. Low-Power Image Capture

Figure 5.16 shows the dynamic range of the on-chip low-power image sensor at 30fps. The dynamic range of the sensor is about 48dB. The dynamic range is limited and reduced when increasing the frame rate since the chip is not fabricated in a specialized CMOS image sensor technology, but a normal CMOS technology as shown in Figure 5.17. Thanks to the efficient motion gesture classification engine, the difference between the hand gesture and the background is still large enough at 30fps for real-time gesture recognition in the DSP. This is because the peak-based motion gesture classification engine does not require clear details of the hand regions. Figure 5.18 shows 32×32 raw hand-gesture images captured by the low-power on-chip image

sensor of the test chip at 30fps. The high efficiency of the motion gesture classification engine allows the raw image data to be directly transferred to the DSP.

Figure 5.16: Measured dynamic range of the image sensor at 30fps.

Figure 5.17: Layout of the sensor pixel in a standard 65nm CMOS.

Figure 5.18: Four 32×32 raw hand-gesture images captured by the on-chip low-power image sensor at 30fps.

Figure 5.19 shows the measured power consumption of the image sensor versus the supply voltage at 15fps and 30fps. The analog parts including the DAC and the pixel array dominate the total power consumption of the image sensor. By utilizing several power reduction techniques in the analog parts as well as employing the digital circuits for the row decoder, timing generator, and PISO registers, the image sensor achieves low-power image capturing with the total power of $1.19\mu\text{W}$ at 0.5V and 30fps.

Figure 5.19: Measured power of the image sensor versus the supply voltage at 15fps and 30fps.

5.3.3. Gesture Type Processing and Recognition

Figure 5.20 describes the detailed feature extraction processing and recognition results of the gesture types. The first horizontal-type gesture has the higher row peak R_{pk} of 3173 than the column peak of 1086, obtaining a type coefficient C_T of 2.92 which is greater than the threshold level T_{th} of 1.9 achieved through training. Thus, the accurate recognition result of the horizontal type is achieved based upon the classification tree in Figure 5.4 (a). In contrast, the vertical gesture type has the higher column peak of 3078 compared to the row peak of 1387, which results in the C_T of $0.45 < 1/T_{th}$ (i.e., 0.53) achieving the correct recognition result of the vertical type. In addition, the RC peaks of the diagonal types 1 and 2 are also extracted and accurately identified with the coefficients C_T of 1.1 and 0.84, respectively, based on the system classification tree in Figure 5.4 (a). Figure 5.21 shows other sample captured hand-gesture types with their corresponding recognition results.

Figure 5.20: Captured gesture types with extracted peaks and type recognition results.

Figure 5.21: Sample captured hand-gesture-type images with their corresponding recognition results.

5.3.4. Motion Hand Gesture Processing and Recognition

Figure 5.22 describes the detailed processing of a captured moving horizontal hand gesture in the FECs and its direction recognition result. As explained in the system algorithm flow as shown in Figure 5.3, two frames (i.e., frame 1 and frame 2) of a moving hand gesture are saved for feature extractions. Before calculating the RC sums for detecting RC peaks, the previous frame (i.e., background) is subtracted from frame 1 and frame 2 for removing the fixed-pattern noises. Then, two feature extraction cores calculate the RC sums and detect the RC peaks' amplitudes and coordinates for estimating the gesture type and directions. The horizontal motion hand-gesture, as shown in Figure 5.22, exhibits the correct gesture-type coefficients C_T of 2.47 and 2.44 in frame 1 and frame 2, respectively. The extracted row-peak coordinate of frame 1 ($PC_{r,fr1} = 24$) is greater than that of frame 2 ($PC_{r,fr2} = 7$), resulting in the up-down

coefficient C_{UD} of $3.4 > 1$, which identifies the accurate direction of the horizontal moving up gesture based upon the classification tree in Figure 5.4 (a). Similarly, the other seven different motion hand gestures including vertical moving towards right/ left, horizontal moving down, and diagonal moving up-right/ up-left/ down-right/ down-left gestures as shown in Figure 5.23 are captured and accurately recognized using the extracted RC peaks' amplitudes and coordinates.

Figure 5.22: Detailed processing of a captured motion gesture and its recognition result.

By utilizing the efficient peak-based motion gesture recognition engine with the fixed-pattern-noise-free feature, the proposed system achieves the recognition accuracy of 90.6 % for eight different motion hand gestures as shown in Figure 5.23.

Figure 5.23: Sample captured eight motion hand gestures with their corresponding recognition results.

5.3.5. Performance and Comparison

Figure 5.24 shows the latency breakdown of the proposed motion gesture recognition system at 250 KHz. By exploiting the parallelism for the feature extraction architecture, the proposed system achieves real-time gesture recognition operation at 30fps with the total processing time of 4.228ms including the RC accumulation, peak detection, and gesture classification.

Figure 5.25 shows the measured total power of the proposed system including the 0.5-V on-chip image sensor when sweeping the supply voltage of DSP from 0.8V to 1.2V at 30fps. With only 3.2KB on-chip memory and a 1K-pixel sensor utilizing several power reduction techniques, the system consumes the total power of only 137.0 μ W at the DSP supply voltage of 0.8V while operating the image sensor at 0.5V and 30fps for real-time gesture recognition.

Figure 5.24: System processing time breakdown.

Figure 5.25: Measured total power of the system at 30fps and 250 KHz versus the supply voltage of the DSP.

Table 5.1 summarizes the measurement comparison of the proposed system and recently introduced gesture recognition systems [23]-[29]. By exploiting an on-chip 1K-pixel image sensor and an efficient peak-based gesture classification engine with less memory (3.2KB), the proposed system has the smallest chip area of 1.78mm^2 compared to the previously reported gesture recognition ASIC systems [23]-[27]. The vision chip

in [26] has the largest chip area due to the domination of the three reconfigurable array processors, self-organized map neural network, and the 256×256 pixel array. The other two embedded systems [28]-[29] shows much larger areas because of their external peripherals for communication with off-chip sensors. Regarding total power consumption, the proposed system with only 3.2KB on-chip memory also achieves the lowest power of 137 μ W among all the recently introduced systems [23]-[29]. The vision chip in [26] can recognize seven different hand gestures, but it consumes the highest power of 630mW due to the large pixel array size, high ADC resolution, and large processing element array. However, it exhibits the smallest processing time of ~0.2ms with multiple recognition features such as face detection and horizontal estimation. The other systems have larger power consumption, but they provide more complex features for wearables and IoT such as 3D hand depth tracking [23]-[24] [27] and more number of gestures [28]-[29]..

Table 5.1. Comparisons of the proposed system and recently reported systems.

	This Work	[27] ISSCC 2018	[25] VLSIC 2016	[26] JSSC 2014	[24] ISSCC 2014	[23] ISSCC 2014	[28] CVPR 2017	[29] TCAS-II 2017
Type	ASIC	ASIC	ASIC	ASIC	ASIC	ASIC	Embedded	Embedded
Process/ Chip	65nm	65nm	65nm	180nm	180nm	130nm	IBM TrueNorth	ARM Cortex-M4
Sensor (On-Chip)	Image Sensor (YES)	Stereo Camera (NO)	Infrared Sensor (NO)	Image Sensor (YES)	Ultrasonic Sensor (NO)	Sensing Electrodes (NO)	DVS Camera (NO)	EMG Electrodes (NO)
Recog. Features	8 Motion Gestures	3D Tracking + Depth Sensing	8 Motion Gestures	7 Gestures + Face Det. + Hor. Est.	3D Depth Sensing	3D Depth Sensing	11 Hand Gestures	10 Hand Gestures
Area	1.78mm ²	16mm ²	8.1mm ²	82.3mm ²	4mm ²	4.2mm ²	8625mm ²	850mm ²
Accuracy/ Error	90.6%	4.3mm @20-40cm	96%	92%	0.41mm @50cm	10mm @20cm	96.5%	94%
Latency	4.228ms	30.0ms	33.3ms	~0.2ms	33.3ms	4.0ms	105.0ms	>400ms
Power	137 μ W	9.02mW	260 μ W	630mW	401 μ W	19.2mW	178.8mW	189.2mW

By utilizing the efficient low-memory peak-based gesture classification engine and the low-resolution low-power on-chip image sensor, the proposed system outperforms

other designs in terms of total power and area, making this system very well-suited for smart IoT and wearable devices where the area and power budget are extremely critical.

5.5. Conclusion

This chapter presents an accurate, area-efficient, and ultra-low power real-time gesture recognition system for smart wearable devices. The proposed system achieves area-efficient and low-power accurate gesture recognition by exploiting an efficient peak-based gesture classification engine with less memory and a low-resolution and low-power on-chip image sensor. Moreover, the feature extraction architecture eliminates fixed-pattern noises from the on-chip low-power image sensor for further enhancing the recognition accuracy and exploits parallelism for improving the recognition latency. Thus, the proposed system obtains accurate real-time gesture recognition for eight different motion hand gestures with the recognition accuracy of 90.6% and the total processing time of 4.228ms. Test chip measurement in 65nm CMOS demonstrates that the proposed system consumes 137.0 μ W for real-time gesture recognition at 30fps while occupying only 1.78mm², which achieves the smallest area and lowest power among the previously reported gesture recognition systems [23]-[29]. Therefore, the proposed system is well applicable to various ultra-low power applications such as IoT and wearable devices, where high area efficiency and ultra-low power consumption are their topmost requirements.

Chapter 6

Ultra-Low Power Low-Area Vision Chip for Gesture Recognition in Wearables

6.1. Introduction

Gesture recognition has become one of the most popular human-computer interaction techniques for smart wearable devices in recent years. The requirements for gesture recognition in wearable platforms are as follows: high area efficiency because of their small form-factor, low power consumption due to limited battery sizes, and low latency for natural interaction. However, recently proposed gesture recognition systems [23]-[29] induce large power and area overhead, which restrains their applications for wearable devices. Therefore, a low-power and area-efficient gesture recognition system is required.

Our previous vision-based system in [34] enables real-time motion hand gesture recognition with low power consumption and high area efficiency. However, the system is only able to identify eight motion hand gestures with only three gesture types, which is not a very attractive solution for smart mobile devices necessitating a large number of gestures. This chapter presents a new vision chip that further reduces area and power while accurately recognizing 24 motion hand gestures. The proposed work utilizes a novel highly-efficient outermost-edge-based algorithm for correctly identifying 24 motion hand gestures with much less memory. The accuracy is significantly enhanced with the utilization of a self-adaptive motion detector and noise-aware convolution-based feature extraction. Thus, the proposed system accomplishes accurate motion gesture recognition even with noisy gesture images from the on-chip low-power image sensor. Moreover, feature extraction cores exploit parallelisms for achieving low-latency real-time gesture recognition. The rest of the chapter consists of the following. In Section 6.2, we describe the proposed gesture recognition system with detailed

system architecture, algorithm flow, and architecture features including an adaptive-threshold motion detector, 4-way parallel feature extraction cores, 5-stage pipelined edge detection processing elements, a 5-way-parallel-read custom memory and a 32×32 on-chip image sensor. Test chip implementation and measurement results are explained in Section 6.3, followed by conclusions in Section 6.4.

Figure 6.1: Overall architecture of the proposed gesture recognition system.

6.2. Proposed Gesture Recognition System

6.2.1. Overall Architecture and Algorithm Flow

Figure 6.1 shows the overall architecture of the proposed vision system for gesture recognition that consists of an on-chip 32×32 image sensor for low-power gesture capturing and a memory-efficient adaptive-threshold digital signal processor (DSP) for low-power area-efficient accurate gesture recognition. The DSP consists of a memory-

efficient outermost-edge-based gesture recognition engine (OEGRE), an adaptive-threshold motion detector, and a top controller. The motion detector accurately detects hand motion by utilizing a threshold adaptor. The OEGRE includes a dual-core 4-way-parallel feature extraction architecture for detecting outermost edges and a recognition unit for motion hand gesture recognition. The 4-way-parallel FE architecture utilizes a 5-stage pipelined edge detection processing element (EDPE) and a 5-way-parallel-read custom memory (CM) for accelerating the feature extraction for obtaining real-time gesture recognition, whereas outermost pixel detectors identify the image boundary for saving. The top controller handles the flow of the system.

Figure 6.2: Algorithm flow of the system.

Figure 6.2 illustrates the proposed GR algorithm flow. When the system is powered on, the DSP continuously scans the video data from the image sensor until motion is detected. Once the motion is identified, the DSP stores the outermost pixels of the next two frames into the custom memory. Then, feature extraction cores perform edge detection for detecting hand-edge coordinates on the outermost pixels. Next, the proposed recognition unit uses the average edge coordinates as the detected hand positions for identifying the gesture type and the direction of the captured motion gesture. Finally, the system outputs the result and returns to the initial stage waiting for another motion hand gesture.

Figure 6.3: Six different hand gesture types identified by utilizing hand edges' positions on the outermost pixels.

6.2.2. Proposed Outermost-Edge-Based Gesture Recognition

Figure 6.3 illustrates the fundamentals of the proposed outermost-edge-based gesture recognition algorithm. The proposed algorithm recognizes six different hand gesture types by utilizing detected hand positions on the outermost pixels. The hand

positions are detected and extracted as the average hand edge coordinates on the image boundary. Each gesture type has a unique pair of detected hand positions on the outermost rows and columns. Particularly, the vertical type only shows hand edges on the two outermost rows (i.e., row 1 and row 32), whereas the horizontal type has the hand presence on the two outermost columns (i.e., column 1 and column 32). On the other hand, other four diagonal gesture types show edges on four combinations of the two outermost rows and columns as follows: 1) top-left diagonal (TLD) – (row 1, column 1), 2) top-right diagonal (TRD) – (row 1, column 32), 3) bottom-left diagonal (BLD) – (row 32, column 1), and 4) bottom-right diagonal (BRD) – (row 32, column 32).

By observing the changes in hand edge positions on the outermost pixels during the movement of the hand gestures, the proposed algorithm can recognize up to 24 different motion hand gestures involving these six gesture types as shown in Figure 6.4. Figure 6.5 illustrates the classification tree for recognizing the 24 motion hand gestures. At the top level of the classification tree, the detected hand positions on the first stored frame are used for identifying the starting gesture type. Then, at the bottom level, the motion hand gestures are recognized using the as the extracted hand positions on the second frame as well as the classification result of the starting gesture type from the top level. When a motion gesture involving two identical gesture types, the detected hand locations on the two saved frames are compared for recognizing the direction of the gesture. For example, if the motion gesture is classified as vertical left/right (L/R), the hand positions on the outermost rows of frame 1 (i.e., a, b) and frame 2 (i.e., c, d) are compared to determine whether the direction is left or right. On the other hand, the motion gesture of horizontal up/down (U/D) compares the hand positions on the outermost columns of frame 1 (i.e., a, b) and frame 2 (i.e., c, d) for identifying whether the direction is up or down. In addition, the diagonal U/D L/R motion gestures utilize the changes of the hand positions on the same row or column of the two frames for classifying their combinational directions including up left, up right, down left, and down right.

Figure 6.4: Twenty-four motion hand gestures based on outermost-edge positions.

More importantly, only the outermost pixels (i.e., 0.1 KB for each frame) are required for the motion hand gesture recognition, whereas in prior art vision-based systems [25-28] necessitate the whole pixel array for processing and classification. This substantially reduces the total memory size and the computation time for the proposed system, consequently minimizing chip area and power consumption.

Figure 6.5: Classification tree for 24 motion hand gestures based on detected hand positions on the outermost pixels.

Figure 6.6: Self-adaptive motion detector with a pixel threshold adaptor for enhancing motion gesture recognition accuracy.

6.2.3. Key Architecture Features

6.2.3.1. Self-Adaptive Motion Detector (SAMD)

Figure 6.6 illustrates the self-adaptive motion detector (SAMD) with a threshold adaptor for enhancing motion gesture recognition accuracy. When gesture-applying

environments are changed with different light conditions and gesture shapes, the contrast between the background and hand gestures is also varied, requiring the motion detector to be adapted for accurate motion detection in different environments. Therefore, we propose the SAMD that automatically adjusts to different environments for improving motion detection accuracy. The SAMD utilizes a pixel threshold adaptor for updating a pixel threshold whenever a new environment or gesture is applied. Then, the self-adapted pixel threshold P_{TH} is used for detecting if a pixel is changed compared to the background stored in a pixel memory. The SAMD accumulates the number of changed pixels and motion is detected if the number of varied pixels is significant based upon a motion threshold M_{TH} . The motion threshold is also reconfigurable for varying the distance between hand gestures and the image sensor. By utilizing the self-adaptive motion detector, the motion detection and gesture recognition accuracy of the proposed system is significantly improved.

6.2.3.2. 5-Way-Parallel-Read Custom Memory

Figure 6.7 depicts the 5-way-parallel-read custom memory for accelerating the edge detection operation. After the motion is detected, the outermost pixel detector identifies the two outermost rows (i.e., 1 and 32) and columns (i.e., 1 and 32) to store into the custom memory for edge detection. Moreover, to remove fixed pattern noises from the on-chip low-resolution low-power imager, the image data of the previous frame is deducted from that of the present frame before saving. Then, only the fixed-pattern-noise-free data of the outermost pixels is stored into the custom memory. In addition, to accelerate the feature extraction operation, the custom memory employs five 32-to-1 multiplexers in parallel at the output port as shown in Figure 6.7 for enabling five-pixel read at the same time. The use of parallelism speeds up the feature extraction operation by $5\times$ while the employment of the noise-canceling technique substantially enhances the recognition accuracy of the system.

Figure 6.7: 5-way-parallel-read custom memory for accelerating the edge detection operation.

6.2.3.3. 4-Way-Parallel Feature Extraction Architecture

Figure 6.8 (a) illustrates the 4-way-parallel convolution-based feature extraction architecture with the detailed convolution-based edge detection operation. The feature extraction cores exploit a convolution-based edge detection technique using two filters for preventing hand detection errors due to random noises sparsely occurring on the image boundary from the on-chip low-power image sensor. These 1×5 filters are obtained through extensive training in Matlab including Y and Z. The Y filter is used to detect background-to-hand edges, whereas hand-to-background edges are identified by using the Z filter. The feature extraction cores slide the Y and Z filters parallelly along the four boundaries (i.e., rows 1, 32, columns 1, and 32) of a captured frame and perform a simplified logical operation of multiplication, accumulation, and comparison for

detecting background-to-hand and hand-to-background edges. If an edge is detected, the edge location is stored for tracking the hand position and recognizing motion gestures. The 4-way-parallel feature extraction architecture further speeds up the feature extraction by 4 $\times$. On the other hand, the convolution-based edge detection technique minimizes detection errors caused by the possible random noises.

Figure 6.8: (a) 4-way-parallel convolution-based feature extraction architecture with the detailed edge detection operation and (b) the 5-stage pipelined EDPE.

Figure 6.8 (b) shows the architecture of the pipelined edge detection processing element (EDPE) for further accelerating the edge detection operation. The EDPE consists of five stages: 1) fetching, 2) activation, 3) edge detection, 4) extraction and 5)

averaging. First, 5 pixels in each outermost row or column are fetched at the same time with the aid of the 5-way-parallel-read custom memory and then, the readout data are shifted to the activation stage where the activation function is executed using the pixel threshold PTH from the threshold adaptor. Then, the edge detection operation including background-to-hand and hand-to-background detections is performed for identifying the edge locations. In the extraction stage, the detected edge positions are forwarded to the next stage for averaging. Finally, all the hand edge coordinates are obtained in 28 cycles for tracking the hand position and recognizing the motion gesture. Therefore, the speedup of the feature extraction is further achieved by utilizing the 5-stage pipelined EDPEs.

Figure 6.9: Low-power image sensor implementation.

6.2.3.3. Low-Power On-Chip Image Sensor

Since the DSP does not require the inner pixels for gesture recognition, a low-resolution on-chip imager with a digital pixel architecture and a pulse-width-modulation scheme [31]-[33] is employed for power and area reduction as shown in Figure 6.9. The sensor utilizes an in-pixel comparator to sense the time instants at which the voltage of the photodiode intersects the reference voltage. The time information (pulse width) is converted to the digital data and transferred to the DSP. This architecture minimally

uses analog circuits (only the comparator and reference generator) and is more advantageous than the analog readout architecture in power consumption and voltage scaling. One drawback of this architecture is low sensitivity due to the limited exposure time. It only operates with rolling-shutter fashion since it has no memory element in the pixel. Moreover, unlike capturing still images, continuous image capturing for motion sensing further limits the exposure time of a single pixel. To overcome this problem, the pixel is designed to be reset one cycle before the read-out period and the photodiode is exposed to light for twice as long as the conventional structure.

6.3. Test Chip Implementation Results

6.3.1. Test Chip Implementation and Measurement Setup

The proposed gesture recognition system is fabricated in 65nm CMOS GP technology. Figure 6.10 illustrates the system measurement setup with a printed circuit board (PCB) including an onboard QFN80 test chip for testing. An external lens is used for focus adjustment during testing. The test chip with the lens on the PCB communicates with Xilinx FPGA Zed-board for displaying real-time video data from the on-chip imager on the VGA monitor. The power supply provides voltage supplies for the test chip and the PCB, whereas the function generator generates the clock signal for the image sensor. The output results are sent to the logic analyzer and oscilloscope for testing. A source meter is also used for measuring current.

The test chip micrograph and performance summary are shown in Figure 6.11. The test chip includes the on-chip 32×32 image sensor, the self-adaptive motion detector, two feature extraction cores, the recognition unit, and the top controller. The frame rate of 30fps is achieved at the pixel clock (PCLK) frequency of 31.25 KHz as captured in Figure 6.12, which is significantly improved compared to the previous work in [34]. The image sensor is operational down to 0.6V, whereas the supply voltage of the DSP can be scaled down to 0.46 V for real-time gesture recognition at 30fps. By utilizing a memory-efficient gesture recognition algorithm and a low-resolution on-chip imager, the on-chip memory of the proposed system is significantly minimized to only 1.2KB. Thus, the total chip area is considerably reduced to 0.54mm^2 . In addition, the total power of the system is only $213.7\mu\text{W}$ at 30fps, which includes only $3\mu\text{W}$ dynamic power. The leakage dominates the power consumption of the system due to the fabrication in a leaky 65nm CMOS GP process. In terms of power breakdown by modules as shown in Figure

6. 13, DSP dominates the total power with 97% contribution, which the motion detector with the pixel memory size of 1KB consumes up to 65% power of the DSP and the feature extraction cores contribute 29% due to the four 5-way-parallel CMs (i.e., 0.1KB for each core).

Figure 6.10: PCB test board and system measurement setup.

Figure 6.11: Test chip micrograph and performance summary.

Figure 6.12: Captured video signals from the on-chip image sensor. The frame rate of 30fps is achieved at the pixel clock (PCLK) frequency of 31.25 KHz.

Figure 6.13: System power breakdown by modules.

6.3.2. Low Power Hand Gesture Capturing

Figure 6.14 shows the measured power consumption of the on-chip image sensor when sweeping the supply voltage from 0.6V to 1.0V at 30fps. By utilizing a low-resolution digital pixel architecture with the pulse-width-modulation scheme, the image sensor achieves low-power gesture capture with the total power of $7.4\mu\text{W}$ at 0.6V and 30fps. However, due to the fabricated leaky 65nm CMOS technology, the leakage dominates the total power of the imager. The dominance of leakage over photodiode currents also causes a lot of fixed pattern noises on the captured images.

Figure 6.15 shows several captured 32×32 images from the on-chip image sensor at 30fps when sweeping a hand from left to right. Thanks to the employment of the fixed-pattern-noise canceling technique in the custom memory and the random-noise-aware convolution-based feature extraction architecture, the proposed system can accurately recognize motion hand gestures even with the noisy gesture data from the low-power image sensor.

Figure 6.14: Measured power of the imager. Leakage dominates the total power consumption of the sensor due to the leaky fabricated CMOS technology

Figure 6.15: Captured 32×32 images when sweeping a hand from left to right at 30fps.

6.3.3. Real-Time Gesture Recognition Operation

Figure 6.16 shows the captured total latency of the proposed system for motion hand gesture recognition with the latency breakdown by operations. The high utilization of parallelism in the feature extraction architecture, which consists of the 5-way-parallel-read custom memory and the 4-way-parallel edge detection operation with 5-staged pipelined EDPEs, enables the system to achieve real-time operation with the total processing time of 1.056ms including hand edge detection in the feature extraction cores (960 μ s) and gesture classification in the recognition unit (96 μ s).

(a)

(b)

Figure 6.16: (a) Captured latency of the system with (b) the latency breakdown.

6.3.4. Motion Hand Gesture Recognition Accuracy

Figure 6.17 illustrates the detailed processing of a captured moving vertical hand gesture and its recognition result. After the motion is detected, the outermost pixels of the next two frames, which fixed-pattern noises are canceled by subtracting the pixel data of the previous frame from these frames, are stored into the custom memory for hand edge detection. As shown in Figure 6.17, due to the dominance of leakage, fixed-pattern noises are largely presented on the captured background and gesture images. By employing the noise-removal technique in the feature extraction cores, the fixed pattern noises are removed, and the saved outermost pixels do not have these noises on the background region. However, these noises are still presented in the hand regions. Thanks to the noise-aware convolution-based edge detection technique, the proposed system accurately detects hand edges on the outermost pixels and then, identifies the hand locations based upon the average edge positions as shown in Figure 6.17. Since the hands are only detected on row 1 and row 32, the hand gesture type is recognized as a vertical gesture based upon the classification tree shown in Figure 6.5. Regarding the movement of the gesture, the row-1 hand positions change from 14 to 22 and the row-32 hand locations move from 12 to 18. Thus, the direction of the motion hand gesture is identified as moving towards the right. Finally, the motion gesture is accurately recognized as a vertical gesture type moving from left to right. Similarly, other 23 motion hand gestures are correctly recognized based upon the detected hand positions on the outermost pixels.

Figure 6.17: Detailed processing of a sample captured vertical hand gesture.

Figure 6.18 shows sample captured six hand gesture types with detected hand positions and their recognition results. By utilizing the accurate outermost-edge-based motion gesture recognition algorithm with the noise-aware convolution-based feature extraction architecture, the proposed system accurately recognizes 24 motion hand gestures involving these six gesture types. When identifying ~500 hand gesture images captured by the on-chip image sensor in the real world, the average accuracy of the system for recognizing 24 motion hand gestures is ~85% as shown in Figure 6.19 and Table 6.1. The accuracy of this system is degraded because of the dominance of leakage as shown in Figure 6.14, which causes excessive noise on the gesture images from the low power imager. However, the accuracy of the system can be improved by making decisions using the dominant results based on several recognitions since the system captures multiple frames for multiple classifications in a single hand sweep.

Figure 6.18: Sample captured six hand gesture types with detected hand positions and their recognition results.

Figure 6.19: Average recognition accuracy for 24 motion hand gestures when recognizing ~500 hand gesture images. The average accuracy of the system is ~85%.

Table 6.1: List of 24 motion hand gestures.

Motion Hand Gestures	No.
TRD Moving To Horizontal	1
Diagonal Moving Up Left	2
BLD Moving To Horizontal	3
Vertical Moving To TRD	4
BLD Moving To Vertical	5
Horizontal Moving Up	6
BRD Moving To Horizontal	7
Vertical Moving To BLD	8
Vertical Moving To TLD	9
Diagonal Moving Down Right	10
Horizontal Moving To TLD	11
Vertical Moving Towards Left	12
TLD Moving To Vertical	13
Horizontal Moving To TRD	14
TLD Moving To Horizontal	15
Vertical Moving Towards Right	16
BRD Moving To Vertical	17
Diagonal Moving Up Right	18
Horizontal Moving To BRD	19
Horizontal Moving Down	20
TRD Moving To Vertical	21
Diagonal Moving Down Left	22
Horizontal Moving To BLD	23
Vertical Moving To BRD	24

6.3.5. Comparison and Discussion

Figure 6.20 shows the measured total power consumption of the proposed system versus the supply voltage of at $VDD_{Imager}=0.6V$ and 30fps. With a small pixel array and only 1.2KB on-chip memory, the system consumes the total power of 213.7 μW with only 3 μW of dynamic power at $VDD_{DSP}=0.46V$ while operating the image sensor at 0.6V and 30fps for real-time motion gesture recognition. Due to the highly leaky 65nm CMOS GP fabrication technology, leakage dominates the total power of the system.

Figure 6.20: Measured total power of the proposed system versus the supply voltage of the DSP at $VDD_{Imager} = 0.6V$ and 30fps.

Table 6.2 compares the proposed system with recently introduced gesture recognition systems [23-27] [34]. By utilizing an on-chip low-resolution image sensor and the memory-efficient (1.2KB) outermost-edge-based DSP, the proposed system obtains the smallest chip area of $0.54mm^2$ among the state-of-the-art systems for gesture recognition. The vision chip in [26] suffers from the largest area overhead due to the employment of reconfigurable array processors, neural network, and the large pixel array of 256×256 . Regarding total power consumption, the proposed system with only 1.2KB on-chip memory also achieves the lowest power of $213.7 \mu W$ compared to the recently introduced systems [23-27]. Our previous gesture recognition system in [34] has lower total power consumption due to the fabrication in a low-power 65nm process with lower leakage. Regarding dynamic power, the proposed system shows $44\times$ lower power than our work in [34]. The vision chip in [26] can recognize seven different hand gestures, but it consumes the highest power of 630mW due to the large pixel array size, high ADC resolution, and large processing element array. However, it exhibits the

fastest recognition speed. The proposed system has the second lowest recognition latency with the high utilization of parallelism in feature extraction cores.

Table 6.2: Comparisons of the proposed system and previously reported systems.

	This Work	[34] T. Yoo, ASSCC 2018	[27] S. Choi, ISSCC 2018	[25] S. Oh VLSIC 2016	[26] C. Shi, JSSC 2014	[24] R. J. P. ISSCC 2014	[23] Y. Hu, ISSCC 2014
Process	65nm GP	65nm LP	65nm	65nm	180nm	180nm	130nm
Sensor (On-Chip)	Image (Yes)	Image (Yes)	Stereo (No)	Infrared (No)	Image (Yes)	Ultrasonic (No)	Electrodes (No)
Recognition Features	24 Motion Gestures	8 Motion Hand Gestures	3D Tracking + Depth Sensing	8 Motion Gestures	7 Gestures + Face Detection	3D Depth Sensing	3D Depth Sensing
Area	0.54mm²	1.78mm ²	16mm ²	8.1mm ²	82.3mm ²	4mm ²	4.2mm ²
Accuracy/Error	85%	90.6%	4.3mm @20-40cm	96%	92%	0.41mm @50cm	10mm @20cm
Latency	1.056ms	4.228ms	30.0ms	33.3ms	~0.2ms	33.3ms	4.0ms
Total Power	213.7μW @P_{Dyn.}=3μW	137 μ W @P _{Dyn.} =134 μ W	9.02mW	260 μ W	630mW	401 μ W	19.2mW

By utilizing an ultra-low-memory (1.2KB) outermost-edge-based DSP and the low-resolution low-power on-chip image sensor, the proposed system outperforms other systems in terms of total power and area, making it very well suited for wearable devices where power and area budgets are extremely limited.

6.4. Conclusion

This chapter presents an accurate, area-efficient, and ultra-low power real-time gesture recognition system for smart wearable devices. The proposed work uses a novel highly-efficient outermost-edge-based gesture recognition algorithm for accurately recognizing 24 motion hand gestures with ultra-low memory. The accuracy is significantly enhanced with the utilization of a self-adaptive motion detector and noise-

aware convolution-based feature extraction. Thus, the proposed system accomplishes accurate motion gesture recognition with an average recognition accuracy of 85%. Furthermore, feature extraction cores highly exploit parallelisms for accelerating the recognition speed, achieving real-time gesture recognition with a low latency of 1.056ms. Test chip measurements in 65nm show that the proposed system consumes only 3- μ W dynamic power at 30fps while occupying 0.54-mm². Therefore, the proposed system is well applicable to many ultra-low power applications such as wearable devices, where ultra-low power and area efficiency are their top priorities.

Chapter 7

Conclusion and Future Works

7.1. Conclusion

The relentless advancement of process technology has tremendously brought massive performance boosts and much more integration to modern digital circuits and systems. However, this leads to excessive power consumption which results in thermal issues on silicon and significantly restricts the chip yield, reliability, and performance [4]. Thus, chip designers are required to take into considerations the power consumption at all design levels. In addition, there have been increasingly ongoing demands for hand-held devices and wireless sensor nodes. Their power budgets are extremely restricted because their small form-factors can only accommodate a limited-size battery. In other words, low-power design has become one of the most critical design constraints in digital circuits and systems.

In this thesis, we identified several critical circuit components that typically suffer from large power consumption, proposed new techniques to reduce power and improve performance as well as area efficiency, and demonstrated their effectiveness through test chip measurements. Furthermore, we addressed the high power and area issues of the state-of-the-art gesture recognition systems for smart portable devices and presented two ultra-low power and area-efficient systems for gesture recognition with test chip measurements.

FFs are fundamental building blocks in modern processors; they typically dominate the total area and power of the overall system. FFs generally consume large dynamic power in SoCs due to redundant transitions of their large number of internal clocked nodes even when there is no data activity. Many low-power FFs [7]-[12] have been recently proposed for reducing or even eliminating power penalty coming from the redundant transitions. However, they suffer from either large area penalty [7]-[8], which

is too costly since FFs typically occupy a significant amount of logic area in SoCs, or functional failures at low-voltage operations [8]-[11], which makes these FFs inapplicable for low-voltage applications. Thus, a new area-efficient and low-voltage FF that eliminates the redundant transitions for ultra-low power applications is required. In chapter 3, we proposed an extremely low-voltage and low-power single-phase-clocking redundant-transition-free flip-flop (FF), named change-sensing flip-flop (CSFF). By utilizing a local change-sensing scheme for eliminating redundant transitions of internal clocked nodes, CSFF does not consume any dynamic power when there is no data activity. CSFF saves up to 90% power dissipation at 5% data activity without additional transistors compared to the conventional transmission-gate flip-flop (TGFF). CSFF consumes only 0.138 fJ/cycle, which is 84% lower than that of TGFF, at 0.4 V and 10% activity. In addition to the significant improvement in power and energy efficiencies, CSFF also enhances performance and minimum operating voltage. The test chip measurement in 65nm demonstrates successful operations of CSFF down to 0.19 V and the delay improvement of 37% compared to TGFF in the supply voltage range of 0.4 V to 1.0 V.

Level shifters are also one of the key components in voltage-scaled VLSI systems. Digital cores in today's processors have been voltage-scaled independently, and there has also been a significant increase in the number of the digital cores in modern processors. This requires level shifting between different core voltage domains. In addition, the low-voltage circuit design has been broadly researched for ultra-low power applications, reaching as ultra-low as 230mV in a recent pipelined microprocessor [14]. This necessitates wide-range level shifters for communicating between the processor cores and other higher-voltage modules. Recently reported low-voltage level shifters [15]-[22] suffer from the trade-off between power, area, delay, and reliability. Previously proposed cross-coupled level converters reduce the contention between very-strong pull-up and weak pull-down networks at the expense of large area and slow conversion speed, whereas recently introduced current mirror level shifters eliminate static power at the cost of high delay and area overhead. Therefore, a new area-efficient and low-voltage level shifter with fast and energy-efficient operations is required. In chapter 4, we presented an ultra-low voltage level shifter with fast and energy-efficient voltage conversion from the deep subthreshold region to the superthreshold region. The proposed level shifter achieves better performance and higher energy efficiency by

addressing the reduced swing and the slow fall transition issues in prior arts. A novel reduced-swing buffer design is exploited to attain lower standby power consumption while a pass transistor is used for improving the speed of the fall transition. The proposed level shifter consists of only 11 transistors occupying $7.45 \mu\text{m}^2$, which obtains the smallest area among the state-of-the-art ultra-low voltage level shifters. Measurement results from a test chip fabricated in 65-nm CMOS technology demonstrate that the proposed level shifter shows the maximum leakage and speed improvements of $16.3\times$ and $2.7\times$ compared to the Wilson current mirror level shifter (WCMLS). The proposed level shifter also accomplishes the maximum switching energy reduction of $8.5\times$ and can convert deep subthreshold voltage as low as 100 mV to the superthreshold voltage of 1.2 V.

Gesture recognition has become one of the most popular human-machine interaction techniques for smart wearable devices in recent years. The requirements for gesture recognition in wearable platforms are as follows: high area efficiency because of their small form-factor, low power consumption due to limited battery sizes, and low latency for natural interaction. However, recently proposed gesture recognition systems [23]-[29] induce large power and area overhead, which restrains their applications for wearable devices. Therefore, an ultra-low power and area-efficient gesture recognition system-on-chip are required. In chapter 5, we proposed an accurate, area-efficient and low-power real-time gesture recognition system for smart wearable devices. This proposed work utilizes a peak-based gesture classification engine with less memory and a low-resolution and low-power on-chip image sensor for achieving high area efficiency and low-power. In addition, the feature extraction architecture removes fixed-pattern-noise from the low power on-chip image sensor for accuracy improvement and employs parallelism for recognition speed enhancement. Thus, the proposed system accomplishes accurate real-time gesture recognition for eight motion hand gestures with the recognition accuracy of 90.6% and latency of 4.228ms. Measurement results of a test chip fabricated in 65nm CMOS demonstrate that the proposed system consumes $137.0\mu\text{W}$ at 30fps while occupying only 1.78mm^2 , which achieves the lowest power and smallest area among the recently reported gesture recognition systems.

In chapter 6, with the objective of further reducing power consumption and chip area as well as adding more features to the current gesture recognition system [34], we proposed another ultra-low power gesture recognition SoC for smart wearable devices.

The proposed work exploits a novel highly-efficient outermost-edge-based gesture recognition algorithm for accurately identifying 24 motion hand gestures with ultra-low memory. The accuracy is significantly enhanced with the utilization of a self-adaptive motion detector and noise-aware convolution-based feature extraction architecture. Thus, the proposed system accomplishes accurate motion gesture recognition with an average recognition accuracy of ~85 % even with noisy gesture images from the on-chip low-power image sensor. Furthermore, feature extraction cores highly exploit parallelisms for accelerating the recognition speed, achieving real-time gesture recognition with a low latency of 1.056ms. Test chip measurements in 65nm show that the proposed system consumes only 3- μ W dynamic power at 30fps while occupying 0.54-mm², which outperforms recently reported gesture recognition systems regarding area and power, making it very well-suited for smart wearable devices.

7.2. Future Works

Based on the circuit techniques presented in this dissertation, there are further opportunities to further improve power, area efficiency, and performance in low-voltage VLSI systems such as IoT and wearable platforms. The proposed low-power CSFF [35]-[37] and ultra-low voltage LS [38] are planned to be employed in our future gesture recognition chip for further reducing power consumption and improving the performance of the overall system. Since the on-chip memory dominates the total power and area of the gesture recognition system [34], the use of the CSFF with the change-sensing scheme can significantly minimize the dynamic power consumption of the whole system especially when there is no data activity. The utilization of the FF also enables the system to operate at subthreshold regions for further reducing power consumption. On the other hand, the employment of the proposed LS could improve area efficiency and performance since the power supplies of the on-chip image sensor, and the DSP are separately scaled down, requiring level shifting between two voltage domains.

In addition, our future work is to continue on the development of the next vision chip for gesture recognition using convolution neural networks (CNN). The motivation of this future work is to utilize CNN to bring more features such as tracking and localization to the current vision chip and improve the accuracy while achieving ultra-low power and high area efficiency as well as low latency for natural interaction.

Therefore, the chip would be very well applicable to smart mobile applications such as AR/ VR devices, where power and area budgets are extremely restricted because of their small form factor and limited battery sizes.

List of Author's Publications

Patent

- [1] **Van Loi Le**, Tae-Hyoung Kim, Juhui Li, and Alan Chang, “Low power flip-flop circuit,” *US Patent 9628062 B1*, issued on April 18, 2017.
- [2] **Van Loi Le**, Tae-Hyoung Kim, and Taegeun Yoo, “Ultra-low power outermost-edge-based gesture recognition system,” *Singapore Patent 10201902927U*, filed on April 1, 2019.

Journal

- [3] **Van Loi Le**, J. Li, A. Chang, and Tony T. Kim, “A 0.4-V 0.138-fJ/Cycle Single-Phase-Clocking Redundant-Transition-Free 24T Flip-Flop with Change-Sensing Scheme in 40-nm CMOS,” in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 53, pp. 2806-2817, Oct. 2018.
- [4] **Van Loi Le** and Tony T. Kim, "An Area and Energy Efficient Ultra-Low Voltage Level Shifter with Pass Transistor and Reduced-Swing Output Buffer in 65-nm CMOS," in *IEEE Transactions on Circuits and Systems-II (TCAS-II)*, vol. 65, pp. 607-611, May 2018.
- [5] **Van Loi Le**, T. Yoo, J. E. Kim, K.-H. Baek, and T. Kim, “A 213.7- μ W Gesture Sensing System-on-Chip with Self-Adaptive Motion Detection and Noise-Tolerant Outermost-Edge-Based Feature Extraction in 65-nm”, *IEEE Solid-State Circuits Letters (SSC-L)*, under review. (*Special Issue of 2019 IEEE European Solid-State Circuits Conference*)
- [6] **Van Loi Le**, T. Yoo, J. E. Kim, N. L. Ba, K.-H. Baek, Tony T. Kim, “A 137- μ W 1.78mm² 30-frames/s Real-Time Gesture Recognition System for Smart Devices”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, to be submitted.

[7] T. Yoo, **Van Loi Le**, J. E. Kim, K.-H. Baek, Tony T. Kim, “A 3- μ W 0.54mm² 30-frames/s Vision Chip for Real-Time Gesture Recognition in 65nm CMOS”, planned to submit to *IEEE Journal of Solid-State Circuits (JSSC)*, 2019.

[8] L. Lu, T. Yoo, **Van Loi Le**, and T. Kim, “An Ultra-Low Power 8T SRAM with Vertical Read Word Line and Data-Aware Write Assist,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, under review.

[9] S. M. Siddiqui, S. Ruchi, **Van Loi Le**, T. Yoo, I.-J. Chang, and T. Kim, "SRAM Radiation Hardening through Self-Refresh Operation and Error Correction," *IEEE Transactions on Device and Materials Reliability (TDMR)*, under review.

Conference

[10] **Van Loi Le**, T. Yoo, J. E. Kim, K.-H. Baek, Tony T. Kim, “A 213.7 μ W Gesture Sensing System-on-Chip with Self-Adaptive Motion Detection and Noise-Tolerant Outermost-Edge-based Feature Extraction in 65nm”, 2019 *IEEE European Solid-State Circuits Conference (ESSCIRC)* [Accepted].

[11] **Van Loi Le**, T. Yoo, and Tony T. Kim, “A 213.7- μ W Real-Time Gesture Recognition System for Wearables”, *International Solid-State Circuit Conference (ISSCC) Student Research Preview*, San Francisco, USA, Feb. 2019.

[12] **Van Loi Le**, J. Li, A. Chang, and Tony T. Kim, “An 82% Energy-Saving Change-Sensing Flip-Flop in 40nm CMOS for Ultra-Low Power Applications,” in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 197-200, Korea, Nov. 2017.

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