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A 0.058mm² 24μW Temperature Sensor in 40nm CMOS Process With $\pm 0.5^{\circ}\text{C}$ Inaccuracy From -55°C to 175°C

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Abstract This paper describes the design of a high accuracy smart temperature sensor in the 40nm standard CMOS process. Due to process scaling, the high threshold voltages, large leakage currents and low intrinsic gains, etc., cause the realization of conventional high performance analog circuits to become very challenging in advanced processes. In the proposed design, some new techniques have been utilized in order to overcome the obstacles due to process scaling. The sensor's frontend is based on substrate PNP transistors, couple with a two-step zooming ADC. This temperature sensor achieves a two-point calibrated inaccuracy of $\pm 0.5^{\circ}\text{C}$ and a one-point trimmed inaccuracy of $\pm 0.8^{\circ}\text{C}$ over a range of temperature from -55°C to 175°C . It draws 20μA from a 1.2V power supply and occupies an area of 0.0578 mm².

Keywords temperature sensor · 40nm Standard CMOS · Gain-enhancement Integrator · Reconfigurable Sample & Hold

1 Introduction

With increased user reliance on mobile electronic devices, such as mobile computing devices, mobile phones, electric vehicles, cordless tools, etc., users are more keenly aware of the benefit of accurate status of the state of charge of the mobile computing device's energy storage device. Many mobile devices include a fuel gauge that can indicate the state of charge of an energy storage device, such as a battery, a fuel cell, etc.[1].

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In order to properly charge or recharge the energy storage devices and determine accurate state of charge information about the energy storage device, the temperature information are required. Moreover, as the batteries's capacities and densities increase, the self-heating and increase leakage currents make the temperature information be critical to the systems' reliability. In this manner, the temperature sensors are usually included in the energy storage devices such as Battery fuel gauges.

Many publications on temperature sensors were proposed in recent years, most of them are not suitable in this applied area. The temperature sensors in processors consumed significantly high power which were up to mW [2–4]. Some temperature sensors in RFIDs adopted large temperature coefficient on-chip resistors[5] which are not usually available in standard CMOS processes. The time-domain designs utilized the temperature dependencies of threshold voltages (V_{th}) and mobilities (μ) of MOSFETs. The nonlinear temperature coefficients of V_{th} and μ result in poor accuracy.

Meanwhile, most of the temperature sensors reported were fabricated in old technologies, such as $0.5\mu\text{m}$, $0.35\mu\text{m}$ and $0.18\mu\text{m}$ [6–9]. Due to process scaling driven by digital portions in large SOCs, their scaling-incompatibility such as high supply voltages and intrinsic gains prevent them to be employed. Moreover, in newer technologies, lower supply voltages, smaller intrinsic gains, higher leakage current densities and relatively higher threshold voltages make the analog circuit design more challenging.

The large temperature range of Battery Fuel Gauge is another challenge for the temperature sensor design. In most applications[10], the temperature sensors were aimed at military range from -55°C to 125°C or even narrower. However, as the temperature could rise to as high as 175°C , issues such as leakage will be of very serious concern.

From the above discussion, it is obvious that existing solutions are not suitable for Battery Fuel Gauge applications. Issues related to process scaling, SOC-friendly, large temperature range and production cost control make temperature sensor design in the standard 40nm CMOS process very challenging.

In this paper, we present a low-power integrated temperature sensor for Battery Fuel Gauge applications. The proposed temperature sensor is realized in 40nm standard CMOS process. A sensing range of -55°C to 175°C is targeted, which is enough for the battery charging monitoring. In order to provide the required accuracy for temperature information, Dynamic Element Matching (DEM) and Chopping techniques are both utilized in the front-end and in the ADC. A two-step Zooming ADC converts the voltage domain temperature information into digital bits.

The gain-boosted integrator architecture and reconfigurable Sample & Hold circuit are employed in the design to further improve the performance. Unlike in [10], all the digital control portions including the DEM for capacitor arrays are realized on-chip.

The rest of this paper is organized as follows, the overall architecture and basic principles are explained in Section II. The circuitry realization including the front-end and converter are depicted in Section III and IV respectively. In Section V, the measurement results are illustrated and analyzed. The conclusion is presented in Section VI.

2 Principles and Proposed Architecture

2.1 Principles

The basic operating principle of substrate PNP transistors based temperature sensor is illustrated in Fig. 1.

Fig. 1 Operating Principle of the Proposed Temperature Sensor

As shown in Fig.1(a), two different biasing currents flow through two PNP transistors and the required V_{BE} and ΔV_{BE} are produced directly.

The equation for V_{BE} is from [11]

$$V_{BE}(T) = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\frac{T}{T_0} - \eta\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) + \frac{kT}{q}\ln\left(\frac{I_C(T)}{I_C(T_0)}\right) \quad (1)$$

In eq.(1), V_{G0} is the bandgap voltage of silicon at 0K, the value is approximately 1.206V. K is the Boltzmann's constant, and η is a temperature constant. I_C is the collector current. T is the temperature value with Kelvin units and T_0 is an arbitrary reference voltage. The parameters with subscript 0 designates an appropriate quantity at reference temperature.

The proportional to absolute temperature (PTAT) voltage ΔV_{BE} is

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q}\ln\left(\frac{I_2}{I_1}\right) = \frac{kT}{q}\ln n \quad (2)$$

In eq. (2), the parameter n is the current ration of the two biasing currents of the BJTs. Ignoring the higher order portion of V_{BE} , a temperature independent voltage can be written as :

$$V_{ref} = V_{BE} + \alpha\Delta V_{BE} \quad (3)$$

If the ΔV_{BE} is utilized as the input of an analog-to-digital converter (ADC) with a reference, V_{ref} , the ratio of them can be used to represent the temperature information:

$$\mu = \frac{\alpha\Delta V_{BE}}{V_{ref}} = \frac{\alpha\Delta V_{BE}}{\alpha\Delta V_{BE} + V_{BE}} \quad (4)$$

Since ΔV_{BE} is a linear PTAT voltage and V_{ref} is a temperature-independent voltage, the value of μ is also a PTAT linear value. The final required temperature value can be derived by[12]

$$T_{out} = T_h \times \mu + T_{zero} \quad (5)$$

T_h is the value when V_{BE} is close to zero. The extrapolated temperature is around 330°C as shown in Figure 1(b). T_{zero} is approximated to -273K.

If the summation of V_{ref} in eq.(3) is shifted into the digital domain, the supply voltage could be lower than the bandgap voltage. Consequently, eq.(3) can be rewritten into

$$\mu = \frac{\alpha \Delta V_{BE}}{\alpha \Delta V_{BE} + V_{BE}} = \frac{\alpha}{\alpha + V_{BE}/\Delta V_{BE}} = \frac{\alpha}{\alpha + X} \quad (6)$$

The parameter X represents $V_{BE}/\Delta V_{BE}$. In this manner, the ADC only needs to process the ratio between V_{BE} and ΔV_{BE} , which simplifies the frontend and makes the digital back-end calibration possible[13].

2.2 Proposed Architecture

As the proposed design is achieved in standard CMOS process and based on accuracy consideration, the substrate PNP transistors are chosen for temperature sensing. The system level architecture of the proposed temperature sensor is shown in Fig.2. In

Fig. 2 The System Level Structure of the Proposed Temperature Sensor

Fig.2, $\Sigma\Delta$ represents the $\Sigma\Delta$ modulator, and SAR stands for *Successive Approximation*, which are two sub blocks of the zooming ADC adopted in the presented design.

The leftmost portion generates the PTAT biasing currents for the BJT Core. The BJT Core contains two identical PNP transistors to produce the required V_{BE} and ΔV_{BE} voltages. Unlike in [10], the output of BJT Core are clock-like waveforms. The two voltage levels for the output of BJT Core are V_{BE1} and V_{BE2} . The consideration of moving chopper switches from the input of ADC into the BJT Core is based on the large threshold voltages of transmission gate transistors.

As mentioned earlier, the threshold voltages in the 40nm CMOS process are optimized for digital circuits design. Consequently, they can be as high as 0.8V for minimum length transistors with 1.2V power supply. As the values of V_{BE} vary from 0.4V to 0.8V in the large temperature range, it is difficult to turn on either NMOS or PMOS even in the room temperature. In order to avoid the utilization of bootstrapped switches for area consideration, the switches are placed closer to the upper current source transistors.

The ADC used in this design is a new architecture Zooming ADC. The ADC's conversion can be split into two steps. The first step is comparison with a SAR ADC, and the second step generates the output with a $\Sigma\Delta$ ADC, where the first integrator is reconfigurable. In the first step, the first integrator behaves like Sample&Hold to realize the function of SAR. When the coarse results are produced, the first integrator is reset and recombined into a normal integrator. In this manner, the digital back-end combines the output of two steps and converts them into corresponding temperature values after digital calibration.

In order to achieve the required accuracy, DEM and Chopper techniques are adopted both in the frontend and the capacitor arrays of ADC. Furthermore, the integrators are gain boosted and offset removed. At the sensitive nodes, thick gate transistors are utilized to limit the influence of large gate leakage currents in the 40nm CMOS process.

3 Frontend of the Proposed Sensor

The circuit of the frontend sensing portion is shown in Fig.3. It contains a PTAT Current generator and a BJT core. The actual sizes of each transistor are shown as well. All current mirrors are identical. In order to achieve better matching, large length is preferred. Each bipolar transistor's multiplier is 10.

Fig. 3 The PTAT Current Generator and the BJT Core

In the PTAT current generator, the base-emitter voltage difference of Q_L and Q_R appears on resistor R_1 to produce the PTAT current. The unit biasing current for BJTs is I_{PTAT} . In the BJT core, the two BJTs Q_1 and Q_2 are biased by I_{PTAT} and nI_{PTAT} alternatively. When the BJT transistor is biased by nI_{PTAT} , its base-emitter voltage is $V_{BE,h}$. The base-emitter voltage becomes $V_{BE,l}$ when the smaller I_{PTAT} flows through it. The detailed component sizes can be found in Table.1.

Table 1 Actual Sizes of the important components in Frontend

Component Name	W (μm)	L (μm)	Note
M ₁	2	3	5+1=6 PTAT current Branches
M ₂	2	3	10+1=11 PTAT current Branches
M ₃	2	0.5	
M ₄	2	0.5	
R ₁	1	5	Series=20, Value= 63.527 K Ω
Q ₁	8	8	m=10, Current Ratio= 10:1
Q ₂	8	8	m=10, Current Ratio= 10:1
Q _L	8	8	m=10, Current Ratio= 5:1
Q _R	8	8	m=10, Current Ratio= 5:1

As described in [14], PTAT biasing currents are preferred to reduce the non-linear term in the formula of V_{BE} . In this manner, the PTAT currents are adopted for the BJT core's biasing. In order to reduce the influence of non-ideal effects, DEM technique is utilized to suppress the current sources' mismatch. As the current sources' gates are connected to opamp's output directly, the gate leakage currents can degrade the

In comparison to the separated DEM and chopper structure in [8], the merged DEM and chopper architecture in this design can reduce the mismatch between Q_1 and Q_2 .

Fig. 4 (a) The BJT Core in [13]; (b) The BJT Core in this work

During phase ϕ_1 (ϕ_1 and ϕ_2 are complementary non-overlap clocks) in the upper circuit of Fig.4(a), the smaller voltage $V_{BE,I}$ appears on the left BJT Q_1 . This voltage

is sampled by $(m+1)C_1$,

$$(m+1)C_1(V_{BE\downarrow} - V_{CMin}) \quad (7)$$

C_1 is the unit capacitor of the ADC. The value of C_1 is 150fF based on the calculation of noise requirement. m is the number of unit capacitor for ADC sampling. The range of m in the aimed temperature range is 4 to 29. Hence, maximum m is chosen to be 30. V_{CMin} is the input common mode voltage of the first integrator.

In the second phase ϕ_2 , the voltage value of V_{BE1} becomes the larger value $V_{BE\uparrow}$. Only mC_1 samples this voltage:

$$mC_1(V_{BE\uparrow} - V_{CMin}) + aC_1\Delta V_{outp} \quad (8)$$

The parameter aC_1 is the integrating capacitor. Consequently, the voltage increase in the first integrator's upper output is

$$\Delta V_{outp} = 1/a \cdot (V_{BE\downarrow} - m\Delta V_{BE}) \quad (9)$$

Similarly, the lower output variation is:

$$\Delta V_{outn} = 1/a \cdot (-V_{BE\downarrow} + m\Delta V_{BE}) \quad (10)$$

The entire output increment within a cycle is

$$\Delta V_{out} = 2/a \cdot (V_{BE\downarrow} - m\Delta V_{BE}) \quad (11)$$

If the mismatch of two BJT transistors Q_1 and Q_2 is considered, the output change of Fig. 4(a) becomes

$$\Delta V_{out} = 2/a \cdot [(V_{BE\downarrow} - m\Delta V_{BE}) - (m+1)V_T \cdot \Delta s] \quad (12)$$

The parameter Δs represents the mismatch of the Q_1 and Q_2 . Apparently, the mismatch is amplified by the sampling factor $(m+1)$. As described in [13], the value of m is from 6 to 28. In this manner, the BJTs' mismatch caused by sampling error is amplified by the sampling factor dramatically. More detailed derivation can be found in Appendix A.

When the sampling configuration in Fig. 4(b) is adopted, the output variation becomes:

$$\Delta V_{out} = 2/a \cdot [(V_{BE\downarrow} - m\Delta V_{BE}) - V_T \cdot \Delta s] \quad (13)$$

Only the term $V_T \cdot \Delta s$ remains in the final output of the first integrator. Comparing this with the result shown in Eq.12, the value is much smaller and has much less impact on the accuracy of the temperature sensor.

A typical 10 Monte-Carlo simulation waveforms of the generated V_{BE} is depicted in Fig.5. Apparently, the mismatches of the current mirrors are removed by the adopted chopping and DEM.

Fig. 5 10 Monte-Carlo simulation waveforms of the generated V_{BE}

4 Zooming ADC

Fig. 6 shows the top level structure of the proposed Zooming ADC when it is in the second order $\Sigma\Delta$ ADC's configuration. When it is working as a SAR ADC, the first stage is a little different from the Fig.6. The detailed SAR conversion will be discussed later. For charge injection consideration, two non-overlapped clock ϕ_{1d} and ϕ_{2d} that controls the sampling switches are slightly delayed from ϕ_1 and ϕ_2 respectively.

Fig. 6 The Top Level Structure of Proposed Zooming ADC

The second integrator has the same architecture as the first one, therefore, the detailed connection is not shown here. The remainder of this section will describe the individual portions of the Zooming ADC.

4.1 Zooming ADC Mechanism

The proposed Zooming ADC is a two-step ADC. The first five cycles are used for the rough value comparison and the following cycles are for the accurate $\Sigma\Delta$ ADC's configuration.

This Zooming ADC is designed to be 15 bits, 5 bits for SAR conversion and 10 bits for Sigma-Delta conversion. Assume the Over-Sampling Ratio (OSR) of the 10 bits Second-Order $\Sigma\Delta$ ADC is OSR_1 , hence for 15 bits SNR requirement, the OSR should be $4 \cdot OSR_1$ with the same circuit. Benefiting from the pre-processing of the 5 bits SAR, the total conversion time of the Zooming ADC is just $5 + OSR_1$. As OSR is usually much larger than 5 (64, 128, etc.), for most one-shot applications, the total energy consumption for one conversion can be significantly reduced.

The zooming ADC is based on a Feed-forward Second-Order $\Sigma\Delta$ ADC. There are two integrators and one comparator. The total number of sampling capacitors units is 29, which corresponds to the range of input ratios between V_{BE} and ΔV_{BE} .

Assume the parameter m represents the output of SAR conversion, the Least Significant Bit (LSB) voltage of SAR is $V_{LSB_{SAR}}$. The output of the first integrator can be written as

$$V_{out} = V_{in} - m \cdot V_{LSB_{SAR}} \quad (14)$$

By comparing the input signal with different reference tap voltages, the Zooming ADC can generate the coarse output bits in the first step. During the SAR ADC conversion, the value of m changes from MSB ($16 \cdot C_S$) to LSB ($1 \cdot C_S$). When the SAR comparison is completed, the Zooming ADC output enters the $\Sigma\Delta$ ADC combination for conversion. During the $\Sigma\Delta$ conversion, the value m is fixed, and the output of comparator controls the switch SW_{ctrl} to maintain the stability of the entire loop.

4.2 SAR ADC Mechanism

When the Zooming ADC works as a SAR ADC, the first integrator is changed to a Sample&Hold configuration as shown in Fig.7. In order to simplify the analysis, the conventional integrator structure is adopted. In the real design, the gain-boosting integrator structure is used which will be explained in the next section.

Fig.7(a) is the traditional Sample&Hold circuit, and Fig.7(b) is the new modified Sample&Hold circuit based on the structure of an integrator. Fig.7(c)(d) show the Sample&Hold configurations during the two phases.

If the input common mode voltage (V_{CMin}) of the opamp is equal to half the supply voltage ($0.5V_{DD}$ is around 500mV or 600mV), due to the high threshold voltages (400mV to 800mV) and low supply voltages (V_{DD} is from 1V to 1.2V), there is no headroom for the input pair transistors to work in the saturation regions (one V_{GS} is

Fig. 7 First Integrator in SAR Comparison

greater than $0.5V_{DD}$). In this manner, V_{CMin} cannot be $0.5V_{DD}$ either for PMOS or NMOS input pair. However, for large output voltage swing consideration, it is better to keep the output common mode voltage at half the supply voltage. As a result, the output common mode voltage is not equal to that at the input.

Correlated Double Sampling (CDS) techniques are widely employed for the switched-capacitor integrators in order to remove the opamp's offset and low frequency noise. Based on the aforementioned analysis, the traditional CDS technique in [10] is not suitable for the proposed design because it shorts the input and output nodes during the sampling phase. Therefore, the new structure in Fig. 6 is utilized.

In the first five cycles of the SAR conversion, the value of C_{in} changes from 16 unit capacitors to 1 unit capacitor. The values of two holding capacitors C_1 and C_2 are equal. During SAR conversion, these two capacitors are swapped during the two phases, ϕ_1 and ϕ_2 .

In phase ϕ_1 which is the sampling phase, the left plate of C_2 is connected to the input common mode voltage V_{CMin} , and the right plate is connected to the output common mode voltage V_{CMout} . At the same time, C_1 is connected between the input and output of the opamp in order to maintain the common mode difference between them. In the holding phase ϕ_2 , C_1 and C_2 's roles are swapped. C_2 transfers the input signal to the output of opamp, and C_1 is pre-charged between the two different common mode voltages.

With the adopted split-capacitor architecture, the CDS technique can still be utilized with different input and output common mode voltages.

A typical simulation waveform of the first integrator's output of the proposed zooming ADC (and BJT core's output as reference) is shown in Fig.8 as reference. In the first $250\mu s$, the integrators' switched-capacitor CMFB (common-mode feedback) circuits will be stable. The following 5 cycles are for the SAR conversion. After the SAR step, the second sigma-delta begins.

Fig. 8 A typical simulation waveform of the first integrator of the proposed zooming ADC

4.3 The First Integrator in the Sigma Delta ADC

As the first integrator of Sigma-Delta ADC needs to have high gain for noise suppression, the opamp in the first integrator is very crucial to the entire ADC. However, the small intrinsic gain in the 40nm CMOS process makes the design of the single stage high gain opamp very difficult. To overcome this obstacle, the gain-boosting integrator structure is utilized in this Zooming ADC design[15–17].

The ideal transfer function of integrator is :

$$H(\omega) = -\frac{C_S}{C_I} \frac{1}{1 - e^{j\omega T}} \quad (15)$$

C_S is the input sampling capacitor and C_I is the integrating capacitor. If finite opamp gain (A) is considered, the equation becomes:

$$H(\omega) = -\frac{C_S}{C_I} \frac{1}{1 - e^{j\omega T} \left(1 - \frac{C_S}{C_I A}\right)} \quad (16)$$

The finite opamp gain causes the integrator gain not equal to the one in Eq.15. If the proposed structure in Fig.6 is utilized, the gain of the integrator is boosted.

$$H(\omega) = \frac{C_S/C_I}{[1 - m(\omega)]e^{-j\theta(\omega)}} \quad (17)$$

$$m(\omega) = -\frac{1}{A} \left[1 + \frac{C_S}{C_I} + \frac{C_{off}}{C_I}\right] \quad (18)$$

$$\theta(\omega) = \frac{1}{A^2} \frac{C_S}{C_I \cdot \omega T} \quad (19)$$

In the above equations, $m(\omega)$ and $\theta(\omega)$ represent the gain error and phase error respectively. The offset storing capacitor C_{off} is introduced as the same as in Fig.6 (C_{off1} and C_{off2}). Another advantage of this integrator is the offset-insensitivity. According to the analysis in [15], the input referred offset of the opamp can be removed by C_{off} .

Fig. 9 Adopted CDS Evaluation with PSS and PAC Simulation Results

The adopted CDS technique is evaluated by the PSS and PAC simulations. As shown in Fig.9, without the CDS, the original folded-cascode opamp's DC gain is only 40dB in this 40nm CMOS process. Thanks to the CDS, the DC gain is boosted to more than 100dB. The significant increase guarantees the effective gain of the first integrator which is related to the SNDR of the entire ADC directly.

4.4 DEM Control Logic for The Capacitor Arrays

Unlike in [10], the DEM control logic for the capacitor arrays is realized on-chip. The block diagram of the DEM is shown in the following figure.

Fig. 10 DEM Control Logic for The Capacitor Arrays

The DEM function is triggered only in the $\Sigma\Delta$ conversion step.

The output of the first SAR comparison step are in 5-digits. These digits are converted into 29 thermal bits by a 5-to-29 Decoder. Each of the two shift register rings contain 29 D-Flipflop cells. These D-Flipflop cells are preset by the decoder. In this manner, the output of $\Sigma\Delta$ conversion chooses either the i to $(m+i)$ ring or the i to

$(m + i + 2)$ ring with p Multipliers where p is equal to 29 in this design. The output of the Multipliers is directly connected to the capacitor array's switches.

According to the analysis in [12], each capacitor is assumed to have a mismatch of δ_i compared to the averaged capacitor value. Based on the random normal distribution of the mismatch, the sum of these error equates to zero.

If the original mismatch error δ_i is 5%, the residue error is around 2.5×10^{-3} , which has little influence on the accuracy of the entire temperature sensor.

4.5 Offset-Free Comparator

The comparator circuit used in this design is demonstrated in Fig.11.

Fig. 11 Offset Compensated Comparator

The upper portion is the pre-amplifier of the comparator, and the lower part is the SR Latch and Multiplexer for system level chopping.

The voltages V_{op1} and V_{on1} are the differential output of the first integrator, and V_{op2} and V_{on2} are the differential output of the second integrator. V_{CMo} is the output common-mode voltage for both integrators and V_{NS} is the biasing voltage for the current source of the pre-amplifier. The differential output of the pre-amplifier are VC_{1p} and VC_{1n} . These two voltages are the input of the following SR Latch.

In the first phase ϕ_1 , the input pair of the pre-amplifier is shorted as diodes. Therefore, the offset of pre-amplifier is sampled by the top plates of C_2 and C_3 . In the second phase ϕ_2 , the bottom plate of C_2 is connected to the output of the first integrator. Within this phase, the pre-stored offset voltage is subtracted from the input

of the pre-amplifier. Consequently, the pre-amplifier only process the sum of the two integrators' output, exclude its offset voltage. In this manner, the first stage of the comparator is offset-free.

The above analysis can be proved by the following equations. When the left portion of Fig.11 is considered, due to the charge balancing at the input node, the charge at different phases are equal.

$$\begin{aligned} (V_{CMo} - V_x - V_{of})C_2 + (V_{on2} - V_x - V_{of})C_3 \\ = (V_{op1} - V_{in} - V_{of})C_2 + (V_{CMo} - V_{in} - V_{of})C_3 \end{aligned} \quad (20)$$

V_x is the input common-mode voltage of the pre-amplifier when the input pairs are shorted as diode, and V_{of} is the input referred offset voltage. Therefore, the voltage at the left input node of the pre-amplifier is:

$$\begin{aligned} (C_2 + C_3)V_{in} = V_{CMo}(C_2 - C_3) - V_x(C_2 + C_3) \\ + V_{on2}C_3 - V_{op1}C_2 \end{aligned} \quad (21)$$

If the capacitor values of C_2 and C_3 are equal, Eq.(21) can be simplified into:

$$2V_{in} = V_{on2} - V_{op1} - 2V_x \quad (22)$$

Similarly, the right input voltage in the second phase is:

$$2V_{ip} = V_{op2} - V_{on1} - 2V_x \quad (23)$$

Subsequently, the differential input voltage of the pre-amplifier is:

$$\begin{aligned} V_{input} &= V_{ip} - V_{in} \\ &= \frac{(V_{op2} - V_{on1}) - (V_{on2} - V_{op1})}{2} \\ &= \frac{V_{o1} + V_{o2}}{2} \end{aligned} \quad (24)$$

Apparently, the input referred offset voltage does not exist in the final equation of the pre-amplifier, which proves the pre-amplifier's offset is removed with the sampling method.

4.6 Dithering for Harmonics Reduction

Besides the previous mentioned techniques, additional dithering block is also added to the input of the comparator. An 11-bit Pseudo Random Number Generator (PRNG) generates the 2^{11} random numbers and the output controls a switch. An extra small voltage connects or disconnects the input of the comparator according to the status of the switch. In this manner, the harmonics which are mainly due to the system chopping and integrators are suppressed.

Fig. 12 The Die Photo of the Temperature Sensor

5 Measurements and Comparison

The sensor is fabricated in GlobalFoundries 40nm standard CMOS process. The active area is 0.0578mm^2 and the die photo is shown in Fig. 13.

The proposed temperature sensor consumes $20\mu\text{A}$ currents from a supply voltage between 1.1V to 1.3V at 25°C room temperature. The working frequency for the zooming ADC and other digital blocks is 50kHz. With a over sampling ratio of 128, the resultant temperature value can be generated within 2.56msec.

In order to further analyze the performance of the temperature sensor, some accurate measurement equipments are employed. The thermal-stream which provides the temperature range from -55°C to 175°C is the X-STREAM 4310 from Temptronic company. The supply voltages are generated from Agilent's E3631A, 0-6V, 5A/0- $\pm 25\text{V}$, 1A. The clock generator is the Agilent 33250A, 80MHz Function/ Arbitrary Waveform Generator. The output data is collected by Agilent Logic Analyzer 16802A and the Agilent 34401A 61/2 Digital Multimeter is also adopted.

As the temperature value displayed on the screen of the thermal-stream is the airflow's, a more accurate thermocouple is utilized. Firstly, the thermocouple is calibrated with a high accuracy RTD pt100 Thermometer. Although the RTD can provide temperature accuracy as high as 0.01°C , its huge size of it makes it impossible to place it very close to the chip. Thus, a medium accuracy thermocouple is calibrated and pasted on the surface of the testing chip. The values shown on the screen of the thermal-stream reflect the temperature values of the airflow and the thermocouple. Only the temperature of the thermocouple is stable and the data is collected by the logic analyzer.

Fig. 13 The Die Photo of the Temperature Sensor

Three methods of digital calibration are employed to demonstrate the effectiveness. They will be depicted in the following subsections. In addition, the result comparison with recent publications is also listed.

5.1 Conventional Two-point Calibration

Conventional Two-point calibration is firstly examined. Two temperatures 25°C and 75°C are chosen. Recalling Eq.(4) and Eq.(5), there are three unknown parameters: α , A and B . No ideal value of μ is known before the calibration. The results and simulation are different. In this manner, a fully measured chip is used as a reference for the others. This chip is measured within the full temperature range from -55°C to 175°C . The best accuracy corresponding to A and B values is generated. As two points are used, there are two equations with three unknown parameters. If the value of B is fixed with the best fitting of the reference chip, the residue temperature errors are shown in Fig.14.

The best accuracy is 0.5°C in the temperature range.

If A 's value is pre-set, α and B 's values are derived from the two equations. However, the final result of B has an imaginary term which is not reasonable. As a result, this approach is not used.

5.2 Best-Fitting Two-point Calibration

Besides the conventional two-point calibration, a best-fitting two-point calibration is also utilized. This method is based on searching the best fitting curve of the current

Fig. 14 The Residue Temperature Errors of the Conventional Two-point Calibration

μ line. The value of α is swept to find the minimum temperature inaccuracy. After the best accuracy α is derived, the best μ curve is generated. With this approach, the residue temperature errors of the entire 10 samples are shown.

Fig. 15 The Residue Temperature Errors of the Best-Fitting Two-point Calibration

5.3 One-point Calibration

Due to cost consideration, one-point calibration is preferred over two-point calibration. Usually, some chips from the same batch are chosen as the reference. These chips are measured carefully over the temperature range and the parameters of the three unknown α , A and B can be determined partly.

In our measurement, one chip's temperature performance is chosen as the reference to simply the calculation. An accurate external voltage named V_X is adopted to provide the accurate internal V_{BE} value. Assume the ADC's output is X_1 under this V_X and X_2 under the internal V_{BE} value, the value of V_{BE} value can be derived with a simple equation:

$$V_{BE} = V_X \times (X_2 \div X_1) \quad (25)$$

After the calibration of this single chip, the value of A and B can be fixed. These two fixed parameters A and B , can be applied to the other 9 chips. Using this method, the residue temperature errors of the 10 chips can be derived.

Fig. 16 The Residue Temperature Errors of the One-point Calibration

As shown in Fig16, the best accuracy is around $\pm 0.8^\circ\text{C}$, slightly worse than the previous two approaches.

5.4 Result Comparison

The performance of this design is compared with the state-of-the-art sensors as shown in Table I. Although the analog circuit design under 40nm CMOS is much more challenging than the old processes, this design can still achieve comparable FOM in the largest temperature range.

6 Conclusion

A BJT-based high accuracy temperature sensor for the Battery Fuel Gauge applications has been implemented in standard 40nm CMOS process. In order to achieve

Table 2 Performances Summary and Comparison

	CICC'09 [2]	JSSC'10 [18]	T-CAS.I '13[4]	JSSC'13 [10]	This Work
Type	FDC	TDC	TDC	Z-M	Z-M
Process (nm)	65	350	65	160	40
Power(μ A)	333	11.1	500	6.8	20
V_{DD} (V)	1.2	3.3	1	1.5~2	1~1.3
Temp. range($^{\circ}$ C)	-40~110	0~90	0~110	-55~125	-55~175
Acc. $3\sigma(^{\circ}$ C)	-2.9/2.7	-0.4/0.6	± 1.5	0.15	0.5
Calibr.($^{\circ}$ C)	@90	@10,70	@40	@30	@35
Conv.time	3 μ s	500ms	2.13 μ s	5.3ms	2.56ms
$Acc^2.FOM$ ($J\%^2$)	15.1n	22m	1.86m	0.75n	2.4n

¹ $Acc^2.FOM = \text{Energy} / \text{Conversion} \times (\text{Relative Inaccuracy})^2$;

²Relative Inaccuracy(%) = $100 \times \text{Max Error} / \text{Specified Temperature Range}$

high accuracy, low power consumption and large temperature range in the 40nm C-MOS technology, some new techniques have been utilized in this work. In the front-end portion, the chopper switches are merged with DEM in order to suppress the influence of BJTs' mismatches and guarantee the fully turn-on of the switches under large threshold voltages and low supply voltages. The Zooming ADC can be divided into two steps. The gain-boosting integrator architecture is adopted to achieve the high gain with low intrinsic gain by the process scaling. In the first step for SAR comparison, the integrator is reconfigured into a Sample & Hold with split integrating capacitors. The DEM control logic is realized on chip to reduce the mismatch of the sampling capacitors. Furthermore, the comparator is offset-free with the special sampling method. According to the measurement results, this temperature sensor can achieve a one-point calibrated inaccuracy of $\pm 0.8^{\circ}\text{C}$ and a two-point trimmed inaccuracy of $\pm 0.5^{\circ}\text{C}$ over the temperature range from -55°C to 175°C .

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