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A 2.6–3.4 GHz Fractional- N Sub-Sampling Phase-Locked Loop Using a Calibration-Free Phase-Switching-Sub-Sampling Technique

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Abstract—Sub-sampling phase-locked loop (SSPLL) achieves lower in-band phase noise compared to a conventional charge-pump phase-locked loop with frequency dividers. Recently, several works have been reported to enable fractional- N operation of SSPLL to broaden its applications. However, they require careful calibrations with extra silicon area and adjusting time (~ 20 ms measured) to achieve low phase noise. For scenarios requiring short settling time such as frequency modulation, such a time consuming calibration is undesirable. This letter presents a phase-switching technique for fractional- N mode SSPLL to eliminate this calibration. The principle of the technique is analyzed and a prototype is fabricated in 65-nm CMOS technology. Even without calibration, the frequency synthesizer achieves a figure of merit of -234.3 dB under fractional- N operation, with 13.3-mW power consumption at 1.2-V supply.

Index Terms—Calibration free, CMOS phase-locked loop (PLL), fractional- N sub-sampling (SS), phase switching (PS).

I. INTRODUCTION

HIGH-PERFORMANCE phase-locked loop (PLL) with low phase noise and high-frequency resolution is crucial for robust wireless communications. Among PLL families, sub-sampling PLL (SSPLL) remains unbeaten in terms of in-band phase noise performance due to the absence of the $20 \log N$ amplification in the noise from the phase-frequency detector and the charge pump. However, the biggest challenge of SSPLL application in RF synthesizer is the lack of fine-frequency resolution. Conventional SSPLL inherently permits only integer- N operation, resulting in an output frequency step equal to the input reference (REF) frequency which is usually tens of megahertz. This step is too large for wireless communication because the carrier frequency cannot be tuned correctly.

During a fractional- N mode operation for the conventional SSPLL, the phase error between REF and voltage-controlled oscillator (VCO) feedback signal will increase with time and thus the system fails to lock. Two approaches to solve this problem have been reported in recent years [1]–[3].

Chang *et al.* [1] and Raczkowski *et al.* [2] adopt digital-to-time convertors (DTCs) to modify the input REF clock to align with the feedback VCO clock, maintaining the locked state. In contrast, Chen *et al.* [3] utilizes the alias caused by the increasing phase difference between REF and VCO. By deliberately generating an artificial signal to cancel out the alias, a stable VCO control signal can be obtained and fractional- N mode of the SSPLL is achieved. Although [1]–[3] realized fractional- N operation and low in-band phase noise, they require sophisticated calibrations because the fractional- N operations rely on process, voltages, and temperature (PVT)-dependent parameters, such as DTC gain in [1] and [2] and RC waveform characteristics in [3]. Consequently, extra calibration time is needed before their outputs achieve low phase noise. This time period becomes another challenge for the fractional- N SSPLL to be applied in communications requiring short settling time.

In this letter, we propose a phase-switching-SS (PS-SS) technique as a calibration-free realization of fractional- N SS. During operation, the phase differences between adjacent steps are directly related to the VCO period without PVT dependence, providing signal shifting without any gain error, which eliminates gain error calibration.

II. PHASE-SWITCHING SUB-SAMPLING

To maintain the fractional- N relation between REF and VCO frequency, either the sampling clock (i.e., REF) or the feedback signal (i.e., VCO) can be shifted so that the phase error does not keep increasing. In the proposed PS technique, the VCO provides multiphase feedback, and a multiplexer (MUX) selects a certain phase to be sampled each time. This equivalently shifts the VCO signal to align with REF clock, and thus fractional- N relation is achieved.

Compared with the REF-shifting technique in [1] and [2], this PS technique provides a shifting inherently related to VCO period, eliminating gain error or PVT dependence. Fig. 1(a) describes the operation of fractional- N PS-SS. The VCO provides an eight-phase output which serves as the feedback to the sampler. After each sampling, the MUX selects another phase of VCO ($\text{INT} + \text{DSM}_i$ ahead of the last phase) for the next sampling. In this example, Phase 0 is also shown for better understanding. The selection index wraps back once it exceeds 8. During the locked state, over a long period of $M \times T_{\text{REF}}$, where M is a large integer, the total number of shifted phase is $\sum_{i=1}^M (\text{INT} + \text{DSM}_i)/8$. Thus, the average shifted phase number during each T_{REF} is $(\text{INT} + \overline{\text{DSM}})/8$. This builds the fractional- N relationship between the VCO output frequency (f_{VCO}) and the REF frequency (f_{REF}).

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Fig. 1. (a) Principle of fractional- N PS-SS operation. (b) Architecture of the proposed PS-SSPLL.

As illustrated in Fig. 1(a), we have

$$f_{VCO} = \left(N + \frac{INT + \overline{DSM}}{8} \right) f_{REF}$$

$$= \left(N + \frac{INT + 1 + \alpha/2^r}{8} \right) f_{REF} \quad (1)$$

where the symbols are defined in Fig. 1(a), and +1 is introduced by MASH 1-1. Integer N is ensured by a frequency-locked loop (FLL). Under this control, the PLL output frequency step is

$$\Delta f_{VCO} = \frac{f_{REF}}{8 \times 2^r}. \quad (2)$$

From Fig. 1(a), we can see that the sampled voltage is equivalently dithered by the delta-sigma modulator (DSM) output sequence, with high-pass shaped noise, and will be tackled by the loop filter. To ensure effective filtering of DSM noise, the feedback waveform should be linear across the sampled voltage range. Therefore, in this design, the feedback waveform is transformed to sawtooth, which has a large linear range.

III. DESIGN AND IMPLEMENTATION

Fig. 1(b) shows the system architecture of the proposed PS-SSPLL. Compared with a conventional integer- N SSPLL, only the PS-SS controlling part is added. The details are discussed as follows.

A. VCO and Eight-Phase Feedback Generation

To generate the eight-phase output techniques such as delay-locked loop or phase interpolation can also be used. However, the most important consideration for our design is to generate the eight phases without calibration time. The most suitable means is to divide a 12-GHz VCO output frequency by 4, as dividers take little time to settle. As shown in the equivalent 8 Φ -VCO gray box in Fig. 1(b), they act as a 3-GHz eight-phase VCO. The 12-GHz VCO signal passes an injection-locked frequency divider [4] due to its high input frequency and wide locking range, and a current-mode logic divider as it provides four-input eight-output interface. A side benefit of the high-frequency VCO+dividers is that it provides quadrature clock at 6 GHz and eight-phase clock at 3 GHz. Due to limited area, only a single-phase output at 3 GHz is measured in this prototype.

As the average adjacent phase difference is always $2\pi/8$ as long as the dividers are stable, there is no gain error but

TABLE I
LOOP PARAMETERS OF THE PROTOTYPE PS-SSPLL

K_{saw}	G_m	τ_{pulse}	R_s	C_p	C_s	K_{VCO}
3 GV/s	500 $\mu A/V$	60 ps	25 k Ω	2 pF	30 pF	50 MHz/V

K_{saw} = sawtooth slope

only mismatch among the generated phases. During PS, this mismatch introduces an equivalent random noise to the REF phase.

B. 8-to-1 MUX and Sawtooth Generator

A sawtooth generator is adopted to provide larger linear range for the sampled voltage. Although the transformed signal is at 3 GHz, the opening and closing of the MUX transmission gates operate at the REF frequency (40 MHz). The switching only needs to be stable before the next sampling. This simplifies the design of the MUX. Furthermore, the sawtooth generation can pause well before and after each sampling to further reduce power consumption. Postlayout simulation shows the phase noise of the sawtooth to be below -115 dBc/Hz at 1-kHz offset, introducing negligible impacts to the total phase noise.

C. Other Blocks

To achieve fine resolution, a DSM is adopted. Note that the DSM output range cannot be too large, to ensure the sampled voltages are well within the linear range of the sawtooth wave. In this letter, a MASH 1-1 DSM is chosen for its second-order noise shaping and moderate dither range (from 0 to 3). An serial peripheral interface module sets N , INT , and α , thereby the output frequency. The feedback voltage is captured by a track-and-hold (T/H) circuit, which is followed by a linear G_m cell to convert this voltage into current pulse. The simulated linear range of the G_m cell is from 0.18 to 1.02 V. The FLL and an automatic frequency controller are employed to help with the PLL locking. A 0.4-MHz PLL bandwidth is chosen, with parameters provided in Table I.

IV. MEASUREMENT RESULTS

This prototype is fabricated in GlobalFoundries 65-nm CMOS process. Fig. 2(a) shows the die photograph with active area of $700 \mu m \times 300 \mu m$. The power consumptions of 12-GHz VCO, frequency dividers, output buffer,

TABLE II
COMPARISON WITH OTHER STATE-OF-THE-ART MULTI-GHz FRACTIONAL-*N* PLLS

	[1]	[2]	[3]	[5]	[6]	This work
Tech. (nm)	180	28	65	40	180	65
Architecture ⁽¹⁾	RS-sub-sampling	RS-sub-sampling	AC-sub-sampling	ADPLL	Multi-modulus-divider PLL	PS-sub-sampling
Freq. (GHz)	2.12–2.4	9.2–12.7	2.6–3.9	2.1–2.7	2.9–4.1	2.6–3.4
Available output	Diff.	Diff.	Diff.	Diff.	Diff.	8Φ (3 GHz) Quad. (6 GHz) Diff. (12 GHz)
REF (MHz)	48	40	49.15	32	26	40
Power (mW)	17.3	13	11.5	0.86	69.6	13.3
In-band phase noise ⁽²⁾ (dBc/Hz)	-109 @50 kHz	-114 @200 kHz	-110 @100 kHz	-90 @30 kHz	-93 @100 kHz	-100.3 @100 kHz
Calibration	Needed	Needed	Needed ⁽³⁾	Free	Free	Free
Calibration time (us)	~20000 (measured)	~60 (simulated with 10% error)	Not mentioned	No	No	No
RMS jitter w/ Cal (fs)	266	280	240	-	-	-
RMS jitter w/o Cal (fs)	1892	~870 ⁽⁴⁾	Not mentioned	1710	~560 ⁽⁴⁾	531
FoM w/ Cal (dB) ⁽⁵⁾	-239.1	-240	-241.8	-	-	-
FoM w/o Cal (dB) ⁽⁵⁾	-222.1	~ -230.1	N.A.	-236	-226.6	-234.3
Active area (mm ²)	0.75	~0.66	0.23	0.2	0.68	0.21

⁽¹⁾ PS = phase-switching, RS = reference-shifting, AC = alias-canceling

⁽²⁾ All scaled to 3 GHz by $20 \log(f_c/3\text{GHz})$

⁽³⁾ An extra 8-b ADC operating at REF is needed

⁽⁴⁾ Calculated from phase noise profiles

⁽⁵⁾ $FoM = 20 \cdot \log \frac{\text{RMS jitter}}{1\text{s}} + 10 \cdot \log \frac{\text{Power}}{1\text{mW}}$

Fig. 2. (a) Die micrograph. (b) Fractional-*N* output spectrum showing REF spurs and (c) fractional spurs. (d) Phase noise across the output range.

Fig. 3. Phase noise under fractional-*N* mode (Trace 1, blue) and integer-*N* mode (Trace 4, purple).

The highest fractional spur is -48.4 dB at 313-kHz offset. The high REF spur is caused by the periodic disturbance to the sawtooth generator, the T/H, and the VCO. This can be reduced by spur mitigation techniques [7]. Fig. 2(d) shows the phase noise performance across the output range from 2.6 to 3.4 GHz. Fig. 3 shows a phase noise comparison between fractional-*N* and integer-*N* modes. During fractional-*N* mode, DSM noise slightly affects the out-of-band noise, and rms jitter integrated from 10 kHz to 30 MHz is 531 fs. Table II compares this work with other state-of-the-art multi-GHz fractional-*N* PLLs. Under conditions without calibration, this letter achieves the best jitter performance.

V. CONCLUSION

This letter proposed a calibration-free fractional-*N* PS-SSPLL to eliminate the calibration time. Measurement results prove its low in-band phase noise and jitter.

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and other blocks are 6.1, 3.7, 2.3, and 3.5 mW, respectively. Fig. 2(b) and (c) shows the REF spurs and fractional spurs at a fractional-*N* output of 3.051562 GHz, respectively.