Comparison between chemical vapor deposited and physical vapor deposited WSi$_2$ metal gate for InGaAs n-metal-oxide-semiconductor field-effect transistors

B. S. Ong,1,2 K. L. Pey,1,2,a1 C. Y. Ong,2 C. S. Tan,2 D. A. Antoniadis,1,3 and E. A. Fitzgerald1,4

1Advanced Materials for Micro and Nano-Systems, Singapore-MIT Alliance, Singapore 637460
2School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798
3Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA
4Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA

(Received 21 March 2011; accepted 6 April 2011; published online 3 May 2011)

We compare chemical vapor deposition (CVD) and physical vapor deposition (PVD) WSi$_2$ metal gate process for In$_{0.53}$Ga$_{0.47}$As n-metal-oxide-semiconductor field-effect transistors using 10 and 6.5 nm Al$_2$O$_3$ as dielectric layer. The CVD-processed metal gate device with 6.5 nm Al$_2$O$_3$ shows enhanced transistor performance such as drive current, maximum transconductance and maximum effective mobility. These values are relatively better than the PVD-processed counterpart device with improvement of 51.8%, 46.4%, and 47.8%, respectively. The improvement for the performance of the CVD-processed metal gate device is due to the fluorine passivation at the oxide/semiconductor interface and a nondestructive deposition process. © 2011 American Institute of Physics. [doi:10.1063/1.3584024]

III-V based semiconductors such as In$_x$Ga$_{1-x}$As are touted to be the most suitable alternative to replace Si beyond the 16 nm technology node for n-metal-oxide-semiconductor field-effect transistors (nMOSFETs) because of their higher electron mobility enhancement.1–4 Recently, there are reports using various high-κ dielectric materials on In$_{0.53}$Ga$_{0.47}$As substrate for logic device applications.2–4 These high-κ dielectrics have been deposited using atomic layer deposition (ALD). As for the metal gate layer, most of the literature reports prescribe the use of physical vapor deposition (PVD) processes such as sputtering2–4 or electron beam evaporation.5 PVD process is a destructive deposition method which tends to induce damages in the bulk of the oxide and/or oxide/semiconductor interface when the oxide is ultra-thin (<5 nm).6,7 These process-induced defects tend to degrade the MOSFET device performance and reliability. In order to minimize the damages caused by the physical bombardment from the deposited metal atoms, a less destructive deposition method such as chemical vapor deposition (CVD) is required as an alternative for the metal gate deposition.

Recently, our group has demonstrated a CVD process using tungsten silicide (WSi$_2$) layer for the metal gate on GaAs capacitor.8 The gate stack exhibited smooth and sharp interfaces with in-situ incorporation of fluorine atoms during CVD of WSi$_2$ metal layer using tungsten hexafluoride (WF$_6$) as one of the precursors. Fluorine incorporation has been reported to be able to improve the electrical performance of group IV9,10 and III-V9,11–13 based devices. WSi$_2$ is a good candidate for the metal gate owing to its low resistivity, high chemical resistance, robustness to high temperature processing and fine patterning capability.14–17 However, a detailed study on the effect of using different metal gate process conditions on the device performance characteristics of InGaAs-based nMOSFETs is still lacking. Hence, there is a need to have a thorough understanding of the CVD and PVD process for the metal formation of InGaAs nMOSFET. In this letter, we study the effect of using CVD and PVD process for WSi$_2$ metal gate for In$_{0.53}$Ga$_{0.47}$As nMOSFET with different aluminum oxide (Al$_2$O$_3$) thicknesses. Our results convincingly show that the InGaAs nMOSFET with CVD WSi$_2$ metal layer has a better device performance, as it is a non-destructive process and has an additional benefit from the in-situ fluorine incorporation which improves the integrity of the Al$_2$O$_3$/InGaAs interface.

InGaAs nMOSFET was fabricated on a 300 nm thick In$_{0.53}$Ga$_{0.47}$As with a p-type Be doping concentration of 1 × 10$^{17}$ cm$^{-3}$. It was deposited using molecular beam epitaxy on a heavily doped lattice-matched p-type InP substrate. The substrate was degreased using acetone and isopropyl alcohol. Next, the native oxide was removed using HF solution followed by NH$_4$OH solution. Finally, the surface was passivated with sulfur molecules by soaking into a (NH$_4$)$_2$S solution for at least 10 min. After these surface pretreatments, the samples were immediately loaded into an ALD system. A layer of Al$_2$O$_3$ dielectric of 10 nm and/or 6.5 nm, respectively, was grown at 300 °C using trimethylaluminum (TMA) and H$_2$O as the precursors. The TMA pulse was introduced into the chamber first because TMA has a self-cleaning property which reduces any native oxide previously formed.18 A WSi$_2$ metal gate was deposited using an Applied Materials P50000 CVD system at 330 °C with WF$_6$ and SiH$_4$ as the gas sources and argon as the carrier gas. For the reference samples, the WSi$_2$ metal gate was deposited using a Denton Sputtering PVD system, with argon as the sputtering gas and WSi$_2$ as the sputtering target. The WSi$_2$ metal gate structures were lithographically defined and dry etched using chlorine-based reactive ion etching system.

8Electronic mail: eklpey@ntu.edu.sg.
patterning, the self-aligned source and drain regions were implanted with a Si dose of $1 \times 10^{14}$ cm$^{-2}$. The implant energies are 50 keV and 30 keV for devices with the 10 nm and 6.5 nm Al$_2$O$_3$, respectively. The dopants were activated using rapid thermal processing at 600 °C for 10 s in an N$_2$ ambient. Lastly, the source and drain contacts were formed by electron beam evaporation of Ni/Ge/Au via a lift-off process. The MOSFET electrical characteristics were measured using an Agilent E5270 semiconductor parameter analyzer and a HP 4284 LCR meter in an enclosed chamber.

Figure 1 shows the comparison for the electrical characteristics of In$_{0.53}$Ga$_{0.47}$As nMOSFETs ($L_G=2$ μm and $W=200$ μm) with the metal gate fabricated using the PVD and CVD process with a 10 nm Al$_2$O$_3$ dielectric layer. The transfer characteristic ($V_{DS}=50$ mV) of the two devices shown in Fig. 1(a) shows that the PVD WSi$_2$ metal gate device has a drain current ($I_{DS}$) and maximum transconductance ($g_m$) of 4.6 mA/mm at $V_{GS}=3$ V and 6.1 mS/mm, respectively. While for the CVD WSi$_2$ metal gate device, $I_{DS}$ and $g_m$ increase by 21.8% (i.e., 5.6 mA/mm at $V_{GS}=3$ V) and 9.8% (6.7 mS/mm) as compared to the reference sample. The output characteristics of the two devices are shown in Fig. 1(b). The $I_{DS}$ ($V_{GS},V_{th}=2$ V and $V_{DS}=2$ V) for the PVD and CVD WSi$_2$ metal gated device is 123.1 mA/mm and 131.8 mA/mm, respectively. We observe that the CVD-proceded metal gate device tends to show an enhancement in the device performance most probably due to the in situ fluorine incorporation. Fluorine depth profile in the gate stack is examined using secondary ion mass spectrometry (SIMS) technique as shown in the inset of Fig. 1(a). The CVD WSi$_2$ metal gate device has higher fluorine content in the gate stack due to the WF$_6$ gas precursor used.

In order to further analyze the fluorine passivation effect at the Al$_2$O$_3$/InGaAs interface, another set of the devices were fabricated using a 6.5 nm Al$_2$O$_3$ dielectric layer. As this Al$_2$O$_3$ dielectric layer is thinner, we expect more fluorine atoms to be able to diffuse through this layer and be incorporated at the Al$_2$O$_3$/InGaAs interface. The transfer and output characteristics for the PVD and CVD WSi$_2$ metal gate InGaAs nMOSFETs with the 6.5 nm Al$_2$O$_3$ dielectric layer are shown in Figs. 2(a) and 2(b), respectively. The $I_{DS}$ ($V_{GS},V_{th}=2$ V and $V_{DS}=2$ V) and $g_m$ ($V_{DS}=50$ mV) of the CVD WSi$_2$ metal gate device are 166.6 mA/mm and 9.6 mS/mm which are much higher than that the PVD WSi$_2$ metal gate device. The improvement of $I_{DS}$ and $g_m$ is 51.8% and 46.4%, respectively. Due to its smaller atomic size, F atoms are able to diffuse through the thinner Al$_2$O$_3$ layer, thus leading to more F incorporation at the oxide/semiductor interface for the CVD WSi$_2$ metal gate device. The SIMS profile for the fluorine content in these gate stacks are shown in the inset of Fig. 2(a). This CVD-based device with 6.5 nm Al$_2$O$_3$ has higher fluorine content as compare to the PVD-based devices.

Table I is a summary of the transfer characteristics of the InGaAs nMOSFETs with different gate stacks. As expected, the thinner oxide gate stacks for both PVD and CVD processed devices show an improved performance. However, the exact increment in $I_{DS}$ and $g_m$ for the thinner gate dielectric is higher for the CVD-processed stack (62.5% and 43.3%, respectively) as compared to the PVD-based one (39.1% and 8.2%, respectively). Hence, there is another factor which affects the degradation of the device performance for the PVD WSi$_2$ metal gate devices.

As the interface quality is proportional to the effective mobility ($\mu_{eff}$) of the MOSFETs, $\mu_{eff}$ is extracted for all the
TABLE I. Summary of the transfer characteristics for devices with different gate stacks of different deposition schemes and oxide thickness.

<table>
<thead>
<tr>
<th>Al₂O₃ thickness (nm)</th>
<th>Iᵥₑ私立 Vᵥₑ私立 = 50 mV (mA/mm)</th>
<th>Maximum σₑ私立 (mS/mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVD WSi₂ metal gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>5.6</td>
<td>6.7</td>
</tr>
<tr>
<td>6.5</td>
<td>9.1</td>
<td>9.6</td>
</tr>
<tr>
<td>Increment (%)</td>
<td>62.5</td>
<td>43.3</td>
</tr>
<tr>
<td>PVD WSi₂ metal gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>4.6</td>
<td>6.1</td>
</tr>
<tr>
<td>6.5</td>
<td>6.4</td>
<td>6.6</td>
</tr>
<tr>
<td>Increment (%)</td>
<td>39.1</td>
<td>8.2</td>
</tr>
</tbody>
</table>

In conclusion, we have fabricated InGaAs nMOSFETs using CVD and PVD WSi₂ metal gate having 10 and 6.5 nm Al₂O₃ dielectric layer. The CVD WSi₂ metal gate InGaAs MOSFETs show a better device performance than the PVD WSi₂ metal gate devices. This is due to the in situ incorporation of fluorine atoms during the CVD process and its non-destructive nature, which gives a better Al₂O₃/InGaAs interface quality. These results suggest that the use of the CVD WSi₂ metal gate have advantages over the PVD stack and will be fully compatible with the current fabrication process flow for InGaAs nMOSFETs.

Financial and logistical support for this research work by the Singapore-MIT Alliance (SMA) under the Flagship Research Program (FRP) is gratefully acknowledged. This work was performed in part at the Nanyang Nano-Fabrication Center (N2FC) at School of EEE, Nanyang Technological University (NTU). The authors would like to thank Y. K. Chin, W. J. Lu, W. Liu, and N. Raghavan for useful technical discussions.