Comparison between chemical vapor deposited and physical vapor deposited WSi₂ metal gate for InGaAs n-metal-oxide-semiconductor field-effect transistors

Ong, B. S.; Pey, Kin Leong; Ong, C. Y.; Tan, Chuan Seng; Antoniadis, D. A.; Fitzgerald, E. A.

2011

Ong, B. S., Pey, K. L., Ong, C. Y., Tan, C. S., Antoniadis, D. A., & Fitzgerald, E. A. (2011). Comparison between chemical vapor deposited and physical vapor deposited WSi₂ metal gate for InGaAs n-metal-oxide-semiconductor field-effect transistors. *Applied Physics Letters*, 98(18), 182102-.

<https://hdl.handle.net/10356/86528>

<https://doi.org/10.1063/1.3584024>

© 2011 American Institute of Physics (AIP). This paper was published in *Applied Physics Letters* and is made available as an electronic reprint (preprint) with permission of American Institute of Physics (AIP). The published version is available at: [<http://dx.doi.org/10.1063/1.3584024>]. One print or electronic copy may be made for personal use only. Systematic or multiple reproduction, distribution to multiple locations via electronic or other means, duplication of any material in this paper for a fee or for commercial purposes, or modification of the content of the paper is prohibited and is subject to penalties under law.

Comparison between chemical vapor deposited and physical vapor deposited WSi₂ metal gate for InGaAs n-metal-oxide-semiconductor field-effect transistors

B. S. Ong,^{1,2} K. L. Pey,^{1,2,a)} C. Y. Ong,² C. S. Tan,² D. A. Antoniadis,^{1,3} and E. A. Fitzgerald^{1,4}

¹Advanced Materials for Micro and Nano-Systems, Singapore-MIT Alliance, Singapore 637460

²School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798

³Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA

⁴Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA

(Received 21 March 2011; accepted 6 April 2011; published online 3 May 2011)

We compare chemical vapor deposition (CVD) and physical vapor deposition (PVD) WSi₂ metal gate process for In_{0.53}Ga_{0.47}As n-metal-oxide-semiconductor field-effect transistors using 10 and 6.5 nm Al₂O₃ as dielectric layer. The CVD-processed metal gate device with 6.5 nm Al₂O₃ shows enhanced transistor performance such as drive current, maximum transconductance and maximum effective mobility. These values are relatively better than the PVD-processed counterpart device with improvement of 51.8%, 46.4%, and 47.8%, respectively. The improvement for the performance of the CVD-processed metal gate device is due to the fluorine passivation at the oxide/semiconductor interface and a nondestructive deposition process. © 2011 American Institute of Physics. [doi:10.1063/1.3584024]

III-V based semiconductors such as In_xGa_{1-x}As are touted to be the most suitable alternative to replace Si beyond the 16 nm technology node for n-metal-oxide-semiconductor field-effect transistors (nMOSFETs) because of their higher electron mobility enhancement.¹ Recently, there are reports using various high- κ dielectric materials on In_{0.53}Ga_{0.47}As substrate for logic device applications.²⁻⁴ These high- κ dielectrics have been deposited using atomic layer deposition (ALD). As for the metal gate layer, most of the literature reports prescribe the use of physical vapor deposition (PVD) processes such as sputtering²⁻⁴ or electron beam evaporation.⁵ PVD process is a destructive deposition method which tends to induce damages in the bulk of the oxide and/or oxide/semiconductor interface when the oxide is ultra-thin (<5 nm).^{6,7} These process-induced defects tend to degrade the MOSFET device performance and reliability. In order to minimize the damages caused by the physical bombardment from the deposited metal atoms, a less destructive deposition method such as chemical vapor deposition (CVD) is required as an alternative for the metal gate deposition.

Recently, our group has demonstrated a CVD process using tungsten silicide (WSi₂) layer for the metal gate on GaAs capacitor.⁸ The gate stack exhibited smooth and sharp interfaces with *in-situ* incorporation of fluorine atoms during CVD of WSi₂ metal layer using tungsten hexafluoride (WF₆) as one of the precursors. Fluorine incorporation has been reported to be able to improve the electrical performance of group IV^{9,10} and III-V^{4,11-13} based devices. WSi₂ is a good candidate for the metal gate owing to its low resistivity, high chemical resistance, robustness to high temperature processing and fine patterning capability.¹⁴⁻¹⁷ However, a detailed study on the effect of using different metal gate process con-

ditions on the device performance characteristics of InGaAs-based nMOSFETs is still lacking. Hence, there is a need to have a thorough understanding of the CVD and PVD process for the metal formation of InGaAs nMOSFET. In this letter, we study the effect of using CVD and PVD process for WSi₂ metal gate for In_{0.53}Ga_{0.47}As nMOSFET with different aluminum oxide (Al₂O₃) thicknesses. Our results convincingly show that the InGaAs nMOSFET with CVD WSi₂ metal layer has a better device performance, as it is a non-destructive process and has an additional benefit from the *in situ* fluorine incorporation which improves the integrity of the Al₂O₃/InGaAs interface.

InGaAs nMOSFET was fabricated on a 300 nm thick In_{0.53}Ga_{0.47}As with a p-type Be doping concentration of $1 \times 10^{17} \text{ cm}^{-3}$. It was deposited using molecular beam epitaxy on a heavily doped lattice-matched p-type InP substrate. The substrate was degreased using acetone and isopropyl alcohol. Next, the native oxide was removed using HF solution followed by NH₄OH solution. Finally, the surface was passivated with sulfur molecules by soaking into a (NH₄)₂S solution for at least 10 min. After these surface pretreatments, the samples were immediately loaded into an ALD system. A layer of Al₂O₃ dielectric of 10 nm and/or 6.5 nm, respectively, was grown at 300 °C using trimethylaluminum (TMA) and H₂O as the precursors. The TMA pulse was introduced into the chamber first because TMA has a self-cleaning property which reduces any native oxide previously formed.¹⁸ A WSi₂ metal gate was deposited using an Applied Materials P5000 CVD system at 330 °C with WF₆ and SiH₄ as the gas sources and argon as the carrier gas. For the reference samples, the WSi₂ metal gate was deposited using a Denton Sputtering PVD system, with argon as the sputtering gas and WSi₂ as the sputtering target. The WSi₂ metal gate structures were lithographically defined and dry etched using chlorine-based reactive ion etching system. After the gate

^{a)}Electronic mail: eklpey@ntu.edu.sg.

FIG. 1. (Color online) (a) Transfer and (b) output electrical characteristics of PVD and CVD WSi_2 metal gate InGaAs nMOSFETs with a 10 nm Al_2O_3 dielectric layer. The inset in (a) is the SIMS profile for the fluorine content in the PVD and CVD gate stack.

patterning, the self-aligned source and drain regions were implanted with a Si dose of $1 \times 10^{14} \text{ cm}^{-2}$. The implant energies are 50 keV and 30 keV for devices with the 10 nm and 6.5 nm Al_2O_3 , respectively. The dopants were activated using rapid thermal processing at 600 °C for 10 s in an N_2 ambient. Lastly, the source and drain contacts were formed by electron beam evaporation of Ni/Ge/Au via a liftoff process. The MOSFET electrical characteristics were measured using an Agilent E5270 semiconductor parameter analyzer and a HP 4284 LCR meter in an enclosed chamber.

Figure 1 shows the comparison for the electrical characteristics of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ nMOSFETs ($L_G=2 \mu\text{m}$ and $W=200 \mu\text{m}$) with the metal gate fabricated using the PVD and CVD process with a 10 nm Al_2O_3 dielectric layer. The transfer characteristic ($V_{\text{DS}}=50 \text{ mV}$) of the two devices shown in Fig. 1(a) shows that the PVD WSi_2 metal gate device has a drain current (I_{DS}) and maximum transconductance (g_m) of 4.6 mA/mm at $V_{\text{GS}}=3 \text{ V}$ and 6.1 mS/mm, respectively. While for the CVD WSi_2 metal gate device, I_{DS} and g_m increase by 21.8% (i.e., 5.6 mA/mm at $V_{\text{GS}}=3 \text{ V}$) and 9.8% (6.7 mS/mm) as compared to the reference sample. The output characteristics of the two devices are shown in Fig. 1(b). The I_{DS} ($V_{\text{GS}}-V_{\text{th}}=2 \text{ V}$ and $V_{\text{DS}}=2 \text{ V}$) for the PVD and CVD WSi_2 metal gated device is 123.1 mA/mm and 131.8 mA/mm, respectively. We observe that the CVD-processed metal gate device tends to show an enhancement in the device performance most probably due to the *in situ* fluorine incorporation.¹¹ Fluorine depth profile in the gate stack is examined using secondary ion mass spectrometry (SIMS) technique as shown in the inset of Fig. 1(a). The CVD WSi_2 metal gate device has higher fluorine content in the gate stack due to the WF_6 gas precursor used.^{15,16}

FIG. 2. (Color online) (a) Transfer and (b) output electrical characteristics of PVD and CVD WSi_2 metal gate InGaAs nMOSFETs with a 6.5 nm Al_2O_3 dielectric layer. The inset in (a) is the SIMS profile for the fluorine content in the PVD and CVD gate stack.

In order to further analyze the fluorine passivation effect at the $\text{Al}_2\text{O}_3/\text{InGaAs}$ interface, another set of the devices were fabricated using a 6.5 nm Al_2O_3 dielectric layer. As this Al_2O_3 dielectric layer is thinner, we expect more fluorine atoms to be able to diffuse through this layer and be incorporated at the $\text{Al}_2\text{O}_3/\text{InGaAs}$ interface. The transfer and output characteristics for the PVD and CVD WSi_2 metal gate InGaAs nMOSFETs with the 6.5 nm Al_2O_3 dielectric layer are shown in Figs. 2(a) and 2(b), respectively. The I_{DS} ($V_{\text{GS}}-V_{\text{th}}=2 \text{ V}$ and $V_{\text{DS}}=2 \text{ V}$) and g_m ($V_{\text{DS}}=50 \text{ mV}$) of the CVD WSi_2 metal gate device are 166.6 mA/mm and 9.6 mS/mm which are much higher than that the PVD WSi_2 metal gate device. The improvement of I_{DS} and g_m is 51.8% and 46.4%, respectively. Due to its smaller atomic size, F atoms are able to diffuse through the thinner Al_2O_3 layer, thus leading to more F incorporation at the oxide/semiconductor interface for the CVD WSi_2 metal gate device. The SIMS profile for the fluorine content in these gate stacks are shown in the inset of Fig. 2(a). This CVD-based device with 6.5 nm Al_2O_3 has higher fluorine content as compared to the PVD-based devices.

Table I is a summary of the transfer characteristics of the InGaAs nMOSFETs with different gate stacks. As expected, the thinner oxide gate stacks for both PVD and CVD processed devices show an improved performance. However, the exact increment in I_{DS} and g_m for the thinner gate dielectric is higher for the CVD-processed stack (62.5% and 43.3%, respectively) as compared to the PVD-based one (39.1% and 8.2%, respectively). Hence, there is another factor which affects the degradation of the device performance for the PVD WSi_2 metal gate devices.

As the interface quality is proportional to the effective mobility (μ_{eff}) of the MOSFETs, μ_{eff} is extracted for all the

TABLE I. Summary of the transfer characteristics for devices with different gate stacks of different deposition schemes and oxide thickness.

	Al ₂ O ₃ thickness (nm)	I _{DS} at V _D =50 mV (mA/mm)	Maximum g _m (mS/mm)
CVD WSi ₂ metal gate			
	10	5.6	6.7
	6.5	9.1	9.6
Increment (%)		62.5	43.3
PVD WSi ₂ metal gate			
	10	4.6	6.1
	6.5	6.4	6.6
Increment (%)		39.1	8.2

devices with different gate stacks. Figure 3 shows the extracted μ_{eff} versus the inversion charge density (Q_{INV}) using a split C - V method for the different InGaAs nMOSFETs. The inset of Fig. 3 is the inversion C - V characteristic measured on a $W \times L = 100 \mu\text{m} \times 10 \mu\text{m}$ device. The inversion capacitance for the 6.5 nm Al₂O₃ devices is higher than that for the 10 nm Al₂O₃ devices because of the thinner oxide used. As shown in Fig. 3, the CVD WSi₂ metal gate devices have better interface quality as they have higher μ_{eff} compared to their counterpart PVD stacks. The maximum μ_{eff} for the CVD-processed devices are 1562 cm²/V s and 1406 cm²/V s for the 6.5 nm and 10 nm Al₂O₃ dielectric layers, respectively. The μ_{eff} for CVD-processed device with a thinner Al₂O₃ is higher compared to that of the 10 nm Al₂O₃ layer, indicating a higher quality (lower interface trap density) Al₂O₃/InGaAs interface. This shows that more fluorine atoms are able to passivate the Al₂O₃/InGaAs interface as they can diffuse through the thinner Al₂O₃ layer easier. The PVD WSi₂ metal gate device with 6.5 nm Al₂O₃ dielectric layer has the lowest μ_{eff} . This indicates that the physical bombardment during the sputtering of WSi₂ metal gate dete-

FIG. 3. (Color online) Extracted effective mobility (μ_{eff}) vs inversion charge density (Q_{INV}) using split C - V method for the InGaAs nMOSFETs ($W \times L = 100 \times 10 \mu\text{m}^2$) with different gate stacks. The inset is the inversion C - V characteristics for InGaAs nMOSFETs with different gate stacks measured at 1 MHz.

riorates the Al₂O₃/InGaAs interface quality further for the devices with the thinner oxide layer.

In conclusion, we have fabricated InGaAs nMOSFETs using CVD and PVD WSi₂ metal gate having 10 and 6.5 nm Al₂O₃ dielectric layer. The CVD WSi₂ metal gate InGaAs MOSFETs show a better device performance than the PVD WSi₂ metal gate devices. This is due to the *in situ* incorporation of fluorine atoms during the CVD process and its non-destructive nature, which gives a better Al₂O₃/InGaAs interface quality. These results suggest that the use of the CVD WSi₂ metal gate have advantages over the PVD stack and will be fully compatible with the current fabrication process flow for InGaAs nMOSFETs.

Financial and logistical support for this research work by the Singapore-MIT Alliance (SMA) under the Flagship Research Program (FRP) is gratefully acknowledged. This work was performed in part at the Nanyang Nano-Fabrication Center (N2FC) at School of EEE, Nanyang Technological University (NTU). The authors would like to thank Y. K. Chin, W. J. Lu, W. Liu, and N. Raghavan for useful technical discussions.

¹International Technology Roadmap for Semiconductors, 2010 update; www.itrs.net.

²H. Zhao, F. Zhu, Y. T. Chen, J. W. Yum, Y. Wang, and J. C. Lee, *Appl. Phys. Lett.* **94**, 093505 (2009).

³N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampati, M. Yakimov, Y. Sun, P. Pianetta, C. K. Gaspe, M. B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, *Tech. Dig. - Int. Electron Devices Meet.* **2008**, 1.

⁴Y. T. Chen, H. Zhao, Y. Wang, F. Xue, and J. C. Lee, *Appl. Phys. Lett.* **96**, 103506 (2010).

⁵Y. Q. Wu, M. Xu, R. S. Wang, O. Koybasi, and P. D. Ye, *Tech. Dig. - Int. Electron Devices Meet.* **2009**, 323.

⁶T. Amazawa and H. Oikawa, *J. Electrochem. Soc.* **145**, 1297 (1998).

⁷D. G. Park, K. Y. Lim, H. J. Cho, T. H. Cha, I. S. Yeo, J. S. Roh, and J. W. Park, *Appl. Phys. Lett.* **80**, 2514 (2002).

⁸B. S. Ong, K. L. Pey, C. Y. Ong, C. S. Tan, C. L. Gan, H. Cai, D. A. Antoniadis, and E. A. Fitzgerald, *Electrochem. Solid-State Lett.* **13**, H328 (2010).

⁹C. S. Lai, W. C. Wu, S. C. Tien, J. H. Chen, J. C. Wang, L. L. Tay, and N. Rowell, *Appl. Phys. Lett.* **89**, 072904 (2006).

¹⁰R. Xie, M. Yu, M. Y. Lai, L. Chan, and C. Xhu, *Appl. Phys. Lett.* **92**, 163505 (2008).

¹¹Y. T. Chen, H. Zhao, J. H. Yum, Y. Wang, F. Xue, F. Zhou, and J. C. Lee, *Appl. Phys. Lett.* **95**, 013501 (2009).

¹²H. C. Chin, X. Gong, L. Wang, and Y. C. Yeo, *Electrochem. Solid-State Lett.* **13**, H440 (2010).

¹³Y. T. Chen, H. Zhao, Y. Wang, F. Xue, F. Zhou, and J. C. Lee, *Appl. Phys. Lett.* **96**, 253502 (2010).

¹⁴K. C. Saraswat, F. Mohammadi, and J. D. Meindl, *Tech. Dig. - Int. Electron Devices Meet.* **1979**, 462.

¹⁵K. Roh, S. Youn, S. Yang, and Y. Roh, *J. Vac. Sci. Technol. A* **19**, 1562 (2001).

¹⁶K. Nakajima, H. Nakazawa, K. Sekine, K. Matsuo, T. Saito, T. Katata, K. Suguro, and Y. Tsunashima, *IEEE Trans. Electron Devices* **52**, 2215 (2005).

¹⁷R. Gassilloud, F. Martin, C. Leroux, M. Hopstaken, X. Garros, M. Casse, G. Reimbold, T. Billon, and D. Bensahel, *Microelectron. Eng.* **86**, 263 (2009).

¹⁸C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, *Appl. Phys. Lett.* **92**, 071901 (2008).