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Dopant profile control of epitaxial emitter for silicon solar cells by low temperature epitaxy

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We report an alternative approach to grow phosphorus-doped epitaxial silicon emitter by rapid thermal chemical vapor deposition at low temperature ($T \geq 700^\circ\text{C}$). A power conversion efficiency (PCE) of $(6.6 \pm 0.3)\%$ and a *pseudo* PCE of $(10.2 \pm 0.2)\%$ has been achieved for the solar cell with epi-emitter grown at 700°C , in the absence of surface texturization, antireflective coating, and back surface field enhancement, without considering front contact shading. Secondary ion mass spectroscopy revealed that lower temperature silicon epitaxy yields a more abrupt *p-n* junction, suggesting potential applications for radial *p-n* junction wire array solar cells. © 2011 American Institute of Physics. [doi:10.1063/1.3607303]

Epitaxial thin film silicon (Si) solar cells offer the advantages in terms of performance while reducing material consumption for cost-effective manufacturability.^{1–6} Epitaxial Si, grown via rapid thermal chemical vapor deposition (RTCVD) at high temperatures ($>1100^\circ\text{C}$) with trichlorosilane gas precursor, has been used to produce solar cells with PCE of $\sim 15\%$.⁷ However, phosphorus has been observed to outdiffuse from Si at temperatures over 1000°C .⁸ This increases the width of the depletion region that results in higher recombination and lower open-circuit voltage (V_{oc}).⁹ Thus, there is a strong motivation to accomplish epitaxial Si growth at lower temperatures to suppress undesirable dopant interdiffusion. However, reduced growth rates in low temperature Si epitaxy present an obstacle in solar cell manufacturing where high throughput is required to be cost-effective. In order to realize the benefit of abrupt *p-n* junction with minimal impact to throughput, it would be advantageous to employ high temperature epitaxy to grow the thicker absorber base and lower temperature epitaxy for the shallow emitter. In this letter, phosphorus-doped epitaxial Si emitter grown on monocrystalline substrates at lower temperature ($\geq 700^\circ\text{C}$) by RTCVD using dichlorosilane (DCS) gas precursor is evaluated. To avoid ambiguity introduced by process variations, surface texturization, antireflective coating, and back-surface field are excluded in the cell fabrication to facilitate investigation of the junction quality of the emitter-substrate interface.

The $650\ \mu\text{m}$ thick Czochralski Si substrates with a resistivity of $4\text{--}10\ \Omega\cdot\text{cm}$ are first subjected to thermal oxidation. The $1\ \text{cm} \times 1\ \text{cm}$ Si windows, which act as a template for epitaxial growth, are then defined by photolithography and buffered oxide etch. The substrates are then cleaned in standard Radio Corporation of America (RCA) clean to ensure a pristine epitaxial growth interface. Inside the RTCVD reactor, the substrates are heated *in-situ* in ultra pure H_2 at

1100°C to reduce the native surface oxides. A $\sim 600\ \text{nm}$ thick phosphorus-doped epilayer is grown at 700°C and 900°C using DCS precursor and phosphine dopant gas. The growth rate of the epilayer at $\sim 80\ \text{Torr}$ is $0.07\ \mu\text{m}/\text{min}$ at 700°C and $0.48\ \mu\text{m}/\text{min}$ at 900°C , respectively. POCl_3 diffused cell is also fabricated at 900°C for comparison. The epilayer is passivated with $10\ \text{nm}$ silicon dioxide via rapid thermal oxidation. Front side contact is defined by photolithography, and front side and backside metallization are subsequently evaporated, before subjecting to forming gas anneal at 400°C for $30\ \text{min}$.

Fig. 1 shows the secondary ion mass spectroscopy (SIMS) depth profiles of the emitter of the solar cells. As expected, the POCl_3 diffused cell has a graded profile that tails gently into the substrate, while both cells with epi-emitters have step-like profiles. Moreover, it is evident that a lower growth temperature at 700°C gives a more abrupt *p-n* interface since the diffusivity of phosphorus within Si has Arrhenius temperature dependence. A decrease in phosphorus concentration towards the emitter surface, which can be

FIG. 1. SIMS depth profiles of phosphorus dopant in the emitter layer of the solar cells with epi-emitters and the reference POCl_3 diffused solar cell.

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explained by the phosphorus outdiffusion across the junction interface during the cooling step, will result in high contact resistance of the front side contact and hence poor fill factor (FF) of the cells.¹⁰ SIMS (not shown here) also reveals increased oxygen concentration ($\sim 10^{19} \text{ cm}^{-3}$) at the emitter-substrate interface, possibly arising from the incomplete oxide removal from the substrate surface prior to epitaxial growth.

Pseudo power conversion efficiency (PCE), which is defined as the PCE when the series resistance is excluded,¹¹ can be determined from the *pseudo* current density-voltage (JV) results obtained from different illumination intensities. From Fig. 2, the *pseudo* PCE of the solar cells are $(10.2 \pm 0.2)\%$ (cell with epi-emitter grown at 700°C), $(8.7 \pm 0.2)\%$ (cell with epi-emitter grown at 900°C) and $(10.0 \pm 0.3)\%$ (diffused emitter cell). The results suggest the potential for the cell with an epi-emitter grown at 700°C . Fig. 2 inset presents the solar cell parameters of the $1 \text{ cm} \times 1 \text{ cm}$ solar cells measured under 100 mW/cm^2 illumination (AM 1.5G) at 25°C . It should be highlighted that the measured PCE does not account for the $\sim 10\%$ optical shading from the front side contacts. From Fig. 2 inset, low V_{oc} values of all cells can be associated with the usage of moderately low resistivity Si substrate of $\sim 4\text{--}10 \text{ }\Omega\cdot\text{cm}$, as compared to an optimal base resistivity of $\sim 1 \text{ }\Omega\cdot\text{cm}$ that is often used.^{3,5,7,10} The solar cells with epi-emitter have lower V_{oc} values than the diffused emitter cell. With the abrupt p-n junction in the epi-emitters, a higher V_{oc} value is expected due to lower recombination within the narrower depletion region.⁹ However, the lower calculated shunt resistance (R_{SHUNT}) values of the solar cells with epi-emitter, as compared to diffused emitter cell, indicate recombination losses possibly due to defects within the epi-emitter. The poor FF for all cells can be explained by the calculated high series resistance (R_{SERIES}) due to the high line resistivity of the thin front metallization ($\sim 800 \text{ nm}$) and low surface doping concentration ($\sim 4.5 \times 10^{18} \text{ cm}^{-3}$). Due to the lower V_{oc} and FF of the cells with epi-emitter, we can expect that a higher PCE ($(7.5 \pm 0.4)\%$) of the diffused emitter cell. Interest-

FIG. 2. Illuminated and *pseudo* current density-voltage (JV) characteristics of the solar cells with epi-emitters and the reference POCl_3 diffused solar cell. The inset shows the solar cell parameters of $1 \text{ cm} \times 1 \text{ cm}$ solar cells under AM 1.5G illumination.

ingly, the PCE of cell with epi-emitter grown at 700°C is $\sim 50\%$ higher than that grown at 900°C . This is attributed to the calculated R_{SERIES} of the latter cell being almost twice the R_{SERIES} of the cell with epi-emitter grown at 700°C .

Fig. 3 illustrates the external quantum efficiency (EQE) of the solar cells, which correlates well with their respective short-circuit current density (J_{sc}) as presented in Fig. 2 inset. Poor blue EQE response indicates that the surface passivation is insufficient. It is also evident that front surface recombination is more severe in the cells with epi-emitter than that in the diffused emitter cell. This can be attributed to three reasons: (1) the presence of dead layer due to the higher dopant concentration within the epi-emitter (Fig. 1) that reduces minority carrier lifetime;¹² (2) poorer surface passivation since doping level affects the Si oxidation rate;² and (3) defective epi-emitters as deduced from the calculated R_{SHUNT} values. In the spectral region from 550 to 850 nm , it is clear that the minority carrier diffusion length within the epi-emitter grown at 700°C is higher than that of the epi-emitter grown at 900°C . This observation suggests that lower growth temperature produces a better quality Si epilayer.³

High resolution transmission electron microscopy (HRTEM) analysis reveals the presence of mechanical twins and stacking faults at the interface between the epi-emitter and the Si substrate (Figs. 4(a) and 4(b)). These defects are likely to be caused by the incomplete oxide removal at the substrate surface prior to epitaxial growth,¹³ which corroborates well with the high oxygen level at the emitter-substrate interface measured from SIMS analysis. Such structural abnormalities will contribute to material-induced shunt due to strongly recombinative crystal defects,¹⁴ thus corresponding to the lower V_{oc} and R_{SHUNT} values obtained.

In summary, it has been demonstrated that lower growth temperature at 700°C produces a more defined p - n junction with lesser defect, as compared to the epilayer grown at 900°C . A relatively good PCE of $(6.6 \pm 0.3)\%$ was achieved for the solar cell with epi-emitter grown at 700°C , despite the presence of stacking faults due to oxygen contamination. The PCE will be up to 7.3% if the front contact shading is neglected. A *pseudo* PCE of $(10.2 \pm 0.2)\%$ obtained for this solar cell suggests that low temperature Si epitaxy has the

FIG. 3. External quantum efficiencies of the solar cells with epi-emitters and the reference POCl_3 diffused solar cell.

FIG. 4. HRTEM images of (a) epi-emitter grown at 700 °C and (b) epi-emitter grown at 900 °C, illustrating the quality of the emitter-substrate interface.

potential to be used for radial p - n junction growth on wire array solar cells and can be synergistically integrated to high temperature Si epitaxy to realize better performance epitaxial thin film Si solar cells.

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