Meta-stability immunity technique for high speed SAR ADCs

L. Qiu, K. Tang✉, Y.J. Zheng and L. Siek

An 8-bit 4 GS/s 8-channel time-interleaved successive approximation register (SAR) analogue-to-digital converter (ADC) is presented. To enhance the ENOB (effective number of bits), a meta-stability immunity technique is proposed, which utilises pre-installation to eliminate uncertain decision. The technique has negligible design overhead in terms of power and silicon area. The ADC chip was fabricated in a 65 nm CMOS technology. It achieves an ENOB of 7.45 bits, with 48 mW power consumption and an area of 0.075 mm^2.

Introduction: Successive approximation register (SAR) analogue-to-digital converters (ADCs) are power efficient and compact. Therefore, they are widely used in low power implementations. In asynchronous SAR ADCs, time-out detection is adopted [1] to prevent the error caused by meta-stability. In synchronous SAR ADCs, if the input is very small, the occurred meta-stability possibly leads to conversion errors. Further, it causes ENOB (effective number of bits) degradation. In this Letter, a meta-stability immunity technique is proposed. It eliminates the time budget for small input regeneration and increases the conversion speed.

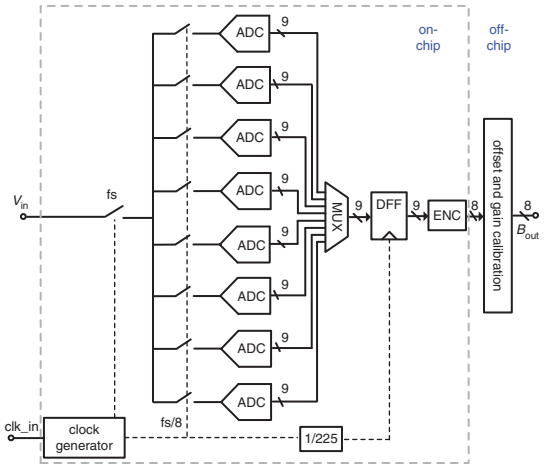

Fig. 1 *Overall 8-channel TI SAR ADC*

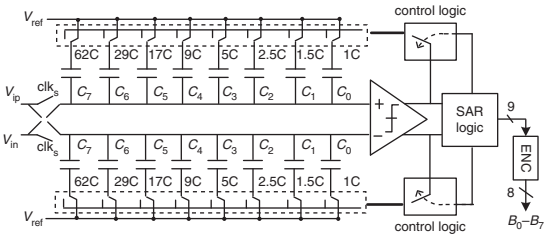

Fig. 2 *Architecture of high speed single-channel SAR ADC*

Proposed meta-stability immunity technique: The time-interleaved (TI) SAR ADC architecture is shown in Fig. 1, which consists of 8-channel TI sub-SAR ADCs operating up to 500 MS/s with total 4 GS/s. A full rate input clock *clk_in* is fed into the on-chip clock buffer, which reshapes the full rate clock signal with fixed pulse width for sampling phase. Also, the clock generator outputs auxiliary clocks with frequency divided by eight for channel selections. The sub-channel SAR ADC utilises non-binary approximation scheme to boost the conversion speed. The redundant 9-bit output is encoded to 8-bit binary output by encoding circuits (ENC) reported in [2]. The offset and gain calibration are done off-chip. To relief the output driven requirement, the full-rate output is down-sampled by a factor of 1/225 to evaluate the ADC performance. The block diagram of the sub-channel SAR ADC is shown in Fig. 2. To shorten the required the DAC settling time, the non-binary successive approximation algorithm [2] is utilised. The non-binary weights are 124 (62C × 2), 58 (29C × 2), 34 (17C × 2), 18 (9C × 2), 10 (5C × 2), 5 (2.5C × 2), 3 (1.5C × 2) and 2 (1C × 2), 1, with redundant rates of 3.1, 12.9, 10.3, 11.7, 11.1, 29, 16.7, 0 and 0%. The proposed meta-stability immunity technique is illustrated in Fig. 3, where a two-bit conversion is taken as an example. In Fig. 3*a*, with the given timeline for each cycle of synchronous conversions, there always are uncertain decision zones near the thresholds due to the presence of meta-stability. The value of the uncertain decision zone is

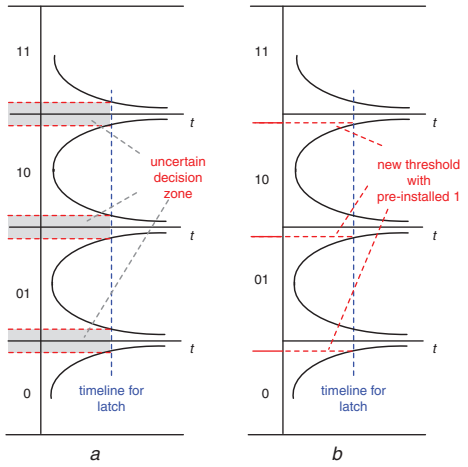

Fig. 3 *Illustration of the proposed meta-stability immunity techniques*
a Conventional conversions with meta-stability zones
b Proposed meta-stability immunity technique with preinstalled 1 in latches

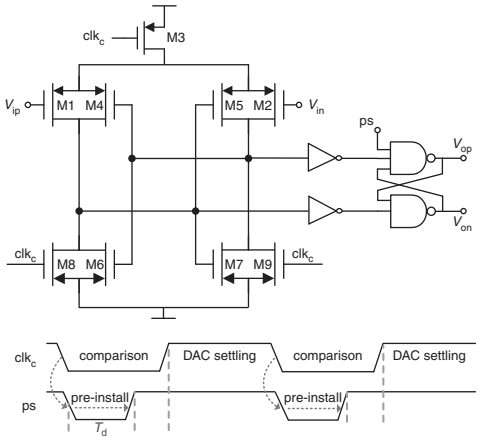

Fig. 4 *Schematic of comparator and latch with pre-installation*

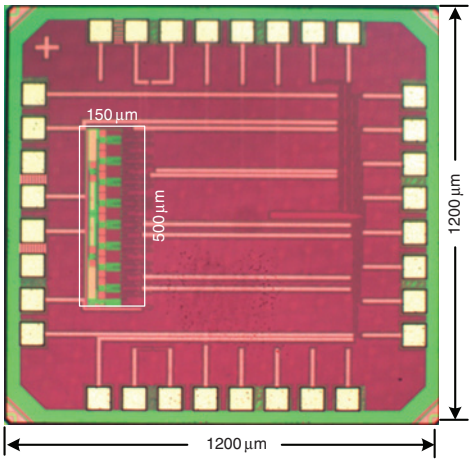

Fig. 5 *Die photo*

$$V_{\text{in-small}} = V_{\text{dd}} \cdot \text{e}^{-(T_{\text{c}}/\tau)} \quad (1)$$

where V_{dd} is the power supply (full swing of latch output), T_{c} is the time period for comparison and τ is the time constant for latch regeneration.

In Fig. 3*b*, it can be seen that if the output of latch is preinstalled as 0 (or 1) for each cycle, the latch output will keep 0 (or 1) when the meta-stability happens. Therefore, the uncertain decision zone is replaced by preinstalled 0 (or 1), with no uncertain zones and no ENOB degradation. In addition, the meta-stability immunity technique introduces a system offset, which is the same as $V_{\text{in-small}}$. The offset is much less than one least significant bit (LSB) and can be easily compensated at digital backend. The operation of the pre-installation and conversion is shown in Fig. 4. The dynamic comparator is followed by a latch with pre-installation function. When the signal *ps* is '0' and clk_c is '1', the positive output V_{op} is forced to be '1'. The timing diagram of clk_c and *ps* is also shown in Fig. 4. The falling of clk_c triggers the *ps* to be '0'. After a certain delay T_d, the *ps* goes back to '1' before DAC settling to give way to the real comparison decision. If it is hard for the comparison making decision. The default output is V_{op} = '1' (V_{on} = '0').

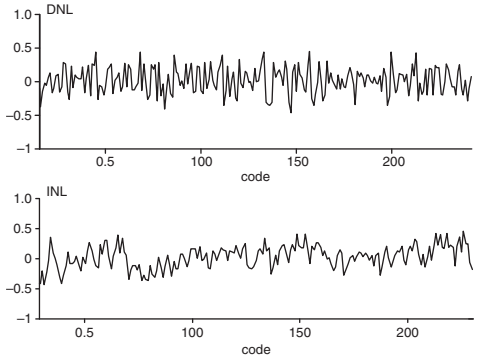

Fig. 6 *Measured DNL and INL*

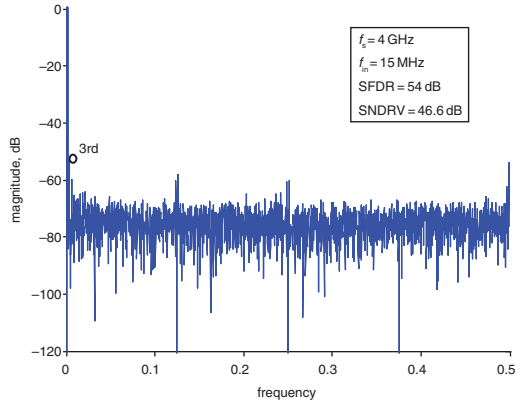

Fig. 7 *Measured 8192-point FFT of 15 MHz input with 4 GS/s*

Table 1: Performance comparisons of GS/s ADCs with 8-bit resolution

	CICC 2014 [3]	JSSC 2013 [4]	JSSC 2014 [5]	This Work
Amplifier Architecture	TI-SAR	SAR	TI-Pipeline	TI-SAR
Technology	40 nm CMOC	32 nm CMOS	65 nm CMOS	65 nm CMOS
Supply voltage (V)	1.2	1.0	1.2	1.2
Power (mW)	39	3.1	120	48
Sampling rate (GS/s)	2.64	1.2	4	4
Resolution	8	8	8	8
SNDR at DC frequency	42.8	39.3	46	46.6
ENOB	6.8	6.24	7.35	7.45
FOM (fJ/conversion-step)	132.6	34.2	183.9	68.6
Area (mm^2)	0.18	0.0015	1.35	0.075

Measurement results: The layout the ADC chip is fabricated in a 1P9M 65 nm CMOS process with low-V_{th} option. The die photo is shown in Fig. 5. The test chip occupies 1200 × 1200 µm, while the dimensions of ADC core are 300 × 500 µm (0.075 mm^2). Instead of using power hungry reference buffer, a decoupling capacitor of 200 pF is used to guarantee the fluctuation of reference voltage to be negligible. The power consumption is 48 mW at 1.2 V power supply when operating at 4 GS/s, with each sub-channel SAR ADC consuming 5.5 mW, and 4 mW for the clock generation and multiplexing. The capacitance of each single-end input sampling DAC array is 128 fF (128C, each unit capacitor C of 1 fF) excluding parasitic capacitance. The measured differential non-linearity (DNL) and integral non-linearity (INL) are shown in Fig. 6. The peak DNL is +0.4/−0.45 LSB and peak INL is +0.42/−0.47 LSB. The 8192-point fast Fourier transform (FFT) of an input of 15 MHz at 4 GS/s is shown in Fig. 7, where the measured spurious free dynamic range (SFDR) and signal to noise and distortion ratio (SNDR) are 54 and 46.6 Db, respectively. By using the proposed meta-stability immunity technique, the ADC could achieve an effective number of bits (ENOB) of 7.45 bits at 15 MHz input frequency. Compared with 8-bit ADCs at GS/s in Table 1, the proposed ADC achieves a better ENOB (7.45 bits). Moreover, it achieves a low figure of merit (FoM) value of 68.6 fJ/conversion-step and small die size of 0.075 mm^2.

Conclusion: A test chip of an 8-channel 8-bit SAR ADC with sampling rate up to 4 GS/s, adopting non-binary searching algorithm, is proposed. With the presence of meta-stability immunity technique, the ADC could achieve a better ENOB of 7.45 bits. Moreover, this technique save time budget for conversion. Therefore, it increases the operation frequency of the ADC.

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One or more of the Figures in this Letter are available in colour online.

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