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A 0.4 V 12T 2RW Dual-Port SRAM with Suppressed Common-Row-Access Disturbance

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Keywords: Static random access memory (SRAM), dual-port, common-row-access, ultra-low voltage.

ABSTRACT

Dual-port SRAMs with two sets of address bus and data IOs are desirable in implantable medical devices to increase throughput at low voltages. Conventional 8T dual-port SRAM

suffers reliability issue at low voltages due to common-row-access disturbance. Specifically, a row is simultaneously accessed by two operations, which can flip existing data and cause incorrect read output. Previous work can address this stability issue by assisting circuitry at cost of timing. This paper presents a low voltage 12T 2RW SRAM featuring parallel access with suppressed disturbance to ameliorate the problem without performance degradation. The proposed SRAM cell suppresses the disturbance by separating read path from internal nodes and minimizing the probability of the worst case stability with area penalty of 6%. In addition, hierarchical bitlines and a virtual ground technique are employed to further lower the minimum operating voltage and power consumption. A 16 kb SRAM has been fabricated in a 65nm CMOS technology and extended the operating voltage from super-threshold region to 0.4V at common-row-access scenario.

1. INTRODUCTION

From motion estimation core to multimedia SoC, ubiquitous computing necessitates high data bandwidth and multi-core processing ability, which are hardly implemented without SRAMs [1]-[9]. Emerging medical products, such as EEG/Neural implantable devices demand medium to high throughput for faster analysis and consequent alarm while maintain low energy consumption. It can be realized by low voltage dual-port SRAMs. These energy-constrained systems consume low power by making operating voltage at near-/sub-threshold region while double throughput by simultaneous operations thanks to dual-port SRAMs. For example, the low voltage dual-port SRAM circuit is beneficial for hardware accelerating in implantable neural devices. It can achieve dual-port pipeline processing ability and consequently increase analysis accuracy/speed by taking advantage of two sets

of address bus and data IOs [10]. Although raising supply voltage can increase performance as well, this method dissipates much more power/energy which is not advocated for implantable applications.

Conventional 8T dual-port (DP) SRAM cells are derived from standard 6T single-port (SP) SRAM cells [3]-[6]. They inherit the weakness of the 6T SRAM cells at low voltage like poor cell stability, reduced read-ability and write-ability, which impedes voltage scaling. These issues are exacerbated as the 8T DP SRAM cell has two more access transistors leading to easier disturbance, especially in the common-row-access mode where two read operations are performed at a selected row simultaneously [4]. This limits the minimum operating voltage (V_{min}) and makes DP SRAM work at higher voltage compared to SP SRAM. Various circuit techniques have been proposed to either improve read-/write-ability of the 8T DP cell or reduce the read-write disturbance under the common-row-access mode. A wordline-voltage-adjustment system is utilized in [3] to improve read and write operation against process, voltage and temperature variations. A priority row decoder with bitline shifter is proposed to circumvent the common access mode [4] for cell stability enhancement. It is obvious that the 8T DP SRAM cell has to employ assisting circuits to accommodate challenges from aggressive voltage scaling. A two-port 6T SRAM cell with reduced area is capable to suppress simultaneous access disturbance when one port is accessed for read and the other is for write [11]. However, the cell cannot support simultaneous read as well as simultaneous write. Hereby new SRAM cell circuit for fully simultaneous read or write (2RW) deserves exploration.

In this paper, we propose a 12T 2RW SRAM cell with two decoupled read ports to significantly reduce common-row-access disturbance and achieve better read-ability and

cell stability. The subsequent increasing of read bitline leakage is suppressed by virtual-ground scheme. Besides, a hierarchical bitline scheme is deployed to improve the performance and the power. These techniques further lower V_{min} to 0.4V and reduce the energy to 8.9pJ, which is 1/5 of the consumption at 1.2V. As an extended version of [12], this manuscript is enhanced by substantial architecture/block details, extensive design technique simulations and more measurement results.

2. DESIGN TECHNIQUES OF THE 12T 2RW DUAL-PORT SRAM CIRCUIT

2.1. 12T Dual-port SRAM Cell Design

Dual-port SRAMs boost computation throughput by doubling memory access. Fig. 1 depicts the conventional 8T DP SRAM cell. Port A and B are accessed by its own address bus and operation signal. Each port consists of its exclusive wordline (WL) and a pair of bitlines (BL and /BL). In the common-row-access mode, the selected cell is inevitably disturbed through the selection of the other WL. Thus, the width of the 2 NMOS drive transistors has to be further increased (e.g. $\times 2.7$) to maintain the cell stability. However, this sizing method is not efficient because the size is not sufficient against disturbance when voltage is lowered to near-/sub-threshold regime. Continue increasing size is not realistic as

Therefore, dual-port SRAM cells with small bitline disturbance are highly required.

Fig. 2 and Fig. 3 portrays the proposed 12T SRAM schematic and layout, respectively. The proposed cell decouples read paths from write path in each port, such as [7]. The read wordlines (RWLA and RWLB) control the access to read paths while write wordlines (WWLA and WWLB) activate data writing. As the SRAM addressing system is for two parallel data access, the 12T SRAM is categorized as dual-port memory although its physical ports are

more than two. The layout of the SRAM cell uses a logic design rule and has a dimension of $3.82\text{ }\mu\text{m} \times 0.72\text{ }\mu\text{m}$ (Fig. 3(a)). Metal 5 is utilized to simplify the signal connecting and routing (Fig. 3 (b)). For 2RW operation, two row decoders are implemented at both sides of the cell array as illustrated in Fig. 4. The conditional discharging of the read bitlines (RBLA and RBLB) is manipulated by VGND employed to suppress leakage. During read, the voltage level of RBLB represents the opposite value of node Q, hence it is connected to a global bitline via a PMOS transistor for inversion. By separating the read paths from the write paths, the amount of read-write disturbance is significantly relaxed and various design metrics such as stability and read/write margins are improved. This will be further discussed in Section 3. The proposed cell eliminates the necessity of over-sizing of the pull down devices while maintains the performance. To make a fair comparison with [5], the benchmark cell has been redesigned using the same logic rule. As Table I shows, the 12T cell shows the area overhead of $\sim 6\%$ for lowering $V_{\min}$ down to 0.4 V. However, the SRAM in [5] can only support nominal voltage operations.

2.2. Virtual Ground (VGND) for Bitline Leakage Reduction

During non-read cycles, RBL is conventionally precharged to a high voltage level and the source terminal of M2 or M4 is normally grounded. This creates leakage current paths from M1 to M2 and M3 to M4. Since the proposed 12T cell doubles the read paths than the conventional single-port cell [7], it is necessary to minimize the RBL leakage for power saving. To address this, a virtual ground technique is employed by controlling the source voltage of M2 and M4 for leakage suppression. Fig. 4 shows the control circuit to implement the virtual ground scheme. Only during read operation, the corresponding VGNDs of the

selected columns are grounded. Otherwise, it is pulled-up to VDD to eliminate the RBL leakage. Fig. 5 plots the waveforms of the VGND circuit when it operates as low as 0.3 V in non-standby mode (NOP = 0). Simulation shows the standby RBL leakage at 0.4 V is correspondingly reduced by 73%. While virtual ground technique fully functions down to 0.3V, the actual minimum operating voltage for the whole chip is 0.4V according to the measurement, which will be analyzed in Section 4.

2.3. Hierarchical Bitlines

Hierarchical bitlines are beneficial to SRAM operations in several aspects such as disturbance mitigation, power reduction, and performance improvement. This work also adopts the hierarchical bitline scheme. In this scheme, a global bitline connects with multiple local bitlines. The local bitline attaches a fraction of total cells and thus has smaller bitline capacitance, which can boost charging/discharging speed. Refined division causes faster local bitline operations but increases local bitline to global bitline delay as well as control complexity.

Fig. 6 shows the correlation between the division ratio and the write performance. The maximum performance is achieved when the write bitlines are divided into eight local write bitlines. However, the performance improvement from four local write bitlines to eight local write bitlines is not significant but area overhead is reduced by $\sim 50\%$. Therefore, four local write bitlines, each of which attaches 64 cells, are implemented due to less area overhead and routing complexity.

3. DISTURBANCE ANALYSIS OF THE PROPOSED 12T SRAM IN COMMON-ROW-ACCESS MODE

Dual-port (DP) SRAMs have various access modes based upon row and column selection. Worst case disturbance occurs when two selected SRAM cells are in the same row, which is called common-row-access. Fig. 7 illustrates the circumstance of the common-row-access for the conventional 8T DP SRAM. In Fig. 7(a), two SRAM cells are accessed in the selected row via two ports, respectively. In Fig. 7(b), only one DP cell is accessed by the two ports. In both cases, the selected cells are disturbed by the current flowing from bitlines to cell nodes through two activated access devices. In addition, like the conventional SRAMs, the half-selected cells also suffer from the same disturbance coming from two enabled WLs. In the 12T SRAM, worst case disturbance also occurs in the common-row-access mode. However, the proposed 12T SRAM cell has better cell stability against disturbance, which will be explained in the following sections.

3.1. Read Disturbance

The read disturbance issue of the conventional 8T DP SRAM cell is described in Fig. 8. When the port A and B are enabled for reading or writing, disturbing current flows from the precharged bitlines to the node of '0' through two access transistors. This degrades read speed and cell stability, and can eventually result in read failure or data flipping [7]. However, in the proposed 12T SRAM cell, the read disturbance is ameliorated in two ways. First, since the read port and the write port are separated, the worst case read disturbance occurs when a write wordline (WWLA/WWLB) is enabled together with a read wordline (RWLA or RWLB). Fig. 9 depicts the worst case disturbance which is applicable to the 12T SRAM cell.

The disturbance current has no interference with read current. Therefore, the read stability of the proposed 12T SRAM cell is better than that of the conventional 8T DP SRAM cell. Second, when two simultaneous read operations are executed in the same row, they are interference-free due to the decoupled read ports, which is not the case in the conventional DP SRAM. The read stability under this condition is thus equal to the hold stability. Fig. 10 shows sample waveforms in the worst case read conditions for comparing the disturbance of the proposed SRAM with that of the conventional DP SRAM. It can be seen that the data in the 12T SRAM cell is secured while the data in the 8T cell flips at the worst case. In addition, better read-ability is achieved by the decoupled read port, which is free from disturbance current. A 500-point Monte Carlo simulation (Fig. 11) validates that the cell instability of the 12T SRAM is $5\times$ less than that of the 8T DP SRAM with supply of 0.4 V. The Monte Carlo simulation is executed in 500 runs instead of normal 1000 runs because the server has limit capability for substantial waveform plotting.

3.2. Write Disturbance

The main challenges in the write operation of DP SRAM cells are write margin and the stability of half-selected cells. The worst case write disturbance is shown in Fig. 12. When writing '0' through a write port (Port A), the pull-up disturbing current through the other port (Port B) degrades the discharging speed. This condition exists in both SRAM cells. Fig. 12 exhibits the voltage of QB under the worst case write disturbance, which should be '0' after a successful write. Specifically when Port A is activated, voltage of QB is quickly pulled down. Due to the disturbance current from Port B, the node voltage is pumped to tens of mV amplitude. The 1k-pt Monte-Carlo simulation with 3σ mismatch on top of TT corner (Fig. 13)

shows a mean QB voltage of 35 mV with one sigma of 15 mV during write operation with a supply voltage of 0.4 V. No QB flips after write completion with the presence of worst case write disturbance. The accessed cell in the 12T SRAM is secured for write at this condition. Note that all Monte-Carlo waveforms are not extracted for Iso-area condition.

3.3. Summary of Disturbance Analysis

Both the 12T SRAM cell and the 8T DP SRAM cell have the same worst case disturbance condition. It occurs in the half-selected cells where two write ports are enabled. However, in the 12T SRAM cell, the probability of the worst case disturbance condition is much lower than that of the conventional DP SRAM cell. Fig 14 illustrates the worst case disturbance conditions in the conventional and 12T SRAM cells. In the conventional DP SRAM cell, the worst disturbance conditions occur during non-write operations in the common-row-access mode. Out of 16 possible cases, 9 cases are under the worst disturbance condition. However, in the 12T SRAM cell, the worst case disturbance will occur only when both ports are activated by the half-selection condition during 2W operation.

This worst case condition can be avoided in actual applications by changing memory access mode slightly. The disturbance analysis also indicates that other decoupled SRAM cells can also be utilized for 2RW SRAMs.

4. MEASUREMENT RESULTS

The 12T SRAM was fabricated in 65nm CMOS technology. The architecture of the 12T SRAM is depicted in Fig. 15. Note that each port has dedicated peripheral circuits such as control logic, decoders, read-out circuits, I/Os, etc. The 16Kb array is configured by 256 rows

$\times 64$ columns. The test chip occupies the area of $398 \times 385 \mu\text{m}^2$. Fig. 16 shows the measured read access time (non-simultaneous read) of the 12T SRAM. At 0.3 V, the read access time of 6.0 μs was achieved including the delay of the I/O circuits and level shifters. The measured leakage is described in Fig. 17. At 0.4 V, the leakage current is 7.6 μA , which is reduced by 88% compared to the leakage at 1.2 V.

Common-row-access mode is especially tested to validate the proposed SRAM circuit. In this scenario, power and energy are calculated via current when simultaneous access occurs at a common row. Both read and write current are averaged by different patterns with respect to the dual port SRAM. The measured total power at common-row-access mode is depicted in Fig. 18. With equal probability of read and write, the average power at 1.2V is 101 $\mu\text{W}/\text{MHz}$. Fig. 19 shows the measured energy per operation of the 12T SRAM. The minimum energy of 8.9 pJ was obtained at 0.5 V, which is dominated by read operation. Fig. 20 displays the screenshot of the common-row-read output at 0.4 V. The 12T SRAM demonstrates the lowest operating voltage (V_{min}) for common-row-access without using any read/write assist circuits. This is accomplished mainly due to the separated read ports for eliminating most of the worst disturbance cases. Employing read/write assisting circuits can further improve V_{min} . Tabel I compares the 12T DP SRAM chip with the 8T DP SRAM (logic rule) in [5].

5. CONCLUSION

Near-/Sub threshold dual-port SRAMs are required by medical hardware accelerators for better data processing capability with relatively low power/energy. This paper presents a 12T 2RW SRAM for low voltage operation. The 12T SRAM improves the cell stability by

decoupling read path and eliminating most of the worst case scenarios existing in the previous DP SRAMs. A test chip demonstrates the successful 2RW operation at common-row-access mode down to 0.4 V. The 12T SRAM also reveals that other SRAMs with decoupled read ports can be used for minimizing the probability of worst disturbance cases in the common-row-access mode.

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Figure Captions

Figure 1. schematic of conventional 8T dual-port SRAM cell.

Figure 2. Proposed 12T 2RW SRAM cell.

Figure 3. (a) Front-end layout of 12T dual-port SRAM cell; (b) Back-end layout of 12T SRAM cell.

Figure 4. Architecture of 12T 2RW SRAM.

Figure 5. Simulated virtual ground waveforms at $V_{DD} = 0.3$ V.

Figure 6. Hierarchical bitline analysis over various division ratios.

Figure 7. Simplified illustration of common-row-access in the conventional DP SRAMs (a) two selected DP cells in a row and (b) one selected DP cell in a row.

Figure 8. Worst case read disturbance in the conventional 8T DP SRAM cell. Note that the cell is accessed for read through port A while port B is under the half-selected condition.

Figure 9. Worst case read disturbance in the 12T SRAM cell. Note that the cell is accessed for read through port A while port B is under the half-selected condition.

Figure 10. Simulated waveforms comparing the worst case read disturbance of the proposed SRAM with the conventional 8T DP SRAM at FNSP corner and 27°C .

Figure 11. (a) Simulated waveforms comparing the read disturbance of the proposed SRAM with the conventional 8T DP SRAM (a) at FNSP corner and 27°C ; (b) from a 500-pt Monte-Carlo simulation at TT corner with 3σ mismatch and 125°C .

Figure 12. Worst case write disturbance in the conventional and 12T SRAM cells. Note that the cell is accessed for write through port A while port B is under the half-selection condition [9].

Figure 13. Histogram of node QB voltage under the worst case write disturbance (Fig.12) from a 1k-pt Monte-Carlo simulation at TT corner with 3σ mismatch and 125°C .

Figure 14. Probability of the worst case SNM in the common-row-access mode. Note that the 12T SRAM has only one worst SNM case out of sixteen scenarios while the conventional DP SRAM shows nine worst SNM cases.

Figure 15. 12T SRAM: (a) architecture and (b) microphotograph.

Figure 16. Measured access time of the proposed SRAM.

Figure 17. Measured leakage of the proposed SRAM.

Figure 18. Measured total power with common-row access.

Figure 19. Measured energy with common-row access.

Figure 20. Screenshot of data output at common-row-read circumstance.

Table I Comparison of this work with 8T DP SRAM in [5] (logic rule)

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(b)

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SRAM Cell	V _{min}	Leak. (uA)	Area (um ²)	Total power (mW/MHz)	Access Time (ns)
This work	0.4	63	2.254 (65nm)	0.101	6.5
SRAM in [5]	1.2	6.85	2.94 (90nm)	~0.226	NA