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Abstract: The model predictive control (MPC) is a promising control method for cascaded H-bridge (CHB) rectifiers. One well-known MPC method is the finite-control-set MPC (FCS-MPC). However, three main issues arise in FCS-MPC: heavy computational burden, low steady-state performance, and time-consuming tuning work of weighting factor. Here, an alternative MPC method, deadbeat (DB) control with a capability of voltage balance, has been proposed for a single-phase CHB rectifier. The proposed method is based on the DB solution to obtain zero current error at the sampling instant and the use of a redundancy-based modulation strategy for voltage balance, leading to the ease of controller design and elimination of tuning work. The proposed method has been evaluated against FCS-MPC method on a single-phase three-cell CHB rectifier. The experimental results show that a reduced computational burden, an improved steady-state performance, and a comparable dynamic response can be achieved in the proposed method in comparison with FCS-MPC method.

1 Introduction

Multilevel converter provides a cost-effective solution in the medium-voltage high-power energy conversion system. Of the multilevel converter topologies, the cascaded H-bridge (CHB) converter has received considerable attention in industry because of its modularisation and extendibility [1]. The main drawback of CHB converter is the multiple isolated dc supplies needed when it is used as an inverter [2]. However, whenever the converter is used as a rectifier, it is even more attractive due to the available distinct dc-links feeding separate loads [3–15]. This feature makes CHB rectifier an appealing topology to be used, for example, in traction applications [3] and solid-state transformers (SSTs) [5, 6, 8].

The CHB rectifier normally aims to obtain a sinusoidal current on the ac side and to establish equal voltages across individual capacitors on the dc side. Several control methods have been presented for CHB rectifiers [4–15]. Some of them rely on a combination of multiple proportional–integral (PI) controllers which regulate power flow at each H-bridge [4–7]. The others achieve voltage balancing through redundancy-based modulation strategies and control ac-side current by cooperating with PI controller [8], adaptive resonant controller [9], hysteresis current controller [10], or selective harmonic elimination method [11–13]. Despite the effectiveness of the aforementioned methods, there are still open tasks such as ease of controller design and elimination of tuning work.

In last decade, model predictive control (MPC) method has been introduced into the control of multilevel converters [16–19], including works on CHB converter operated as either an inverter [20–22] or as a rectifier [14, 15]. One of MPC methods, named finite-control-set MPC (FCS-MPC), has been reported for CHB rectifiers in [14]. In FCS-MPC method, a cost function presenting the errors of controlled variables is evaluated for each possible switching state for a predefined horizon. The optimal switching state which minimises the cost function is selected and applied in the next sampling period. However, three main issues arise in FCS-MPC method for CHB rectifier. The first is that the computational burden associated with the number of switching states increases exponentially as the number of cells in CHB rectifier is added. The second is the larger current ripples and errors generated in steady state due to only switching state applied for the entire sampling period, which, in turn, requires an increased sampling frequency in

comparison with modulation-based control methods. The third issue is that FCS-MPC method handles multiple control objectives in single cost function through the weighting factor, but the tuning work of weighting factor is time-consuming.

An alternative MPC method is the deadbeat (DB) control (DBC). This method obtains the desired voltage by nullifying the error of controlled variable at the end of the next sampling period and then uses a modulator to apply the desired voltage to the converter [15, 23, 24]. In comparison with FCS-MPC method, the current control of CHB rectifier in DBC method is achieved by considering voltage level instead of switching state, where therefore a reduced computational effort is obtained. Moreover, DBC applies two output voltages with their durations per sampling period, leading to an improved steady-state performance. In DBC method, the voltage balancing of CHB rectifier can be dealt with in the modulation stage and therefore the use of weighting factor is avoided, leading to the elimination of a time-consuming tuning work. The DBC method has been presented for CHB rectifier in [15], where, however, the voltage balancing modulation has not been explored.

In this paper, a DBC method with voltage balancing modulation has been proposed for a single-phase CHB rectifier. In the proposed method, a combination of two adjacent voltage levels along with their durations are obtained on the basis of DB solution to eliminate the current error at the next sampling instant. A redundancy-based modulation algorithm is derived to provide the capability of voltage balance. Finally, the proposed method has been evaluated against FCS-MPC method in experimental test on a single-phase three-cell CHB rectifier. Nevertheless, the proposed method can be easily extended to a single-phase CHB rectifier with more cells.

This paper is organised as follows. In Section 2, the description of CHB rectifier is described. In Section 3, the FCS-MPC method is reviewed to obtain a fair comparison. In Section 4, the proposed method is presented. Experimental results are presented in Section 5. Finally, the conclusion of this paper is addressed in Section 6.

2 Description of single-phase CHB rectifier

Fig. 1 shows the topology of single-phase three-cell CHB rectifier, which consists of three H-bridges connected in cascade. v_s and i_s are the source voltage and current, respectively. L_s is the boost

inductor and R_s is the equivalent resistor for the inductor and wires. C_i and R_i ($i = 1, 2, 3$) are the dc capacitor and resistive load attached to the individual H-bridge. The dc load may be passive in nature or possibly active converter. S_{ij} ($i = 1, 2, 3; j = 1, 2, 3, 4$) stands for switches in each H-bridge.

Define the switching function as

$$P_i = \begin{cases} 1, & S_{i1}, S_{i4} \text{ turn on} \\ 0, & S_{i1}, S_{i3} \text{ turn on or } S_{i2}, S_{i4} \text{ turn on} \\ -1, & S_{i2}, S_{i3} \text{ turn on} \end{cases} \quad (i = 1, 2, 3) \quad (1)$$

The total ac-side voltage v_{HT} of CHB rectifier can be given as

$$v_{HT} = v_{H1} + v_{H2} + v_{H3} \quad (2a)$$

$$v_{Hi} = P_i v_{Ci} \quad (i = 1, 2, 3) \quad (2b)$$

where v_{Hi} and v_{Ci} are the ac-side and dc-link voltages of the i th H-bridge, respectively.

3 FCS-MPC method

The FCS-MPC method for a single-phase CHB rectifier has been proposed and well described in [14], but several details that can serve as the foundation for comparison are included as follows.

Fig. 2 shows the block diagram of FCS-MPC method, where the sum of dc-link voltages is regulated by a PI controller to the reference value. The reference source current i_s^* is synchronised with source voltage v_s by using the normalised source voltage $\hat{v}_s$. The $\hat{v}_s$ can be simply obtained through dividing v_s by its amplitude. As shown in Fig. 2, the FCS-MPC use a prediction model to calculate the future controlled variables on the basis of sampled variables and possible switching states. For simplification, the prediction model of a single-phase CHB rectifier, which can be found in [14], is not addressed in this paper.

In FCS-MPC method, as shown in Fig. 2, the optimal switching state S_{ij} is selected among all possible switching states by minimising the cost function. For a single-phase n -cell CHB rectifier, there are 4^n possible switching states. It results in a considerable computational burden on digital controller since the

Fig. 1 Topology of single-phase three-cell CHB rectifier

Fig. 2 Block diagram of FCS-MPC method

computations increase exponentially as the number of cells is added. In addition, another issue arises in FCS-MPC method due to the fact that only switching state is applied for the whole sampling period. Consequently, an increased sampling frequency has to be used to obtain a higher waveform quality.

The CHB rectifier has intrinsic control problems since each H-bridge aims to establish equal dc-link voltage while it must interact with the others to generate a sinusoidal source current on the ac side. The FCS-MPC handles these two control objectives of CHB rectifier in a cost function, though weighting factor and the cost function for a three-cell CHB rectifier can be defined as

$$g = |i_s^* - i_s| + \lambda_v \sum_{i=1}^3 |v_{Ci}^* - v_{Ci}| \quad (3)$$

where the λ_v is a weighting factor. To obtain a satisfied control performance, a fine tuning of λ_v has to be done, which is a time-consuming work.

In this paper, an alternative MPC method, DBC with voltage balancing modulation, which can overcome the three above-mentioned drawbacks of FCS-MPC method, has been proposed as follows.

4 Proposed control method

Fig. 3 shows the block diagram of the proposed control method. The proposed method is based on the prediction of system response to obtain the desired total ac-side voltage v_{HT}^* by nullifying the error of source current in the next sampling period. To synthesise v_{HT}^* in CHB rectifier, two output voltages $v_{HT}^{(1)}(k)$ and $v_{HT}^{(2)}(k)$ adjacent to v_{HT}^* are selected and their durations $T^{(1)}(k)$ and $T^{(2)}(k)$ are calculated. Then, dc-link voltage balance is achieved in the modulation stage. In the following, the individual parts of the proposed method were explained.

4.1 The desired total ac-side voltage

The total ac-side voltage at the kT_s instant can be expressed in the inverse model of current filter as

$$v_{HT}(kT_s) = -\frac{L_s}{T_s} i_s((k+1)T_s) + \left(\frac{L_s}{T_s} - R_s\right) i_s(kT_s) + v_s(kT_s) \quad (4)$$

Assuming the system is controlled well, the source current $i_s((k+1)T_s)$ becomes equal to the source current reference i_s^* and therefore, the desired total ac-side voltage is derived as

$$v_{HT}^*(kT_s) = -\frac{L_s}{T_s} i_s^* + \left(\frac{L_s}{T_s} - R_s\right) i_s(kT_s) + v_s(kT_s) \quad (5)$$

4.2 Voltage level selection

The desired total ac-side voltage v_{HT}^* is continuous and therefore cannot be applied directly to the converter. Instead, as shown in Fig. 4, two total ac-side voltages $v_{HT}^{(1)}$ and $v_{HT}^{(2)}$ of the CHB rectifier can be selected to achieve zero current error at the next sampling period. The superscripts (1) and (2) of variables mean the first voltage and second voltage to be applied. For $v_{HT}^{(1)}$ and $v_{HT}^{(2)}$, one voltage has to be smaller than v_{HT}^* and the other is larger than v_{HT}^* . To limit the dv/dt , $v_{HT}^{(1)}$ and $v_{HT}^{(2)}$ should be adjacent to each other and therefore, they are also the voltages nearest to v_{HT}^* . Taking a single-phase three-cell CHB rectifier as an example, assuming $v_{C1} = v_{C2} = v_{C3} = \underline{v}_{CC}$ [$\underline{v}_{CC}$ is the average value of all dc-link voltages, as given in (6)], there are eight possible combinations of $v_{HT}^{(1)}$ and $v_{HT}^{(2)}$, as shown in Table 1, where $v_{HT}^{(1)}$ is considered smaller than $v_{HT}^{(2)}$. However, when v_{HT}^* is over the maximum or below the minimum total ac-side voltage of CHB rectifier, no proper combination of $v_{HT}^{(1)}$ and $v_{HT}^{(2)}$ is available to eliminate the current error at the next sampling period. In such case, as shown in Table 1, the maximum

Fig. 3 Block diagram of proposed control scheme

Fig. 4 Source current trajectory with zero error at the sampling instant

Table 1 Combinations of $v_{HT}^{(1)}$ and $v_{HT}^{(2)}$ for a single-phase three-cell CHB rectifier

v_{HT}^*	$[v_{HT}^{(1)}, v_{HT}^{(2)}]$
$v_{HT}^* > 3\underline{v}_C$	$[3\underline{v}_C, 3\underline{v}_C]$
$3\underline{v}_C > v_{HT}^* > 2\underline{v}_C$	$[2\underline{v}_C, 3\underline{v}_C]$
$2\underline{v}_C > v_{HT}^* > \underline{v}_C$	$[\underline{v}_C, 2\underline{v}_C]$
$\underline{v}_C > v_{HT}^* > 0$	$[0, \underline{v}_C]$
$0 > v_{HT}^* > -\underline{v}_C$	$[-\underline{v}_C, 0]$
$-\underline{v}_C > v_{HT}^* > -2\underline{v}_C$	$[-2\underline{v}_C, -\underline{v}_C]$
$-2\underline{v}_C > v_{HT}^* > -3\underline{v}_C$	$[-3\underline{v}_C, -2\underline{v}_C]$
$v_{HT}^* < -3\underline{v}_C$	$[-3\underline{v}_C, -3\underline{v}_C]$

or minimal total ac-side voltage $3\underline{v}_C$ or $-3\underline{v}_C$ is applied during the entire sampling period to minimise the current error

$$\underline{v}_C = \frac{v_{C1} + v_{C2} + v_{C3}}{3} \quad (6)$$

4.3 Durations calculation

By applying $v_{HT}^{(1)}(k)$ and $v_{HT}^{(2)}(k)$, the source current at the $(k+1)T_s$ instant is obtained as

$$i_s((k+1)T_s) = i_s(kT_s) + \sigma^{(1)}(k)T^{(1)}(k) + \sigma^{(2)}(k)T^{(2)}(k) \quad (7)$$

where $\sigma^{(1)}(k)$ and $\sigma^{(2)}(k)$ are slopes of source currents generated by $v_{HT}^{(1)}(k)$ and $v_{HT}^{(2)}(k)$. $T^{(1)}(k)$ and $T^{(2)}(k)$ are the durations of $v_{HT}^{(1)}(k)$ and $v_{HT}^{(2)}(k)$, respectively.

The expressions of $\sigma^{(1)}(k)$ and $\sigma^{(2)}(k)$ are given as

$$\sigma^{(1)}(k) = -\frac{R_s}{L_s}i_s(kT_s) + \frac{v_s(kT_s) - v_{HT}^{(1)}(k)}{L_s} \quad (8a)$$

$$\sigma^{(2)}(k) = -\frac{R_s}{L_s}i_s(kT_s + T^{(1)}(k)) + \frac{v_s(kT_s) - v_{HT}^{(2)}(k)}{L_s} \quad (8b)$$

where $i_s(kT_s + T^{(1)}(k))$ is source current at the change instant of $v_{HT}^{(1)}(k)$ and $v_{HT}^{(2)}(k)$ and can be obtained as

$$i_s(kT_s + T^{(1)}(k)) = i_s(kT_s) + \sigma^{(1)}(k)T^{(1)}(k) \quad (9)$$

Imposing the $i_s((k+1)T_s)$ in (6) to be equal to reference current i_s^* , the DB control law is derived as

$$i_s^* = i_s(k) + \sigma^{(1)}(k)T^{(1)}(k) + \sigma^{(2)}(k)T^{(2)}(k) \quad (10)$$

Based on (10), the $T^{(1)}(k)$ can be calculated by solving a quadratic equation and then two values of $T^{(1)}(k)$ are available as

$$T^{(1)}(k) = \frac{a + bT_s \pm \sqrt{(a + bT_s)^2 - 4bcT_s}}{2b} \quad (11)$$

where $a = v_{HT}^{(1)}(k) - v_{HT}^{(2)}(k)$; $b = (R_s/L_s)[v_s(kT_s) - v_{HT}^{(1)}(k) - R_i i_s(kT_s)]$; $c = v_{HT}^* - v_{HT}^{(2)}(k)$.

One value between 0 and T_s is chosen and the other smaller than 0 or larger than T_s is discarded. Then, $T^{(2)}(k)$ can be calculated by subtracting $T^{(1)}(k)$ from T_s as

$$T^{(2)}(k) = T_s - T^{(1)}(k) \quad (12)$$

4.4 Voltage balancing modulation

The voltage balancing can be dealt with in the modulation stage by utilising the redundant feature of CHB rectifier. That means different switching pairs can generate same total ac-side voltage. Fig. 5 shows all switching pairs (P_1 , P_2 , P_3) to be selected to balance the dc-link voltages of a single-phase three-cell CHB rectifier. To keep all dc-link voltages to be equal, it is required to charge the dc capacitors with their voltages smaller than the average dc-link voltage $\underline{v}_C$ [as given in (6)] and discharge the others whose voltages are larger than $\underline{v}_C$. Which dc capacitor C_i should be charged or discharged can be determined by comparing corresponding dc-link voltage v_{Ci} with $\underline{v}_C$. According to the comparison result, the sort of dc-link voltages is shown in Fig. 5.

For any H-bridge cell, it is obvious that the charge or discharge on dc capacitor will be affected by the direction of i_s and v_{Hi} . The v_{Ci} will increase when i_s times v_{Hi} is positive. Otherwise, the v_{Ci} will decrease. Considering this characteristic, the desired switching pair should be selected on the basis of the direction of i_s . For example, as shown in Fig. 5, if $v_{HT} = 0$ is desired, at the same time, in the case of $v_{C1} > v_{C2} > \underline{v}_C > v_{C3}$, the switching pair $(-1, 0, 1)$ should be selected when $i_s > 0$. Here, v_{C1} and v_{C2} are decreasing

v_{HT}	Possible (P_1, P_2, P_3)	Sort of dc-link voltages	Selected (P_1, P_2, P_3)	
			$i_s > 0$	$i_s < 0$
$3v_c$	(1, 1, 1)	---	(1, 1, 1)	
		$v_{C1} > v_{C2} > v_{C3}$	(0, 1, 1)	
		$v_{C1} > v_{C3} > v_{C2}$	(0, 1, 1)	
		$v_{C2} > v_{C1} > v_{C3}$	(0, 1, 1)	
		$v_{C2} > v_{C3} > v_{C1}$	(0, 1, 1)	
		$v_{C3} > v_{C1} > v_{C2}$	(1, 0, 1)	
		$v_{C3} > v_{C2} > v_{C1}$	(1, 0, 1)	
		$v_{C1} > v_{C2} > v_{C3}$	(1, 0, 1)	
		$v_{C1} > v_{C3} > v_{C2}$	(1, 0, 1)	
		$v_{C2} > v_{C1} > v_{C3}$	(1, 0, 1)	
$2v_c$	(1, 0, 1)	$v_{C2} > v_{C1} > v_{C3}$	(1, 0, 1)	
		$v_{C2} > v_{C3} > v_{C1}$	(1, 0, 1)	
		$v_{C3} > v_{C1} > v_{C2}$	(1, 0, 1)	
		$v_{C3} > v_{C2} > v_{C1}$	(1, 0, 1)	
		$v_{C1} > v_{C2} > v_{C3}$	(1, 1, 0)	
		$v_{C1} > v_{C3} > v_{C2}$	(1, 1, 0)	
		$v_{C2} > v_{C1} > v_{C3}$	(1, 1, 0)	
		$v_{C2} > v_{C3} > v_{C1}$	(1, 1, 0)	
		$v_{C3} > v_{C1} > v_{C2}$	(1, 1, 0)	
		$v_{C3} > v_{C2} > v_{C1}$	(1, 1, 0)	
v_c	(0, 0, 1)	$v_{C1} > v_{C2} > v_{C3}$	(0, 0, 1)	(1, 1, -1)
		$v_{C1} > v_{C3} > v_{C2}$	(-1, 1, 1)	(1, 1, -1)
		$v_{C2} > v_{C1} > v_{C3}$	(0, 1, 0)	(1, -1, 1)
		$v_{C2} > v_{C3} > v_{C1}$	(-1, 1, 1)	(1, -1, 1)
		$v_{C3} > v_{C1} > v_{C2}$	(0, 0, 1)	(1, 1, -1)
		$v_{C3} > v_{C2} > v_{C1}$	(1, -1, 1)	(1, 1, -1)
		$v_{C1} > v_{C2} > v_{C3}$	(1, 0, 0)	(-1, 1, 1)
		$v_{C1} > v_{C3} > v_{C2}$	(1, -1, 1)	(-1, 1, 1)
		$v_{C2} > v_{C1} > v_{C3}$	(0, 1, 0)	(-1, 1, 1)
		$v_{C2} > v_{C3} > v_{C1}$	(0, 1, 0)	(-1, 1, 1)
0	(1, -1, 1)	$v_{C2} > v_{C1} > v_{C3}$	(1, -1, 1)	(-1, 1, 1)
		$v_{C2} > v_{C3} > v_{C1}$	(1, -1, 1)	(-1, 1, 1)
		$v_{C3} > v_{C1} > v_{C2}$	(0, 1, 0)	(1, -1, 1)
		$v_{C3} > v_{C2} > v_{C1}$	(1, 1, -1)	(1, -1, 1)
		$v_{C1} > v_{C2} > v_{C3}$	(1, 0, 0)	(-1, 1, 1)
		$v_{C1} > v_{C3} > v_{C2}$	(1, 1, -1)	(-1, 1, 1)
		$v_{C2} > v_{C1} > v_{C3}$	(-1, 0, 1)	(1, 0, -1)
		$v_{C2} > v_{C3} > v_{C1}$	(-1, 0, 1)	(1, 0, -1)
		$v_{C3} > v_{C1} > v_{C2}$	(-1, 1, 0)	(1, -1, 0)
		$v_{C3} > v_{C2} > v_{C1}$	(-1, 1, 0)	(1, -1, 0)
$-v_c$	(0, 0, -1)	$v_{C1} > v_{C2} > v_{C3}$	(0, -1, 1)	(0, 0, -1)
		$v_{C1} > v_{C3} > v_{C2}$	(-1, -1, 1)	(1, -1, -1)
		$v_{C2} > v_{C1} > v_{C3}$	(-1, 1, -1)	(0, -1, 0)
		$v_{C2} > v_{C3} > v_{C1}$	(-1, 1, -1)	(0, -1, 0)
		$v_{C3} > v_{C1} > v_{C2}$	(-1, -1, 1)	(-1, 1, -1)
		$v_{C3} > v_{C2} > v_{C1}$	(1, -1, -1)	(-1, 0, 0)
		$v_{C1} > v_{C2} > v_{C3}$	(1, -1, -1)	(-1, 1, -1)
		$v_{C1} > v_{C3} > v_{C2}$	(-1, 1, -1)	(-1, 1, -1)
		$v_{C2} > v_{C1} > v_{C3}$	(-1, 1, -1)	(-1, 1, -1)
		$v_{C2} > v_{C3} > v_{C1}$	(-1, 1, -1)	(-1, 1, -1)
$-2v_c$	(1, -1, -1)	$v_{C2} > v_{C1} > v_{C3}$	(1, -1, -1)	(-1, 0, 0)
		$v_{C2} > v_{C3} > v_{C1}$	(1, -1, -1)	(-1, 0, 0)
		$v_{C3} > v_{C1} > v_{C2}$	(-1, 1, -1)	(0, -1, 0)
		$v_{C3} > v_{C2} > v_{C1}$	(-1, 1, -1)	(-1, -1, 1)
		$v_{C1} > v_{C2} > v_{C3}$	(1, -1, -1)	(-1, 0, 0)
		$v_{C1} > v_{C3} > v_{C2}$	(-1, -1, 1)	(-1, 0, 0)
		$v_{C2} > v_{C1} > v_{C3}$	(-1, -1, 1)	(-1, 0, 0)
		$v_{C2} > v_{C3} > v_{C1}$	(-1, -1, 1)	(-1, 0, 0)
		$v_{C3} > v_{C1} > v_{C2}$	(-1, -1, 1)	(-1, 0, 0)
		$v_{C3} > v_{C2} > v_{C1}$	(-1, -1, 1)	(-1, 0, 0)
$-3v_c$	---	$v_{C1} > v_{C2} > v_{C3}$	(-1, -1, -1)	(-1, -1, -1)
		$v_{C1} > v_{C3} > v_{C2}$	(-1, -1, -1)	(-1, -1, -1)
		$v_{C2} > v_{C1} > v_{C3}$	(-1, -1, -1)	(-1, -1, -1)
		$v_{C2} > v_{C3} > v_{C1}$	(-1, -1, -1)	(-1, -1, -1)
		$v_{C3} > v_{C1} > v_{C2}$	(-1, -1, -1)	(-1, -1, -1)
		$v_{C3} > v_{C2} > v_{C1}$	(-1, -1, -1)	(-1, -1, -1)
		$v_{C1} > v_{C2} > v_{C3}$	(-1, -1, -1)	(-1, -1, -1)
		$v_{C1} > v_{C3} > v_{C2}$	(-1, -1, -1)	(-1, -1, -1)
		$v_{C2} > v_{C1} > v_{C3}$	(-1, -1, -1)	(-1, -1, -1)
		$v_{C2} > v_{C3} > v_{C1}$	(-1, -1, -1)	(-1, -1, -1)

Fig. 5 Switching pairs selected to balance dc-link voltages of a single-phase three-cell CHB rectifier

and v_{C3} is increasing. However, in the same condition but with $i_s < 0$, v_{C1} and v_{C2} are decreasing and v_{C3} is increasing when switching pair (1, 0, -1) is selected.

Fig. 6 Calculation flow of the proposed method

4.5 Calculation flow

Fig. 6 shows the calculation flow of the proposed method. As shown in Fig. 6, the proposed method uses two look-up tables (Tables 1 and 2) for selection. The number of cases in these two tables will increase linearly as the number of cells is added. Nevertheless, the proposed methods have a lower computational burden than FCS-MPC method whose computational burden increases exponentially as the number of cells is added. There are four possible switching states for H-bridge cell. As shown in (1), two redundant switching states (S_{i1} and S_{i3} on and S_{i1} and S_{i3} on) can lead to the same switching function ($P_i = 0$). To balance the switchings in each cell, these two switching stages are used alternatively.

5 Experimental results

Experimental tests have been carried out to evaluate the proposed method against FCS-MPC method. Fig. 7 shows the set-up of a single-phase three-cell CHB rectifier. The control method is implemented on a DSpace DS1104 controller. Owing to limited hardware resources in DS1104 controller, a TMS320F28335 digital signal processor is adopted for generating gate signals, which access to each H-bridge through fibreoptics. A 240/120 V step-down isolated transformer is used to connect the grid with the CHB rectifier.

Nominal experimental conditions are listed in Table 2, where f_s is a sampling frequency, T_d is a dead time of gate signals, and K_p along with K_i are parameters of PI controller. To obtain a fair reference, the weighting factor λ_v of FCS-MPC method was well adjusted in experimental test.

5.1 Calculation time

Table 3 shows the calculation time needed in the DSpace DS1104 controller for FCS-MPC method and proposed method, which is measured by using the dSPACE Profiler. As shown in Table 3, the proposed method makes a significant reduction in calculation time in comparison with FCS-MPC method.

5.2 Steady-state performance

Fig. 8 shows the steady-state experimental waveforms of source current, dc-link voltages, and total ac-side voltage and measured spectrum of source current for FCS-MPC method and proposed method. It should be noted that the converter is connected to the grid via a step-down isolated transformer. Therefore, many small spikes appear on the v_s and they are generated by the switching operations. It can be noted from the waveforms and their zoomed-in area in Fig. 8 that both methods can achieve current tracking, but

Fig. 7 Set-up of a single-phase three-cell CHB rectifier

Table 2 Nominal experimental conditions

v_s	120 V RMS/50 Hz	f_s	5 kHz
L_s/R_s	8.6 mH/0.7 Ω	T_d	2 μ s
C_f/R_f	3900 μ F/20 Ω	v_c^*	70 V
K_p/K_i	0.7/2.5	λ_v	1.5

Table 3 Calculation time

Control method	Calculation time, μ s
FCS-MPC	146.585
proposed method	36.564

the current ripple is large in FCS-MPC method when the sampling frequency is not high enough. Under the same sampling frequency, the proposed method has an improved current waveform in steady state with reduced ripples, as shown in Fig. 8b, because the current trajectory is changed more frequently, in comparison with FCS-MPC method. As shown in a detailed view of source current from the zoomed-in area of Fig. 8b, the proposed control method can eliminate current error at the sampling instant.

As shown in Fig. 8 for both FCS-MPC method and proposed method, three dc-link voltages are balanced and all controlled to the reference value 70 V. Since H-bridge has a single-phase input, dc-link voltage has ripple components at twice source side frequency (100 Hz). This ripple can be filtered to an acceptable level by using large capacitance. Comparing the waveforms of total ac-side voltage v_{HT} in Figs. 8a and b, the proposed method provides a clearer staircase waveform against FCS-MPC method. However, some narrow voltage pulses, whose width are dead time, unavoidably exist during the commutation process.

More evaluations of steady-state performance are shown in Table 4, where the average steady-state error (SSE) and total harmonic distortion (THD) of source current for FCS-MPC method

and proposed method are given. The definition of average SSE of signal x is given as [25]

$$\Delta|x| = \frac{1}{M} \sum_{l=1}^M |x^*(l) - x(l)| \quad (13)$$

where M is 10,000 per fundamental period, which is much larger than the total number of sampling instants per fundamental period. It can be noted in Table 4 that the proposed method has the lower average SSE and THD of i_s than FCS-MPC method.

5.3 Dynamic performance

Fig. 9 shows the dynamic responses of FCS-MPC method and proposed method, where a step change of dc-link reference voltage v_c^* from 60 to 80 V is evaluated. It can be seen in Fig. 8 that like FCS-MPC method, an extreme change of ac-side voltage v_{HT} can be generated for a fast source current tracking in the proposed method and all dc-link voltages reach new reference value without any overshoot or undershoot, while they remain balanced. A faster

Fig. 8 Steady-state experimental waveforms and measured spectrum
(a) FCS-MPC method, (b) Proposed method

Table 4 Average SSE and THD of i_s

Control method	$\Delta i_s $, A	THD of i_s , %
FCS-MPC	0.81	12.07
proposed method	0.34	3.96

dc-link voltage regulation can be achieved by tuning PI controller, but its overshoot may be seen.

A further comparison of dynamic response under the condition of unbalanced loads for FCS-MPC method and proposed method is shown in Fig. 10, where one dc load R_1 is changed from nominal value 20 to 13 Ω , while R_2 and R_3 are unchanged. Here, the load current of the first H-bridge cell instantaneously increases $\sim 50\%$. It can be seen in Fig. 10 that v_{C1} is regulated to reference value faster in the proposed method than FCS-MPC method by using the voltage balancing modulation strategy described in Section 4.4, while the other two dc-link voltages v_{C2} and v_{C3} are nearly unaffected by this change. Even under the condition of unbalanced loads, a good current tracking is still obtained in the proposed method, as shown in Fig. 10b.

6 Conclusion

In this paper, a DBC method with voltage balancing modulation has been introduced for a single-phase CHB rectifier. The proposed method has been evaluated in experimental test and its advantages

over FCS-MPC method are summarised in Table 5. In comparison with FCS-MPC method, as shown in Table 5, the proposed method has several merit factors in terms of a significant reduction in computational burden, an enhanced steady-state current performance, a comparable dynamic response, and elimination of weighting factor that avoids the time-consuming tuning work. The proposed control method can be easily extended to any single-phase CHB rectifier with more cells.

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Fig. 9 Dynamic response with a step change of v_C^* from 60 into 80 V
(a) FCS-MPC method, (b) Proposed method

Fig. 10 Dynamic response with a step change of R_1 from 20 into 13 Ω , while R_2 and R_3 remain unchanged
(a) FCS-MPC method, (b) Proposed method

Table 5 Evaluation of proposed method and FCS-MPC method

Control method	Computational burden	Steady-state performance	Dynamic response	Use of λ_v
FCS-MPC	high	low	fast	required
proposed method	low	high	fast	not required

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