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Multiple-Vector Model Predictive Power Control of Three-Phase Four-Switch Rectifiers with Capacitor Voltage Balancing

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Abstract—Model predictive power control (MPPC) takes the switching non-linearity of power converters and system constraints into consideration. It is a promising control technique for three-phase four-switch rectifiers (TPFSRs) because capacitor voltage balancing control and instantaneous power control can be simultaneously designed for this type of power converters. However, since only one switching vector is allowed in each control interval, conventional MPPC (C-MPPC) may lead to significant output power ripples that can severely degrade system power quality. This is particularly true for TPFSRs due to the limited number of switching states as well as the constraint imposed by the capacitor voltage balancing control. To improve the performance of TPFSRs, this paper proposes a multiple-vector model predictive power control (MV-MPPC) scheme, which can minimize active power and reactive power ripples and achieve capacitor voltage balancing with a constant switching frequency. An equivalent zero voltage vector model and a capacitor voltage balancing model are derived to implement the proposed control scheme. Comparative experimental results are presented to demonstrate the superiority of the proposed control scheme over the C-MPPC.

Index Terms—Model predictive control, equivalent zero voltage vector, three-phase four-switch rectifier, capacitor voltage balancing, power ripples reduction.

I. INTRODUCTION

Three-phase six-switch rectifiers (TPSSR) are widely used in grid-connected energy storage systems due to their advantages such as bidirectional power flow, controllable power factor, sinusoidal line current and good dc voltage regulation ability [1]. Nevertheless, this type of power converters is sensitive to the switch faults caused by overstressed operation under harsh environments. The failure of power switches is critical as it may decrease the system performance or even lead to more severe cascading failures. Once a fault occurs, the system operation has to be halted. However, in some hazardous environments or mission-critical applications, it is desirable that power converters can continuously operate with degraded performance in the case of switch failures.

Over the past few years, the demand for fault tolerant rectifiers is growing increasingly, which has promoted the

development of fault detection methods and fault tolerant topologies for power switch failures. Fault detection, as the prerequisite of fault tolerant operation, has been extensively investigated for open-circuit switch failures, where single or multiple faults in a rectifier can be located [2]–[6]. With the knowledge of fault location, corresponding fault tolerant schemes can be applied to maintain the continuous operation.

Reference [6] introduced an additional parallel leg for open-circuit fault tolerant operation. However, this solution may increase the system cost due to the additional redundant switching leg. Sharing one leg with the inverter was adopted for fault tolerant operation in [7]–[10], but this solution is only applicable to multi-converter topologies. A pulse width modulation-based fault tolerant scheme was presented in [11] by utilizing the anti-parallel diode for open-circuit fault management. However, the current was distorted and the overall performance in post-fault conditions was not satisfactory. By connecting the faulty phase to the dc-link midpoint, a three-phase four-switch rectifier (TPFSR) was presented in [12]–[18], which requires minimum additional components for fault tolerant operation. Nevertheless, since there are only four switching states available in the TPFSR, the rectifier system may suffer from unbalance three-phase input currents, high total harmonic distortion (THD) and significant power ripples. Such operations may degrade system power quality or even cause cascading or catastrophic failures in the system. Therefore, accurate modeling and proper control schemes for TPFSRs should be developed to meet the technical specifications, such as low THD and low active/reactive power ripples.

Substantial research efforts have been focused on the comprehensive design and performance improvement of TPFSRs, such as detailed modeling, optimized modulation, and analytic comparison. A double Fourier integral analysis-based model of TPFSRs was constructed for accurate modeling in [19]. However, the model was not applicable in industrial applications because of its complexity. d - q rotating coordinate-based analysis was developed for TPFSRs, but the system stability was challenged by the capacitor voltage oscillations and deviations. The effects of two space vector modulation (SVM) approaches on capacitor current optimization were investigated by Zeng et al. in [13]. A high-frequency model for current ripple analysis was proposed in [15], where the ac current ripples of three SVM-based approaches were investigated. A hybrid PWM strategy based on the evaluation of root-mean-square values was developed to reduce the dc-link capacitor stress [14] and zero voltage vector distribution based on common mode volt-

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age and capacitor current stress optimization was developed in [20]. However, unlike TPSSRs where the dc-link voltage is constant, the basic voltage vectors of TPFSRs may vary in amplitude and phase with the oscillations of capacitor voltages and a large amount of complex trigonometric functions have to be involved for SVM-based approaches.

Another approach for implementing high-performance TPFSRs is to use model predictive power control (MPPC) [21], in which the discrete nature and constraints of power converters are taken into account to predict future behaviors of the system [22], [23]. The MPPC of TPFSRs under unbalanced grid voltages was investigated in [24] to improve the rectifier reliability under nonideal conditions. In MPPC, the system behaviors are predicted only for the possible voltage vectors, and the one with the minimum cost function value is selected and applied. No phase-locked loop (PLL) is required in MPPC schemes, and the elimination of PLL ensures the grid synchronization of TPFSRs at all times even during the transition from normal operation to post-fault operation. The capacitor voltage offset deviation in TPFSRs is always suppressed by adding an additional component to the cost function [25]. However, since only one switching vector is allowed in each control interval, conventional MPPC (C-MPPC) may lead to significant output power ripples that can severely degrade system power quality. This is particularly true for TPFSRs due to the limited number of switching states as well as the constraint imposed by the capacitor voltage balancing control in the cost function.

In this paper, a multiple-vector model predictive control (MV-MPPC) scheme for TPFSRs is proposed for minimization of active power and reactive power ripples. A novel equivalent zero vector model is implemented to carry out the proposed scheme. To cope with the capacitor voltage balancing, the capacitor voltage is comprehensively modeled and an appropriate control strategy is developed to balance the capacitor voltage. A comparative study of the proposed MV-MPPC with C-MPPC is carried out. Simulation and experimental results confirm that smaller ripples and higher quality of control variables can be obtained with the proposed scheme. The major contributions of this paper include:

- The drawback of C-MPPC utilized in TPFSRs is deeply analyzed. To cope with the limited number of switching vectors in this topology, a simple way to compose an equivalent zero voltage vector is proposed.
- A comprehensive model of the capacitor voltage is proposed. With the proposed model, a novel MV-MPPC with capacitor voltage balancing and power ripples minimization with a constant switching frequency is proposed and experimentally verified.
- The proposed scheme is based on the $\alpha\beta$ frame which is identical to that of the healthy state operation. No phase-locked loop (PLL) is required and the TPFSRs is always in synchronization with the grid.
- The performance of C-MPPC and MV-MPPC is evaluated with both simulation and experimental results.

This paper is structured as follows. The model of FSTPRs is illustrated in Section II. Section III revisits the C-MPPC of TPFSRs. Section IV presents the proposed MV-MPPC of

Fig. 1: Topology of the three-phase four-switch rectifier.

TPFSRs. Simulation and experimental results are presented in Section V. And finally, conclusions are drawn in Section VI.

II. MODEL OF TPFSR

Assuming the switch fault occurs in leg 'c', the corresponding phase is connected to the dc-link midpoint for post-fault operation. The other two phases are connected to the switching legs. The circuit of a TPFSR can be illustrated in Fig.1. The grid supply and the output from the three-phase grid-connected TPFSR are considered as ideal voltage sources. v_{sa} , v_{sb} , and v_{sc} denote the grid voltages, and i_a , i_b , and i_c represent the input currents. L_s and R_s are the filter inductance and equivalent resistance, respectively. v_{c1} , v_{c2} , and v_{DC} are the upper capacitor, lower capacitor and dc-link voltages, respectively. C_1 and C_2 are the output capacitors, whose values are assumed to be identical $C_1 = C_2$.

A. Model of Voltage Vectors and Zero Vector

Variables S_a and S_b are defined as the states of the switches, i.e. $S_a = 1$ indicates the close state of S_1 and open state of S_3 , and $S_a = 0$ describes the complementary operation of the switches. With all the possible combinations of S_a and S_b , four voltage vectors are available in TPFSRs. The converter voltages can be expressed by

$$\begin{aligned} u_{ao} &= S_a v_{c1} + (S_a - 1) v_{c2} \\ u_{bo} &= S_b v_{c1} + (S_b - 1) v_{c2} \\ u_{co} &= 0 \end{aligned} \quad (1)$$

It is clear that $u_{xo} = u_{xn} + u_{no}$, ($x = a, b, c$) and the grid voltage is balanced with $u_{an} + u_{bn} + u_{cn} = 0$. Then the phase-to-neutral voltages are

$$\begin{aligned} u_{an} &= (\frac{2}{3} S_a - \frac{1}{3} S_b) v_{c1} + (-\frac{1}{3} + \frac{2}{3} S_a - \frac{1}{3} S_b) v_{c2} \\ u_{bn} &= (-\frac{1}{3} S_a + \frac{2}{3} S_b) v_{c1} + (-\frac{1}{3} - \frac{1}{3} S_a + \frac{2}{3} S_b) v_{c2} \\ u_{cn} &= (-\frac{1}{3} S_b - \frac{1}{3} S_a) v_{c1} + (\frac{2}{3} - \frac{1}{3} S_a - \frac{1}{3} S_b) v_{c2} \end{aligned} \quad (2)$$

The values of the four active voltage vectors (V_1 , V_2 , V_3 , and V_4) are listed in Table. I.

As shown in Table. I, there is no zero voltage vector in TPFSRs. Moreover, four basic active voltage vectors vary in amplitude and phase with the oscillations of capacitor voltages. In order to give an intuitive display of the four voltage vectors, the voltage vectors under identical capacitor voltages $v_{c1} = v_{c2} = 150V$ and deviated capacitor voltages $v_{c1} = 200V, v_{c2} = 100V$ are depicted in Fig.2.

TABLE I: Switching Function and The Four Basic Voltage Vectors in The α - β Plane of TPFSR

S_a	S_b	Vector	u_α	u_β
0	0	V_1	$-v_{c2}/3$	$-v_{c2}/\sqrt{3}$
1	0	V_2	$2v_{c1}/3 + v_{c2}/3$	$-v_{c2}/\sqrt{3}$
1	1	V_3	$v_{c1}/3$	$v_{c1}/\sqrt{3}$
0	1	V_4	$-v_{c1}/3 - 2v_{c2}/3$	$v_{c1}/\sqrt{3}$

Fig. 2: Vectors in the $\alpha\beta$ plane of the FSTPR.

Due to the absence of zero voltage, the equivalent zero vector V_{ez} is modeled. The zero vector can be obtained in many ways, e.g., a combination of two, three or even four vectors. As shown in Fig.2 (b), vector V_1 is always in parallel with vector V_3 regardless of the capacitor voltage. Among all the combinations, the simplest way to compose the zero vector is to properly adjust the active time of V_1 and V_3 . According to the volt-second equivalent law, the zero voltage vector can be obtained by applying V_1 with a time interval of t_{v1} while applying V_3 with a time interval of $\frac{v_{c2}}{v_{c1}}t_{v1}$. The applied time of the equivalent zero voltage is

$$t_{v0} = (1 + \frac{v_{c2}}{v_{c1}})t_{v1}. \quad (3)$$

B. Model of Capacitor Voltages

According to the Kirchhoff's current law, the dynamic equations for capacitor voltage are derived as

$$C \frac{dv_{c1}}{dt} = i_{c1} = S_a i_a + S_b i_b - \frac{v_{DC}}{R_{DC}}, \quad (4)$$

$$C \frac{dv_{c2}}{dt} = i_{c2} = -(1 - S_a) i_a - (1 - S_b) i_b - \frac{v_{DC}}{R_{DC}}. \quad (5)$$

where i_{c1} and i_{c2} are the upper and lower capacitor currents, respectively. v_{DC} is the dc-link voltage and R_{DC} is the equivalent load resistant.

Applying the Kirchhoff's current law, the following equation can be derived

$$i_c = i_{c2} - i_{c1}. \quad (6)$$

Substituting (4) and (5) into (6), the dynamic equation for capacitor voltage is

$$C \frac{d(v_{c2} - v_{c1})}{dt} = -(i_a + i_b) = i_c. \quad (7)$$

After the transient state, a DC component $\bar{i}_c$ may be introduced to i_c . Then, the analytical solution of (7) is deduced as:

$$v_{c2}(t) - v_{c1}(t) = \frac{1}{C} \int (i_c + \bar{i}_c) dt + v_{c2}(0) - v_{c1}(0). \quad (8)$$

As shown in (8), if the current of the faulty phase is not strictly symmetrical, the small dc component of i_c will give rise to the deviation of capacitor voltages. When $\bar{i}_c$ is positive, the voltage of the lower capacitor deviates to a higher value, while that of the upper one deviates to a lower value and vice versa.

C. Model of Rectifier

The relationship between grid voltages and line current can be expressed in the α - β reference coordinate as

$$\frac{d\vec{i}_s}{dt} = -\frac{R_s}{L_s} \vec{i}_s + \frac{1}{L_s} \vec{v}_s - \frac{1}{L_s} \vec{u}_s \quad (9)$$

where $\vec{i}_s = i_\alpha + j \cdot i_\beta$ is the input current vector, $\vec{v}_s = v_\alpha + j \cdot v_\beta$ is the grid voltage vector, $\vec{u}_s = u_\alpha + j \cdot u_\beta$ is the voltage vector generated by the TPFSR.

For a three-phase grid-connected TPFSR, the instantaneous active and reactive power can be represented in the α - β reference coordinate as

$$P = 1.5(v_\alpha i_\alpha + v_\beta i_\beta), \quad (10a)$$

$$Q = 1.5(v_\beta i_\alpha - v_\alpha i_\beta). \quad (10b)$$

The time derivatives of active and reactive power can be obtained by differentiating (10a) and (10b)

$$\frac{dP}{dt} = 1.5 \left(\frac{dv_\alpha}{dt} i_\alpha + v_\alpha \frac{di_\alpha}{dt} + \frac{dv_\beta}{dt} i_\beta + v_\beta \frac{di_\beta}{dt} \right), \quad (11a)$$

$$\frac{dQ}{dt} = 1.5 \left(\frac{dv_\beta}{dt} i_\alpha + v_\beta \frac{di_\alpha}{dt} - \frac{dv_\alpha}{dt} i_\beta - v_\alpha \frac{di_\beta}{dt} \right). \quad (11b)$$

The ideal grid voltage components can be written as

$$v_\alpha = U_g \sin(\omega t), \quad (12a)$$

$$v_\beta = -U_g \cos(\omega t) \quad (12b)$$

where U_g is the amplitude of the grid voltage and ω is the grid frequency.

Thus, the time derivatives of the grid voltage can be presented as

$$\frac{dv_\alpha}{dt} = \omega U_g \cos(\omega t) = -\omega v_\beta, \quad (13a)$$

$$\frac{dv_\beta}{dt} = \omega U_g \sin(\omega t) = \omega v_\alpha. \quad (13b)$$

Based on (9), the time derivatives of line current can be obtained as

$$\frac{d\vec{i}_\alpha}{dt} = -\frac{R_s}{L_s} \vec{i}_\alpha + \frac{1}{L_s} \vec{v}_\alpha - \frac{1}{L_s} \vec{u}_\alpha, \quad (14a)$$

$$\frac{d\vec{i}_\beta}{dt} = -\frac{R_s}{L_s} \vec{i}_\beta + \frac{1}{L_s} \vec{v}_\beta - \frac{1}{L_s} \vec{u}_\beta. \quad (14b)$$

Substituting (13a), (13b), (14a), and (14b) into (11a) and (11b), respectively. The time derivative of active and reactive power can thus be obtained as

$$\frac{dP}{dt} = \frac{3}{2L_s} [(v_\alpha^2 + v_\beta^2) - (v_\alpha u_\alpha + v_\beta u_\beta)] - \frac{R_s}{L_s} P - \omega Q, \quad (15a)$$

$$\frac{dQ}{dt} = \frac{3}{2L_s} [(v_\alpha u_\beta - v_\beta u_\alpha)] - \frac{R_s}{L_s} Q + \omega P. \quad (15b)$$

From (15a) and (15b), the prediction for active and reactive power at the next sampling period can be obtained as

$$P(k+1) = P(k) + \frac{3}{2L} \left[(v_\alpha^2(k) + v_\beta^2(k)) - (v_\alpha(k)u_\alpha(k) + v_\beta(k)u_\beta(k)) - \frac{R_s}{L_s}P(k) - \omega Q(k) \right] T_s, \quad (16a)$$

$$Q(k+1) = Q(k) + \frac{3}{2L} [(v_\alpha(k)u_\alpha(k) - v_\beta(k)u_\beta(k)) - \frac{R_s}{L_s}Q(k) + \omega P(k)] T_s, \quad (16b)$$

where T_s is the sampling period.

III. CONVENTIONAL MODEL PREDICTIVE POWER CONTROL WITH CAPACITOR VOLTAGE BALANCING

Generally, the cost function for power control can be defined such that both active and reactive power at the end of one sampling period is as close as possible to their reference values, which can be expressed as

$$J_r = ((P^* - P(k+1))^2 + (Q^* - Q(k+1))^2) / P_N^2 \quad (17)$$

where P^* and Q^* are the future references of active power and reactive power, respectively. P_N is the nominal output power.

Since the capacitor voltage deviation is proportional to the dc component of i_c as shown in Section II-B, the capacitor voltage deviation can be suppressed by adding a cost function component. Therefore, the cost function of C-MPPC can be written as

$$J = ((P^* - P(k+1))^2 + (Q^* - Q(k+1))^2) / P_N^2 + \lambda (i_c^* - i_c(k+1))^2 / I_N^2, \quad (18)$$

where $i_c^* = k_p(v_{c2} - v_{c1})$ is the current future reference of the faulty phase. $k_p = 1$ is a positive scalar coefficient and I_N is the nominal phase current. λ is the weighting factor which denotes the importance of capacitor voltage deviation suppression versus active and reactive power control.

Since the capacitor voltage fluctuates with the fundamental frequency of the grid, the capacitor voltage suppression component in the cost function is not negligible, especially when the load is high or a fast capacitor voltage convergence is required. In these cases, the capacitor voltage suppression component is dominant in the cost function, and the voltage vector that leads to the convergence of capacitor voltage will be selected rather than the one that makes active and reactive power track their references. As only four voltage vectors are available in FSTPRs, the voltage vector selected for suppression of capacitor voltage deviation could probably be the worst one for active and reactive power tracking control, which will definitely give rise to significant ripples in active and reactive power.

IV. MULTIPLE-VECTOR MODEL PREDICTIVE POWER CONTROL WITH CAPACITOR VOLTAGE BALANCING

In order to solve this problem, MV-MPPC with capacitor voltage balancing is proposed. The implementation of the proposed scheme is composed of the following parts, i.e., voltage vectors selection, calculation of the duration for each active vector, control of the capacitor voltage deviation and

Fig. 3: Control diagram of the proposed MV-MPPC.

Fig. 4: Active and reactive power slopes as a function of the time for each voltage vector and equivalent zero vector.

duty cycle calculation for each leg. The whole control diagram is depicted in Fig.3. The detailed introduction of each part is elaborated in the following section.

A. Voltage Vector Selection

Two active voltage vectors are selected based on (17). One active voltage vector is the one with the lowest value of cost function. To simplify the calculation, the other active voltage vector is selected from the adjacent vector with a lower value of cost function.

B. Minimization Criteria

After determining the two active voltage vectors, the duration of each voltage vector should be calculated.

Let (15a) and (15b) be written as

$$\sigma_{pi} = \left. \frac{dP_i}{dt} \right|_{V=V_i} \quad (19a)$$

$$\sigma_{qi} = \left. \frac{dQ_i}{dt} \right|_{V=V_i} \quad (19b)$$

where $i \in \{1, 2, 3, 4\}$. For clear illustrations, with the converter parameters given in Table II and the rectifier operates at unity power factor, Fig.4 depicts the instantaneous active and reactive power slopes as a function of time for each voltage vector and equivalent zero vector V_{ez} .

Fig. 5: Control diagram of the capacitor voltage balancing.

For the chosen example, v_{o1} and v_{o2} are adopted during the duration calculation process. The active and reactive power at the end of the control period can be expressed as

$$P(k+1) = P(k) + \sigma_{p1}t_1 + \sigma_{p2}t_2 + \sigma_{p0}t_0, \quad (20a)$$

$$Q(k+1) = Q(k) + \sigma_{q1}t_1 + \sigma_{q2}t_2 + \sigma_{q0}t_0, \quad (20b)$$

$$t_0 = T_s - t_1 - t_2. \quad (20c)$$

where t_1 is the duration of voltage vector v_{o1} , t_2 is the duration of voltage vector v_{o2} and t_0 is the duration of the equivalent zero vector.

The active and reactive power error can be defined as

$$\Delta P = P^* - P(k) + \sigma_{p1}t_1 + \sigma_{p2}t_2 + \sigma_{p0}t_0, \quad (21a)$$

$$\Delta Q = Q^* - Q(k) + \sigma_{q1}t_1 + \sigma_{q2}t_2 + \sigma_{q0}t_0. \quad (21b)$$

The goal of the control algorithm is to determine the dwell time t_1 and t_2 in order to minimize the active and reactive power ripples. The optimal dwell time of voltage vector t_1 and t_2 can be obtained by minimizing the sum of squared power errors [26], [27]

$$F(t_1, t_2) = \Delta P^2 + \Delta Q^2. \quad (22)$$

The optimal dwell times should satisfy the minimum value conditions

$$\begin{cases} \frac{\partial F(t_1, t_2)}{\partial t_1} = 0 \\ \frac{\partial F(t_1, t_2)}{\partial t_2} = 0. \end{cases} \quad (23)$$

The solution of (23) is given by

$$\begin{cases} t_1 = \frac{t_{num1}}{t_{den}} \\ t_2 = \frac{t_{num2}}{t_{den}}. \end{cases} \quad (24)$$

where t_{num1} , t_{num2} and t_{den} are denoted in (25a) (25b) (25c), respectively. The values of t_1 and t_2 are saturated to zero if they are negative, or T_s if t_1 and t_2 are larger than T_s due to the physical limitation.

C. Capacitor Voltage Balancing Control

As analyzed in (8), the capacitor voltage deviation can be suppressed by injecting a dc component to i_c . According to (2), when employing switching states (00) and (11), the phase 'c' to neutral voltage can be expressed as

$$v_{cn} = \begin{cases} \frac{2}{3}v_{c2}, & S_a S_b = (00) \\ -\frac{2}{3}v_{c1}, & S_a S_b = (11) \end{cases} \quad (26)$$

A positive dc component of i_c can be injected by increasing the duration time of the state (00) or reducing the duration time of the state (11) and a negative dc component of i_c can be injected by increasing the duration time of the state (11)

or reducing the duration time of the state (00). Therefore, the capacitor voltage offset can be canceled by properly adjusting the durations of state (00) and (11). The block diagram of the control strategy is shown in Fig.5. The voltage difference of the capacitor is measured in real time, and the deviation is extracted by a low-pass filter (LPF). k is a positive scalar that determines the convergence time of the capacitor voltage and $\frac{T_s}{v_{DC}}$ is the normalized factor. The adjustment of the state duration $\Delta d_a = \Delta d_b = \Delta d$ is positive when the duration time of state (11) is supposed to reduce and the adjustment is negative when the duration of state (11) is supposed to increase. In the steady state when the capacitor voltage deviation is canceled, Δd will be very close to zero and their effect on the control performance can be neglected.

D. Duty Cycle Calculation

The duration time of zero vector t_0 can be obtained by (20c). (24) is synthesized by applying the state (11) and state (00). According to (3), t_0 can be equivalently achieved by applying state (11) with t_{v1} and state (00) with $t_0 - t_{v1}$. Therefore, the zero vector duration time can be achieved by applying state (11) with a duration time of

$$t_{v3} = \frac{v_{c2}}{v_{DC}} t_0. \quad (27)$$

and the rest time by applying state (00);

The duty cycles applied to leg 'a' and leg 'b' can be denoted as t_a and t_b , respectively. The auxiliary variables h_1 and h_2 are defined for t_a and t_b calculations

$$h_1 = \begin{cases} 1, & \text{if } V_1 \text{ is selected} \\ 0, & \text{if } V_3 \text{ is selected} \end{cases} \quad (28)$$

$$h_2 = \begin{cases} 1, & \text{if } V_2 \text{ is selected} \\ 0, & \text{if } V_4 \text{ is selected} \end{cases} \quad (29)$$

Therefore, the duty cycles of leg 'a' and leg 'b' can be determined as follows

$$t_a = \underbrace{(1 - h_1)t_1 + h_2t_2}_{t_{av}} + \underbrace{\frac{v_{c2}}{v_{DC}}t_0}_{t_{zv}} + \underbrace{\Delta d}_{t_{cv}} \quad (30a)$$

$$t_b = \underbrace{(1 - h_1)t_1 + (1 - h_2)t_2}_{t_{av}} + \underbrace{\frac{v_{c2}}{v_{DC}}t_0}_{t_{zv}} + \underbrace{\Delta d}_{t_{cv}} \quad (30b)$$

where the first term t_{av} is the duration time of active vectors, the second term t_{zv} is the duration time of zero vector and the last term t_{cv} is the duration time for capacitor voltage deviation cancellation. The values of t_a and t_b are saturated to zero if they are negative, or T_s if t_a and t_b are larger than T_s due to the physical limitation.

V. PERFORMANCE EVALUATIONS

In this section, the effectiveness of the proposed MV-MPPC and its performance comparison with C-MPPC are evaluated with both simulation and experimental results. The system configuration and parameters are listed in TABLE II.

$$t_{num1} = (\sigma_{q2} - \sigma_{q0})(P^* - P(k)) + (\sigma_{p0} - \sigma_{p2})(Q^* - Q(k)) + (\sigma_{q0}\sigma_{p2} - \sigma_{q2}\sigma_{p0})T_s \quad (25a)$$

$$t_{num2} = (\sigma_{q0} - \sigma_{q1})(P^* - P(k)) + (\sigma_{p1} - \sigma_{p0})(Q^* - Q(k)) + (-\sigma_{q0}\sigma_{p1} + \sigma_{q1}\sigma_{p0})T_s \quad (25b)$$

$$t_{den} = \sigma_{q0}\sigma_{p2} - \sigma_{q1}\sigma_{p2} - \sigma_{q2}\sigma_{p0} + \sigma_{q1}\sigma_{p0} - \sigma_{q0}\sigma_{p1} + \sigma_{q2}\sigma_{p1}. \quad (25c)$$

Fig. 6: [Simulation data] Steady state performance evaluation. For each figure-set, from top to bottom are, active and reactive power, grid currents, capacitor voltage.

Fig. 7: [Simulation data] Harmonic spectrum of phase 'a' current. For each figure-set, from top to bottom are, phase 'a' grid current and its spectrum.

A. Simulation Evaluations

The steady state control performance comparison between C-MPPC and MV-MPPC was carried out through MATLAB/Simulink as a preliminary concept of proof. The simulation results are shown in Fig.6, where the same outer control loop and test conditions were configured for a fair comparison. The active power reference was set to 600W and the reactive power reference was set to 0var. It is clearly seen

that in both methods, the active power and reactive power can track the reference very well and the capacitor voltage can be controlled balanced. However, the proposed MV-MPPC presents fewer power ripples and lower current harmonics. As shown in Fig.7, the grid current quality is drastically improved using the proposed MV-MPPC. Its THD is only 1.88% while the THD with C-MPPC is 5.79% as multiple switching vectors can be selected during one control period.

(a) MV-MPPC with capacitor voltage balancing control

(b) MV-MPPC without capacitor voltage balancing control

Fig. 8: [Simulation data] For each figure-set, from up to down are, dc-link voltage, active and reactive power, grid currents, capacitor voltage, respectively.

Fig. 9: Experimental test rig.

TABLE II: System Parameters Used in Simulations and Experiments

Parameter	Value	Parameter	Value
Filter inductance	10 mH	Source voltage (RMS)	50 V
Equivalent resistance	0.5 Ω	Source frequency	50 Hz
Capacitor C_1, C_2	1410 μF	Sampling frequency	20 kHz
Dead Time	1 μs		

To examine the effectiveness of capacitor voltage balancing of the proposed MV-MPPC, simulations were done with and without capacitor voltage control, and the results are shown in Fig.8. When MV-MPPC is applied without capacitor voltage control, an obvious dc offset between the two capacitor

voltages is observed and the ripples of dc-link voltages are higher than those of the controlled cases.

B. Experimental Verification of the Proposed Scheme

1) *Experimental Setup:* A 32-bit floating digital signal processor (DSP) TMS320F28335 and a Xilinx FPGA XC3S400 as the assistant controller for implementing PWM signals output, digital-to-analog conversion output, analog-to-digital conversion control, and fault protection, etc, were developed to execute the two model predictive methods. In the following tests, all variables are displayed on a digital oscilloscope via 12-bit digital-to-analog converters, except for the current and voltage variables, which are directly measured by current and voltage probes. The converter was implemented by discrete IGBTs (Infineon IKW40N65H5). The duty cycles obtained in (30a)(30b) are applied by an up-and-down counter and a comparator. Therefore, the proposed MV-MPPC operates at a constant switching frequency of 20kHz.

The experimental test rig is presented in Fig. 9. In the digital implementation of MPPC, it is well-known that there is a one-step delay between the commanding voltage vector and the applied voltage vector [28]. In this paper, the compensation method proposed in [28] is adopted to compensate the one-step delay in both methods. The system and control parameters are listed in Table II. One of the important considerations for implementing MPPC is the calculation burden. It costs 16.56 μs to implement the C-MPPC while 18.66 μs for the MV-MPPC. According to the test results, only a small additional

Fig. 10: [Experimental results] Steady state control performance. For each figure-set, from top to down bottom, active power, reactive power, grid currents and capacitor voltages.

Fig. 11: [Experimental data] Harmonic spectrum of grid current. For each figure-set, from top to bottom are, phase 'a' current and its spectrum.

Fig. 12: [Experimental results] Step change of the active power. For each figure-set, from top to down bottom, active power, reactive power, grid currents and capacitor voltages.

computation burden (12.7%), in comparison with C-MPPC, is required to implement the proposed MV-MPPC.

2) *Steady state power ripples and current quality comparison:* In order to further validate the advantage of the

Fig. 13: [Experimental results] Step change of the reactive power. For each figure-set, from top to down bottom, active power, reactive power, grid currents and capacitor voltages.

Fig. 14: [Experimental results] Responses to external load disturbance. For each figure-set, from top to bottom are, active power, reactive power, grid currents and capacitor voltages.

Fig. 15: [Experimental results] For each figure-set, from top to bottom are, dc-link voltage, two capacitor voltages, active power, reactive power, grid currents.

proposed MV-MPPC, experimental results of both schemes are presented. The steady state responses at 400 W active power and 0 Var reactive power are presented in Fig. 10. As shown in the figure, both schemes can track the power references and

the capacitor voltage can be controlled balanced. However, the proposed MV-MPPC presents much better performance than that of the C-MPPC in terms of lower power ripples and less current harmonics. The harmonics spectrum is further pre-

TABLE III: Test Results of Various Active Power

$Q = 0 \text{ var}$	Method	P_{ripple} (W)	Q_{ripple} (var)	THD of i_a (%)
$P = 400 \text{ W}$	MV-MPPC	30.2	27.0	4.2
	C-MPPC	113.4	86.7	10.96
$P = 600 \text{ W}$	MV-MPPC	37.8	31.2	3.40
	C-MPPC	127.3	107.3	9.61
$P = 800 \text{ W}$	MV-MPPC	43.1	35.9	3.72
	C-MPPC	139.7	116.8	7.16

sented in Fig. 11. The data were acquired from an oscilloscope at 100 kHz sampling rate and analyzed in MATLAB. With the same sampling frequency, the grid current THD of C-MPPC is 7.64%, which is much higher than 2.69% of the proposed MV-MPPC, proving the dramatic performance improvement in grid current quality. The quantitative comparison of both methods with various operating points is summarized in Table III. Generally, the proposed MV-MPPC presents less active and reactive power ripples than that of the C-MPPC and the grid current THD of the proposed MV-MPPC is much lower than that of the C-MPPC.

3) *Transient state comparison:* The response to the step change of active power is presented in Fig. 12. The active power reference steps from 400 W to 600 W at $t = 0.03 \text{ s}$ and then steps down to 400 W at $t = 0.07 \text{ s}$. The response to the step change of reactive power is presented in Fig. 13. The reactive power reference steps from 0 var to 400 var at $t = 0.03 \text{ s}$ and then steps down to 0 var at $t = 0.07 \text{ s}$. It is clearly seen that in both cases, the active power and reactive power track the references very well with similar dynamics, but the proposed MV-MPPC presents lower power ripples and current harmonics. In both cases, the active and reactive power can be controlled separately. However, apart from the active and reactive power control, the capacitor voltage balancing control is applied in the TPFSR. The step change of power, especially the step change of reactive power, will cause the step change of the phase c current, which drives the capacitor voltage to unbalance. Although the active and reactive power control is decoupled, the capacitor voltage control will introduce small ripples to the active and reactive power control during the transient as evidenced from Fig. 12 and Fig. 13.

The responses to external load disturbances under the condition of closed-loop dc-link voltage control are presented in Fig. 14, where the load was initially set to 240Ω , and suddenly stepped to 120Ω , then stepped back to 240Ω . It is clear that during the transient process, the reactive power remains at zero and the active power under both cases show a similar response, which proves that the good dynamic performance of the system is not affected by the proposed MV-MPPC.

4) *Capacitor voltage balancing scheme validation:* The MV-MPPC with and without control of capacitor voltage is shown in Fig. 15. Without the capacitor voltage control scheme, the control performance of the TPFSRs deteriorates. The voltage error between the two capacitors is 80 V , and significant active and reactive power ripples are present and the grid currents are not balanced, indicating the necessity of capacitor voltage control. With the capacitor voltage control, this error is eliminated and the steady control performance

of active and reactive power is greatly improved, proving the effectiveness of the capacitor voltage balancing control scheme.

VI. CONCLUSION

This paper has proposed a MV-MPPC scheme to improve the steady state performance of TPFSRs. To cope with the limited number of switching vectors in TPFSRs, a novel equivalent zero vector model is proposed. A comprehensive model and control scheme of the capacitor voltage has been proposed to balance the capacitor voltage. The duration time of each leg is obtained by active and reactive power ripples minimization and capacitor voltage balancing control. Simulation and experimental results confirm the performance of the proposed MV-MPPC is better than that of the C-MPPC with a constant switching frequency. Considering the negligible computation increase in the digital implementation, it is concluded that the proposed MV-MPPC is more favorable and practical to achieve satisfactory performance of TPFSRs.

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