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Gold-free contacts on $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ high electron mobility transistor structure grown on a 200-mm diameter Si(111) substrate

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The authors report on the fabrication and characterization of low-temperature processed gold-free Ohmic contacts for $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ high electron mobility transistors (HEMTs). The HEMT structure grown on a 200-mm diameter Si(111) substrate is used in this study. Using the Ti/Al/NiV metal stack scheme, the source/drain Ohmic contact optimization is accomplished through the variation of Ti/Al thickness ratio and thermal annealing conditions. For an optimized Ti/Al stack thickness (20/200 nm) annealed at 500 °C for 30 s with smooth contact surface morphology, a specific contact resistivity of $\sim 6.3 \times 10^{-6} \Omega \text{cm}^2$ is achieved. Furthermore, with gold-free Ni/Al gates, the fabricated HEMTs exhibit $I_{\text{ON}}/I_{\text{OFF}}$ ratio of $\sim 10^9$ and a subthreshold swing of $\sim 71 \text{ mV/dec}$. The demonstrated gold-free contact schemes thus provide a solution toward the implementation of GaN-based HEMT process on a Si foundry platform. © 2016 American Vacuum Society.

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I. INTRODUCTION

GaN-based high electron mobility transistor (HEMT) has become a promising candidate for high-power and high-frequency applications due to the superior properties of GaN such as wide band gap, high breakdown field, high channel velocity, and high sheet carrier density.¹ Conventional GaN-based heterostructures are grown on sapphire and silicon carbide (SiC) substrates. However, due to the limited substrate size and cost of SiC, the semiconductor industry is currently focusing on GaN-based materials and device development on the more cost effective option such as silicon substrates. The availability of larger diameter Si wafers (12-in.)^{2,3} and well-established complementary-metal-oxide-semiconductor (CMOS) foundry platform has encouraged the on-wafer integration of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ -based HEMTs with the existing state-of-the-art Si CMOS technology.⁴ In the compound semiconductor platform, the conventional Ohmic contacts for such HEMTs are based on Ti/Al/X/Au metallization schemes. Here, X denotes the transition metals such as Ni, Pt, Cr, Ti, and Mo, acting as diffusion barriers between Al and Au.⁵ Among them, the Ti/Al/Ni/Au is the most well-established state-of-the-art Ohmic contact schemes with an average contact resistance ($< 1.0 \Omega \text{mm}$), yielding good switching characteristics and higher drive current performances.^{6,7} However, due to the high diffusivity of Au, such metal schemes are forbidden in a Si CMOS process platform to avoid cross contamination.⁸ Hence, gold-free metal contact schemes are necessary for the fabrication of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMTs on a Si CMOS platform.

Recently, several Au-free and Ti/Al-based metal schemes (Pt, Cu, Ta, and W) are reported in literature. Liu *et al.*⁹ demonstrated Ti/Al/Ni/Pt Ohmic metal schemes annealed at 975 °C in N_2 atmosphere resulting in a contact resistance (R_C) of $\sim 0.6 \Omega \text{mm}$. Similarly, Ta/Si/Ti/Al/Ni/Ta Ohmic metal stack was demonstrated by Li *et al.*,¹⁰ which achieved a $R_C \sim 0.24 \Omega \text{mm}$ when annealed at 800 °C. However, it is noteworthy to emphasize that the low contact resistance can be achieved at the expense of a high temperature ($\geq 800 \text{ °C}$) annealing process. This leads to increased thermal budget, which limits the implementation of a self-aligned gate-first CMOS-type process.¹¹ A low-temperature Au-free metal contact, for the integration of GaN-on-Si in a CMOS fabrication platform, is also reported recently where partial recess source/drain patterns are used to reduce R_C .¹² To avoid process complexity for the fabrication of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMTs on 200-mm Si(111), it is desirable to showcase low-temperature nonrecess Au-free source/drain contacts with an $R_C < 1.0 \Omega \text{mm}$.¹³

Among various metal alloys, nickel-vanadium (NiV) is typically used in the electroplating industry due to its high corrosion resistance and slow oxidation rate. NiV is proposed to promote intermetallic reaction at low temperature while providing a smooth surface morphology.¹⁴ There has been limited work in studying the NiV alloy as cap layer for Ohmic metal stack formation in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMT structures. In this article, we have demonstrated the fabrication of Au-free HEMTs with Ti/Al/NiV as source/drain Ohmic contacts on $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ two-dimensional electron gas (2DEG) heterostructures grown on a 200-mm diameter Si(111) substrate. A detailed electrical characterization is carried out to address the nature of such Ohmic contacts in nitride material system. A low-temperature rapid thermal

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annealing (RTA) process at 500°C has achieved a comparable R_C of $\sim 0.8 \Omega\text{mm}$ without any recess etching. The direct current (DC) characteristics of the fabricated $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMTs using Ni/Al gates are investigated. The interfacial metal distribution and structural changes of the Ti/Al/NiV stack after thermal annealing are also addressed using high-resolution transmission electron microscopy (HRTEM) combined with energy dispersive x-ray (EDX) spectroscopy.

II. EXPERIMENT

The epitaxial growth of the HEMT layers was carried out using an AIXTRON closed coupled showerhead metalorganic chemical vapor deposition system refurbished at IMRE. The $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ -based heterostructures were grown on 200 mm diameter p-type Si(111) substrates. The $3.8\text{--}3.9 \mu\text{m}$ thick HEMT structure on Si(111) comprised of a $\sim 30\text{ nm}$ thick low-temperature AlN nucleation layer, a $\sim 350\text{ nm}$ thick high-temperature AlN layer, three step-graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ intermediate layers, and about $\sim 1.6 \mu\text{m}$ thick GaN buffer. The top layers consist of a $\sim 300\text{ nm}$ undoped GaN channel layer, an ultrathin AlN spacer ($\sim 1.0\text{ nm}$), an undoped $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer ($\sim 20\text{ nm}$), and a thin undoped ($3.0\text{--}4.0\text{ nm}$) GaN cap layer. A cross-sectional scanning transmission electron microscopy (STEM) image of the HEMT stack is shown in Fig. 1(a). The high-resolution x-ray diffraction technique has been used to estimate the Al compositions (x : 23%–24%) in the barrier layer across the wafer through a reciprocal space mapping (RSM). A typical RSM map of this full HEMT structure is shown in Fig. 1(b). To measure the electrical properties of the 2DEG formed beneath the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier, the Hall effect experiments were performed on the diced samples. The Hall data from our HEMT samples show an average sheet resistance of $\sim 430 \Omega/\text{sq}$ with a sheet carrier density of about $\sim 1.1 \times 10^{13} \text{ cm}^{-2}$. In such a HEMT stack,

the Ohmic contact resistance depends on the characteristics of 2DEG formed beneath the top $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer. The Al composition in the barrier layer and its thickness contribute significantly to the electrical data of 2DEG induced by the piezoelectric and spontaneous polarization. In order to achieve lower crystal defects in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier and to avoid composition fluctuations across the 200 mm diameter epiwafer, we have used Al composition of 23%–24% with an underlying $\sim 1\text{ nm}$ AlN spacer layer. During contact annealing step, once the metal diffuses and reaches 2DEG layer, the electrical conduction increases significantly. The Ohmic contact properties may be further tuned with HEMT samples of higher 2DEG sheet carrier concentrations, or by using a different set of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier thicknesses and Al compositions.

The device fabrication starts with a standard organic cleaning by immersing the samples in acetone, methanol, and isopropyl alcohol. Next, active island is defined followed by a mesa isolation etching ($450\text{--}500\text{ nm}$) using an inductively coupled plasma-reactive ion etching system with Cl_2/BCl_3 chemistry at low temperature 6°C . The source/drain regions are defined using optical lithography. For the residual native oxide removal, 60 s HCl dip of patterned samples is done prior to contact metal deposition. The metal stack of Ti/Al/NiV (wt. % of Ni/V $\approx 93\%/7\%$) is then deposited using e-beam evaporator and RF sputtering system followed by a lift-off process. A final lithography step for gate definition is performed, followed by Ni/Al metal deposition to form the Schottky gate electrodes. The schematic illustration and top view optical micrographs of the $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}/\text{GaN}$ HEMT device structure are as shown in Figs. 2(a) and 2(b), respectively.

The Ti/Al/NiV metal stack is optimized in terms of Ti/Al thickness ratio, annealing temperature, and duration in order to achieve the optimum contact resistance. The relative thickness between Ti and Al is important, as these two metals are responsible for the Ohmic contact formation at

FIG. 1. (Color online) (a) Cross-sectional STEM image of the HEMT structure grown on Si(111). (b) The asymmetric (114) RSM of the full HEMT structure with AlN and step-graded AlGaN intermediate layers.

(a)

(b)

FIG. 2. (Color online) (a) Schematic cross-section and (b) Optical micrograph of AlGaIn/GaN HEMT using Ti/Al/NiV as Ohmic contacts and Ni/Al as Schottky gate. S and D represent source and drain, respectively, while G denotes the gate.

the top surface. Ti and Al react with GaN to form a thin interfacial layer of TiN, AlN, or AlTi_2N , generating N vacancies during the RTA process.^{15,16} In order to probe such interfacial behavior and its effect on the electrical characteristics, the Ti/Al/NiV metal stack was annealed at various temperatures ranging from 400 to 700 °C for 30 s in 1500 sccm flow of N_2 . To achieve the lowest contact resistance, the optimum annealing duration window (20–90 s) is also investigated. The DC characteristics of these fabricated HEMTs are then studied when the lowest Ohmic contact resistance is obtained using such Ti/Al/NiV metal schemes.

III. RESULTS AND DISCUSSION

The linear transmission line method (TLM) is employed for extracting the Ti/Al/NiV contact resistance and specific contact resistivity. Figure 3(a) shows the TLM test structure fabricated on the HEMT surface using (Ti/Al/NiV) with square pads ($W=L=100\ \mu\text{m}$) and varying gap spacing ($d=13, 17, 21, 25, 29$, and $37\ \mu\text{m}$). The mesa isolation etching is essential to prevent any unwanted current spreading confining the current flow within the mesa height of conductive epitaxial 2DEG layers. A rough comparison can be seen between the optical micrographs of the TLM test structures shown in Fig. 3. The Ti/Al/NiV contact (RTA 500 °C)

(a)

(b)

FIG. 3. (Color online) Optical micrographs of TLM test structures fabricated using (a) Ti/Al/NiV at 500 °C for 30 s and (b) Ti/Al/NiV/Au at 825 °C 60 s.

exhibits much smoother surface morphology as compared to that of traditional Ti/Al/NiV/Au (RTA at 825 °C) Ohmic metal stack. It is well known that Ti/Al/NiV/Au-based contacts are prone to rough surfaces due to the high temperature annealing and the formation of AlAu_4 alloy.¹⁷ Such a rough surface morphology of contacts are unfavorable for high frequency microwave applications due to nonuniform current distribution, along with the poor line edge definition leading to scalability and reliability issues in GaN RF devices.¹⁸ In contrast, the low-temperature processed Ti/Al/NiV metal contact scheme (with $\sim 70\ \text{nm}$ NiV) employed here shows a root mean square (RMS) surface roughness of 5–6 nm range ($10 \times 10\ \mu\text{m}$ scan area) from atomic force microscopy (AFM) measurements. In our HEMT structures on Si, we explored an optimized NiV layer thickness of $\sim 70\ \text{nm}$ as this is still sufficient to prevent the oxidation of the Ti/Al stack during thermal annealing. On the other hand, a thicker NiV layer may require a higher annealing temperature window.

The I - V characteristics at different gap spacing of the TLM structures are measured using a 4200-SCS Keithley Parameter Analyzer. Figures 4(a) and 4(b) show the I - V characteristics of TLM contact pads fabricated using different Ti/Al thickness combinations (15/300, 20/200, 25/200, and 20/120 nm) while fixing the NiV cap layer thickness the same. The optimized annealing temperature of 500 °C is employed for 30 s. The nonlinear I - V characteristics are observed for Ti/Al thickness (15/300 nm—ratio 0.05) and (20/120 nm—ratio 0.167), as shown in Fig. 4(b) with a much

Fig. 4. (Color online) (a) I - V characteristics measured between two consecutive TLM contact pads (gap spacing = $13\ \mu\text{m}$) with different Ti/Al relative thickness. (b) I - V characteristics of Ti/Al thickness of 15/300 and 20/120 nm.

lower current. The linear Ohmic characteristics are observed for both sets of Ti/Al thickness: (20/200 nm—ratio 0.1) and (25/200 nm—ratio 0.15); with 0.1 ratio of Ti/Al giving rise to the steepest slope for lowest resistance. At this ratio, it is expected that the top Al layer is consumed by reaction with Ti to form Al_3Ti at a low temperature of $\sim 250^\circ\text{C}$, and the excess remaining Ti layer is still in contact with the GaN cap/AlGaN.¹⁹ Due to the presence of NiV alloy layer, we believe that Ti reacts with the thin GaN cap and $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}$ barrier layer during annealing at 500°C that which promotes the catalyzing effect. The lower Ti/Al thickness ratio of 0.05 (15/300 nm) is Al-rich, and due to the fixed annealing temperature and duration, the whole Ti layer is consumed first with some Al remains unreacted resulting in such a non-Ohmic behavior. In contrast, at higher Ti/Al thickness ratio of 0.167 (20/120 nm), the stack is Ti-rich, and the Al layer requires a higher thermal budget (temperature and duration) to achieve a complete reaction.

Next, the Ti/Al thickness ratio is fixed at 0.1 (20/200 nm) for further annealing temperature optimization to achieve the lowest contact resistance. After annealing at different temperatures from 400 to 700°C , the contact resistance for that respective temperature is extracted from the I - V characteristics. A nonlinear behavior is observed for annealing temperatures of 400 and 700°C , respectively. As discussed, at a temperature below 450°C , the total thermal budget is not sufficient for the formation of TiN layer that generates nitrogen vacancy at the interface, which acts as n-type dopants. The linear Ohmic I - V characteristics are obtained between 450 and 600°C annealing condition for 30 s, with highest slope attained at 500°C indicating lowest contact resistance. The contact resistance “ R_c ” and specific contact resistivity (ρ_c) are extracted with values of $\sim 0.8\ \Omega\text{mm}$ and $\sim 6.3 \times 10^{-6}\ \Omega\text{cm}^2$, respectively, at RTA condition 500°C for 30 s as shown in Fig. 5(a). The I - V characteristics of the annealed samples as a function of contact gap spacing are shown in Fig. 5(b). Fixing the temperature at 500°C , the TLM structures undergo different annealing duration from 20 to 90 s to study the best processing time window. Annealing time of 30 s gives us the optimum contact resistance with a good surface morphology. Prolonged annealing might lead to the out-diffusion of Al, while Ti/Al layers are

Fig. 5. (Color online) (a) Total resistance as function of contact spacing. (b) I - V characteristics of each contact spacing of Ti/Al/NiV TLM structures annealed at 500°C for 30 s.

susceptible to be oxidized at higher RTA duration.²⁰ At higher temperature ($>600^\circ\text{C}$), the nonlinear behavior of the I - V characteristics and the higher contact resistance are probably due to the microstructural changes at the metal-semiconductor junction. AFM is employed to study the surface topography of the Ti/Al/NiV contact annealed at different temperatures. Figures 6(a) and 6(b) show the AFM images of Ohmic contacts annealed at 500 and 700°C , respectively. In these $10 \times 10\ \mu\text{m}$ scan areas, the RMS surface roughness increases from $\sim 5.8\ \text{nm}$ at 500°C to $\sim 12.4\ \text{nm}$ at 700°C for the same annealing duration of 30 s. The substantial surface

Fig. 6. (Color online) Three-dimensional-AFM images of Ti/Al/NiV contacts annealed at (a) 500°C and (b) 700°C for 30 s, respectively. The scan area is $10 \times 10\ \mu\text{m}$.

roughness evolution is caused by the microstructural changes and influences the epitaxial film interfaces underneath the metal layer. This affects the electrical characteristics of 2DEG channel probed with such metal junctions. Thus, we observed nonlinear I - V characteristics with an increase in resistance.

The structural changes and elemental distribution of Ti/Al/NiV metal stack at source/drain contacts are studied using the HRTEM and EDX analyses. The optimized sample is achieved by RTA at 500 °C for 30 s as mentioned earlier. The TEM-EDX experiments are performed using a Titan 80–200 kV scanning TEM. The TEM lamella was prepared using a Helios Nanolab 600 dual-beam focused ion beam system. Figure 7(a) shows the cross-sectional TEM images of Ti/Al/NiV metal stack on $\text{GaN}/\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}$ after RTA. A smooth interface of metal and semiconductor layers is observed from the STEM imaging. It has been reported that the mechanism of the formation of high surface roughness in Au-based (Ti/Al/Ni/Au) Ohmic contact on $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructure is due to the agglomeration of low melting point Al metal. During annealing at high temperatures (typically 800 °C) using RTA, the interface forms Ni–Al alloys. In this study of Ti/Al/NiV system, the annealing temperature (500 °C for 30 s using RTA) is lower than the Al melting point. Therefore, the agglomeration of Al is very less likely and results in smooth surface compared to the Ti/Al/Ni/Au-based metal scheme. RTA leads to the intermixing of metal

layers and the distribution of each element is then investigated using the EDX probe. Figure 7(b) shows the elemental distribution of 350 nm thick Ti/Al/NiV metals stack after RTA, where the EDX profile represents the vertical solid line indicated in Fig. 7(a). One EDX spot is taken at every 5-nm step. The elemental profiles of Al and Ni reveal that both elements are distributed within the entire metal stack due to strong intermixing during annealing. The results show that Al diffuses toward the top of the metal stack. It is noticed from our STEM-EDX analysis that at GaN/metal–stack interface, a ternary TiAlNi-based alloy formed whereas other entire stack is AlNiV-based alloy. It is also seen from the EDX profile that V is stable and remained only at the top of the metal stack, acting as an oxygen diffusion barrier layer. The diffusion of oxygen during annealing is also investigated using EDX analysis to show the merit of this metal contact scheme. The oxygen profile intensity as depicted in Fig. 7(b) is very low across the metal stack implying that the NiV cap is highly effective in preventing oxygen diffusion during annealing, which mitigates the oxidation of the Ti/Al-based metal stack. RTA-induced Al diffusion to NiV top layer forms polycrystalline AlNiV-based alloy as seen from EDX profiles. To address the exact crystalline structure of this alloy, further studies may be required using x-ray diffraction and Auger electron spectroscopy. Figure 7(d) shows the interfacial EDX line scan of 100 nm across the Ti/Al/GaN-cap/AlGaN/GaN interfaces

Fig. 7. (Color online) Cross sectional STEM images across the (a) Ti/Al/NiV metal stack with EDX scan line of 350 nm and (b) EDX elemental profile corresponding to the 350 nm line scan. (c) Ti/GaN-cap/AlGaN/GaN interface with EDX scan line of 100 nm and (d) EDX elemental profile corresponding to the 100 nm line scan. The respective scan position of the EDX profile with respect to the TEM images are as indicated with the dashed color lines.

which is performed along the vertical solid line shown in Fig. 7(c). Such analysis is performed to study the diffusion of metal into the GaN-cap/AlGa_N barrier. One EDX spot is taken at every 2-nm step in this case. The EDX elemental profiles of Ti and Al in Fig. 7(d) reveal that both metals diffuse into the top thin GaN cap layer with intermixing between GaN, Al and Ti. Such complex ternary or quaternary metal compounds of GaN, Ti, and Al nitrides at the AlGa_N/GaN/metal interface reduce the barrier height to GaN, and consequently, such alloys lead to a lower Ohmic contact resistance at source/drain.²¹ The recess etching of the thin GaN cap layer and partial thinning of the AlGa_N barrier thickness may provide a better contact path for metal to the 2DEG channel.²² In our HEMT structures, we have used an undoped AlGa_N barrier, a thin AlN spacer and an undoped GaN cap layer. Due to the presence of such a thin undoped GaN cap layer on top of the AlGa_N layer, the non-recess Ti/Al/NiV contact stack might not be able to match the best results reported in the case of Au-based Ohmic contacts. Thus, to further improve the contact resistance using this scheme, researchers could apply a well-controlled precise recess etching at the source/drain region. Nevertheless, the contact resistance value of our Ti/Al/NiV scheme is still comparable to other reported results.^{13,23–26}

Based on the optimized source/drain Ohmic contacts, the Schottky gate is then fabricated using Ni/Al (20/200 nm) metal layers. Figure 8(a) shows the *I*-*V* characteristics of Ni/Al Schottky diode. The Schottky barrier height “ ϕ_b ” and ideality factor “*n*” are extracted to be 0.73 eV and 1.48, respectively, which are comparable to reported Ni-based contacts on AlGa_N/GaN structure.²⁷ A higher ideality factor (*n* > 1) indicates that trap-assisted tunnelling mechanism²⁸ might be present while the lower barrier height might be attributed to interface states in the AlGa_N/GaN structure.²⁹ The value *n* > 1 also signifies the presence of interfacial native oxide layer and barrier inhomogeneities³⁰ as such heterostructures are grown on a larger diameter Si substrate. Compared to other conventional substrates like SiC or sapphire, such large diameter GaN-on-Si epitaxy usually results in a higher density of vacancy-impurity complexes at the top AlGa_N/GaN interfaces, and therefore, a higher interface trap density is expected in our samples.

Figure 8(b) shows the capacitance-voltage and conductance-voltage characteristics of the fabricated Al_{0.23}Ga_{0.77}N/GaN

FIG. 8. (Color online) (a) *I*-*V* characteristics of Ni/Al Schottky diodes on AlGa_N/GaN HEMT and (b) capacitance and conductance-voltage characteristics of AlGa_N/GaN HEMT at 1 MHz.

HEMT using the Ti/Al/NiV Ohmic contact scheme with gold-free Ni/Al gates. A minor hysteresis effect is observed when sweeping the gate bias from -5 to 0 V and back to -5 V. The interface traps density of the AlGa_N/GaN interface is analyzed using the frequency-dependent conductance method³¹ with the following equations:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{\text{AlGa}_N}}{G_m^2 + \omega^2 (C_{\text{AlGa}_N} - C_m)^2}, \quad (1)$$

$$D_{it} \approx \frac{2.5}{qA} \left(\frac{G_p}{\omega} \right)_{\max}, \quad (2)$$

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln \left[1 + (\omega\tau_{it})^2 \right], \quad (3)$$

where G_m and C_m are the measured conductance and capacitance using the equivalent parallel model; C_{AlGa_N} is the zero bias accumulation Al_xGa_{1-x}N capacitances; ω is the frequency; A is the gate area, and q is the electronic charge. The conductance “ G_p/ω ” versus frequency plot at different gate biases and the interface state density “ D_{it} ” as function of trap time constant “ τ_{it} ” is shown in Figs. 9(a) and 9(b), respectively. As the gate bias increases from depletion to near accumulation, the peak intensity of the G_p/ω becomes larger and the corresponding D_{it} value increases. The increase in gate bias induces the 2DEG channel electron to transfer from the AlGa_N/GaN interface to the Schottky gate. These electrons can trap at AlGa_N defect sites. Such acceptor-type trap states are responsible for the higher G_p/ω intensity and D_{it} value. The extracted interface trap density values of 5×10^{12} – 1.8×10^{13} cm⁻² eV⁻¹, with corresponding time constant of 0.35–1.0 μs, are not only comparable but also an order of magnitude lower than reported results with similar Al_xGa_{1-x}N/GaN HEMTs.^{32,33} The trap time constant reduces exponentially with the increase in energy, indicating that the trap states are continuum in nature at the interface. This is in agreement with the reported results where traps with higher energy levels usually take shorter time for trapping/detrapping process.³²

Figure 10 shows the DC output and transfer characteristics of the Al_{0.23}Ga_{0.77}N/GaN HEMT devices with gate width, $W = 100$ μm, $L_g = 2$ μm, and $L_{gd} = 3$ μm. The fabricated device shows a good pinch-off performance at around -3 V with a maximum drain current $I_{D\max} \sim 320$ mA/mm (at

FIG. 9. (Color online) (a) Normalized Conductance “ G_p/ω ” vs frequency “ ω ” characteristics for different gate biases. (b) Energy distribution of as-measured interface-trap density D_{it} and trap time-constant τ_{it} .

FIG. 10. (Color online) (a) DC output characteristics and (b) transfer characteristics of AlGaIn/GaN HEMT fabricated using the Au-free $\text{Ti}/\text{Al}/\text{NiV}$ metal contacts.

$V_G = 2$ V) and a maximum transconductance $g_m \sim 88$ mS/mm (at $V_{DS} = 6$ V). In addition, these AlGaIn/GaN HEMT devices demonstrate excellent I_{ON}/I_{OFF} ratio $\sim 3 \times 10^9$ (with a subthreshold swing (SS) of ~ 71 mV/decade), which is comparable or even higher than previous reports.^{25,34,35} Such device performance is favorable for high-speed power switching applications. As shown in Fig. 11, the fabricated HEMTs exhibit a low gate leakage current at ON-state ($V_{DS} = 8$ V) with $I_G = 3.2 \times 10^{-6}$ mA/mm at $V_G = -20$ V. The low leakage current might be attributed to the lower thermal processing window which is applied throughout the fabrication process in this study. The gate leakage may reduce further if we adopt a metal-insulator-semiconductor (MIS) type HEMT configuration. Such a low-temperature Ohmic metal stack scheme would then allow CMOS type gate-first processing toward the development of low-cost $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ MISHEMTs. It has been reported that the operating temperature of GaN-based depletion mode HEMT devices is up to 265°C and direct-coupled FET logic integrated circuits up to 375°C using enhancement-mode AlGaIn/GaN HEMTs.^{36,37} In this context, the Au-free $\text{Ti}/\text{Al}/\text{NiV}$ metal scheme on GaN/AlGaIn HEMT has potential to operate in such high temperature applications. Though the present device with such contacts might not work at very high temperature ($>500^\circ\text{C}$) environment, it is noteworthy to mention that at such high temperature ambient, the fundamental electronic properties change significantly and proper cooling systems are necessary on the device architectures.

FIG. 11. (Color online) ON-state gate leakage current characteristics of AlGaIn/GaN HEMT at $V_{DS} = 8$ V.

IV. CONCLUSIONS

In summary, we have demonstrated Au-free $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}/\text{GaN}$ HEMTs-on-Si(111) using a low-temperature processed $\text{Ti}/\text{Al}/\text{NiV}$ Ohmic metal stack. A comparable contact resistance “ R_C ” of $\sim 0.8 \Omega\text{mm}$ is achieved with $\text{Ti}/\text{Al}/\text{NiV}$ (20/200/70 nm) metal layers annealed at 500°C for a duration of 30 s. Due to low temperature processing, the devices exhibit very smooth Ohmic contact topography with a lower OFF-state drain current. The HEMTs fabricated in this study show excellent switching performance with an I_{ON}/I_{OFF} ratio $\sim 3 \times 10^9$ and a subthreshold swing “SS” of ~ 71 mV/decade. The metal interdiffusion profiles of $\text{Ti}/\text{Al}/\text{NiV}$ stack at the nitride interface are studied using the scanning TEM-EDX analyses. We believe that the development of such a low-temperature Au-free Ohmic contact scheme may find its applications in GaN-on-Si processing with an additional possibility of integration with a self-aligned process.

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