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Wide-input dynamic range 1 MHz clock ultra-low supply flip-flop

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A new wide-input dynamic range flip-flop capable of operation at an ultra-low supply voltage of 0.16 V is presented. The proposed flip-flop named as capacitively boosted sense-amplifier flip-flop (CB-SAFF) utilises a capacitively boosted sense-amplifier master stage to sense the data signals and amplify them to a voltage higher than the supply and below the ground for driving the slave latch stage with improved strength. Using the same size of input/output transistors and load capacitance, the proposed CB-SAFF outperforms existing state-of-the-art sense-amplifier flip-flop designs at a low supply voltage operation from 0.16 to 0.6 V in terms of *power delay product* and *clock to output propagation delay* performance metrics. In addition, the proposed CB-SAFF can also sample low-swing data signals down to 0.2 V even at a 0.16 V supply voltage and 1 MHz clock frequency, thus making it highly suitable for applications that demand high speed and low power consumption such as for use in ultra-low voltage Internet of Things, wireless sensor nodes and smart motes.

Introduction: The current Internet of Things (IoT) era demands ultra-low power consuming system on chip (SoC) architectures and circuits for use in wireless sensor nodes, biomedical implants and smart motes [1]. One key approach to reduce power consumption is to aggressively scale down the supply voltage at the expense of speed degradation and poor drive capability. To overcome the drawbacks of aggressive voltage scaling, near-threshold computing was introduced where supply voltage was kept approximately equal to threshold voltage for achieving a better balanced performance [2]. Nevertheless, digital circuits operating below threshold voltage still exhibit poor switching speed and drive capability.

One of the indispensable block in any integrated circuit is the flip-flop (FF). Mixed-signal and digital intensive architectures such as SoC, microprocessors and microcontrollers contain digital circuits like memory, counters, frequency dividers and pipelining elements all of which require good FF design for proper operation. Moreover, the emphasis on high-performance FF design is even more critical for use in ultra-low voltage applications. Thus, FFs capable of operation at supply voltages lesser than the threshold voltage with good drive strength, low *clock to output propagation delay* ($C-Q$) and low *power delay product* (PDP) is essential.

Conventional FF topologies such as transmission gate pair, flow-through latch and semi-dynamic FF all suffer from poor drive strength and transistor sizing issues at ultra-low supply voltages which severely degrades its performance [3]. The sense-amplifier FF (SAFF) [4] which consists of a master sense-amplifier (SA) stage and a slave latch stage is an appropriate choice for low supply voltage operation, since it has attractive characteristics such as near-zero setup time, low hold time and single clock phase operation. However, the conventional SAFF [4] has a NAND gate set-reset (SR) latch which has asymmetrical $C-Q$. Moreover, its operation is also not reliable at ultra-low supply voltages.

The asymmetrical $C-Q$ of conventional SAFF was overcome in Nikolic SAFF [5] and Strollo SAFF [6] by utilising a symmetrical slave latch. There are also other recently proposed improved SAFF topologies namely boost-bulk SAFF (BB-SAFF) [7] and transition completion detection SAFF (TCD-SAFF) [8]. Nevertheless, all these SAFF topologies still suffer from poor driving capability at ultra-low supply voltages leading to speed degradation and poor PDP performance. In addition, the existing SAFF topologies also cannot sample low voltage swing data signals which is essentially required for IoT sensor nodes, biomedical implants and smart motes.

Proposed CB-SAFF: The proposed CB-SAFF consists of a SA master stage followed by a SR latch slave stage as shown in Fig. 1. All NMOS body is connected to ground and all PMOS body is connected to V_{DD} , except for the transistors explicitly shown. The SA stage shown in Fig. 1a utilises a capacitive boosting technique [9] using two metal-oxide semiconductor capacitors MC1 and MC2 to sense the data signals and amplify them to generate a large voltage swing from $-\beta V_{DD}$ to βV_{DD} for driving the SR latch shown in Fig. 1b, where β is the boosting efficiency and is <1 due to parasitic capacitance at

node A and node B. The operation of the proposed CB-SAFF is explained as follows.

Fig. 1 Capacitively boosted SAFF

a Capacitively boosted SA master stage
b SR latch slave stage

When the clock signal CLK is low, the buffer B1 connects one terminal of the boost capacitor MC1 to ground and buffer B2 turns on the pre-charge transistor PT1 to charge MC1 to supply voltage V_{DD} and connects node A to V_{DD} . Buffer is used to prevent the loading of clock signal with capacitor and to aid in boosting the node A to βV_{DD} when CLK turns high. Similarly, the inverter INV1 turns on the pre-charge transistor PT2 to charge MC2 to V_{DD} . The SA stage outputs $\bar{S}$ and R are pre-charged to V_{DD} through transistors P1 and P4. This makes the slave SR latch to hold the previous value using its cross-coupled inverter stages P6-N7 and P7-N8. During this state, changes in data signals do not affect the output of SA since transistor N1 is off.

When the clock signal CLK turns high, the SA senses the differential inputs applied at D , $\bar{D}$ and for instance, if D is high and $\bar{D}$ is low, $\bar{S}$ is discharged to node Z through N4-N2. At the same time, N1 is turned on to deliver the boosted voltage of $-\beta V_{DD}$ to node Z. Thus, $\bar{S}$ is discharged to boosted $-\beta V_{DD}$ instead of ground unlike other existing SAFF topologies. Parallely, PT1 is turned off and node A is connected to boosted supply of βV_{DD} through B1-MC1 instead of V_{DD} unlike existing SAFF topologies, thereby charging R to boosted supply of βV_{DD} . At the latch side, the discharge boosted $\bar{S}$ turns on P5 with increased strength to pull-up Q to V_{DD} and the charge boosted R turns on N14 with increased strength to pull-down Q to ground. The operation is similar and vice-versa when D is low and $\bar{D}$ is high. The always turned-on N6 ensures static operation, so that either S or R can always be discharged to ground even when data input changes when CLK is high.

Simulation results: The proposed CB-SAFF has been designed in 40 nm CMOS along with the conventional SAFF [4], Nikolic SAFF [5], recently proposed BB-SAFF [7] and TCD-SAFF [8] for evaluation of performance metrics in same environment. All SAFFs are individually optimised, use same size input/output transistors and load capacitance of 15 fF for fair comparison. All the SAFFs were simulated under the ultra-low to low supply voltage regime from 0.16 to 0.7 V using CLK of both 1 and 50 MHz at a 50% data switching activity ($\alpha=50\%$) as shown in Fig. 2. The proposed CB-SAFF achieves the least PDP among others from 0.16 to 0.6 V supply and is also the only FF which can operate at 0.16 V supply. The supply is restricted to be below 0.7 V to avoid forward biasing the parasitic diodes which will lead to increased power consumption as can be observed in Fig. 2. The setup time and hold time of the proposed CB-SAFF at 0.5 V supply/1 MHz clock is -10.94 and 25.18 ps, respectively. The rise and fall $C-Q$ also exhibits good symmetrical property at clock frequencies of both 1 and 50 MHz as shown in Fig. 3.

Fig. 2 Variation of PDP with supply voltage V_{DD}
 a Clock frequency of 1 MHz, D and $CLK = 1$ V swing
 b Clock frequency of 50 MHz, D and $CLK = 1$ V swing

Fig. 3 Variation of C-Q delay with supply voltage V_{DD}

From Table 1, it is evident that the proposed CB-SAFF achieves better performance than existing state-of-the-art SAFF designs at a low supply voltage. With its capacitive boosting, the proposed CB-SAFF can sample low-swing data signals at low supply voltages even at CLK of both 1 and 50 MHz where other FFs could not work reliably. From simulations, the proposed CB-SAFF was the only FF which sampled low-swing data signals from 0.2 to 1 at 0.5 V supply/50 MHz CLK . It was also the only FF to accurately sample data signals from 0.2 to 1 V even at an ultra-low supply of 0.16 V/1 MHz CLK as shown in Fig. 4, thereby demonstrating its capability of wide-input dynamic range and ultra-low supply voltage operation.

Table 1: Performance comparison of SAFF designs at CLK of 50 MHz

SAFF	Proposed	[5]	[7]	[8]
C-Q delay (rise) (ps)	86.4	492.3	481.5	520.7
C-Q delay (fall) (ps)	86.2	396.2	958.7	929.4
power (nW)	605.5	206.8	190.4	213.7
supply (V)	0.5	0.5	0.5	0.5
PDP (aJ) @ $\alpha = 50\%$	52.3	101.8	182.6	198.6
min V_{DD} , $CLK = 1$ MHz	0.16	0.2	0.2	0.2
min V_{DD} , $CLK = 50$ MHz	0.35	0.35	0.45	0.4
sample low-swing data	yes	no	no	no
sum of widths (μm)	35.1	24.2	30.4	22

Fig. 4 Output waveform at $D = 0.2$ V, $CLK = 1$ MHz and $V_{DD} = 0.16$ V

Conclusion: A novel wide-input dynamic range ultra-low supply FF which utilises a capacitively boosted SA master stage and slave latch stage is designed in 40 nm CMOS. The proposed CB-SAFF can operate even at an ultra-low supply of 0.16 V at 1 MHz clock and achieves better PDP and propagation delay performance than existing SAFF designs. With its capacitive boosting feature, the proposed CB-SAFF can reliably sample low-swing data signals even at low supply voltages and clock frequencies of 1 and 50 MHz, making it an appropriate choice for IoT applications, smart motes and ultra-low voltage VLSI design.

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One or more of the Figures in this Letter are available in colour online.

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