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Asynchronous-Logic QDI Quad-Rail Sense-Amplifier Half-Buffer Approach for NoC Router Design

Weng-Geng Ho, Kwen-Siong Chong, Ne Kyaw Zwa Lwin, Bah-Hwee Gwee and Joseph S. Chang

Abstract—We propose a low area overhead and power-efficient asynchronous-logic (async) Quasi-Delay-Insensitive (QDI) Sense-Amplifier Half-Buffer (SAHB) approach with quad-rail (i.e. 1-of-4) data encoding. The proposed quad-rail SAHB approach is targeted for area- and energy-efficient Asynchronous Network-on-Chip (ANoC) router design. There are three main features in the proposed quad-rail SAHB approach. First, the quad-rail SAHB is designed to use 4 wires for selecting 4 ANoC router directions, hence reducing the number of transistors and area overhead. Second, the quad-rail SAHB switches only 1 out of 4 wires for 2-bit data propagation, hence reducing the number of transistor switchings and dynamic power dissipation. Third, the quad-rail SAHB abides by QDI rules, hence the designed ANoC router features high operational robustness towards Process-Voltage-Temperature (PVT) variations. Based on the 65nm CMOS process, we use the proposed quad-rail SAHB to implement and prototype an 18-bit ANoC router design. When benchmarked against the dual-rail counterpart, the proposed quad-rail SAHB ANoC router features 32% smaller area and dissipates 50% lower energy under the same excellent operational robustness towards PVT variations. When compared to the other reported ANoC router, our proposed quad-rail SAHB ANoC router is one of the high operational robustness, smallest area, and most energy-efficient designs.

Index Terms—Asynchronous Network-on-Chip (ANoC) router, Quasi-Delay-Insensitive (QDI), Process-Voltage-Temperature (PVT) variations, energy-efficient, quad-rail data encoding.

I. INTRODUCTION

Multi-core processing is a promising option to increase the computation speed in many applications nowadays. In the multi-core processing, the use of Network-on-Chip (NoC) router to link all the processing cores for efficient data communication is widely adopted [1]. To-date, there are many NoC routers reported [2]-[14], including those based on fully synchronous-logic (sync) [2]-[3] and those in part based on asynchronous-logic (async) [4]-[14]. The design of sync NoC routers [2], [3] however, becomes increasingly more challenging due to the timing issues for operation correctness [15]. The timing issues are further compounded in view of wider Process-Voltage-Temperature (PVT) variations [16] in deep-submicron fabrication processes.

Conversely, the design of async NoC (ANoC) routers [4]-[14] has increasingly become attractive in accommodating timing and data synchronization issues because their operations are essentially self-timed. In the ANoC router designs, the Quasi-Delay-Insensitive (QDI) timing model with 1-of- n rails data encoding is well known to accommodate the PVT variations [17].

However, the ANoC router design using the async QDI handshake protocol has higher circuit complexity as compared to the sync NoC router design due to the following reasons. First, the async QDI

handshake protocol requires input completion and output completion circuits to validate the input and output completeness for every pipeline stage [18]. Second, the use of well-established dual-rail data encoding increases the computation block complexity and the number of wires along the pipeline stage [17]. In short, the ANoC router suffers from high area overhead due to the increased circuit complexity, and high dynamic power dissipation due to the increased number of switching in the data propagation.

In this paper, we propose a quad-rail Sense-Amplifier Half-Buffer (SAHB) approach with low area overhead, power-efficient and high operational robustness towards PVT variations, for implementing the ANoC router design. First, we design the quad-rail SAHB to use 4 wires for selecting 4 ANoC router directions, as compared to dual-rail approach that uses 2-rail wires for the same function. Second, we design the quad-rail SAHB to switch only 1 out of 4 wires for 2-bit data propagation, as compared to dual-rail approach that switch 2 out of 4 wires. Third, we design the quad-rail SAHB to abide by QDI rules for ensuring its operational robustness.

Based on 65nm CMOS process, we implement and prototype an ANoC router using the proposed quad-rail SAHB approach. When benchmarked against the dual-rail counterpart, the proposed quad-rail SAHB ANoC router features 32% smaller area and dissipates 50% lower energy under the same excellent operational robustness towards PVT variations. When compared to the other reported ANoC routers, our proposed quad-rail SAHB ANoC router is one of the smallest area, high operational robustness, and most energy-efficient design.

The paper is organized as below. Section II elaborates our proposed quad-rail SAHB cell, and the circuit and pipeline analysis. Section III elaborates our proposed ANoC router's architecture. Section IV presents the chip implementation and measurement results. Finally, Section V draws the conclusions.

II. PROPOSED QUAD-RAIL SAHB

We leverage on our SAHB realization approach [18], and design the async cells in quad-rail encoding. For ANoC router design, the basic quad-rail cells are buffers (BUF), multiplexers (MUX) and demultiplexers (DEMUX). The SAHB quad-rail cells are designed at transistor-level. For sake of simplicity, we only elaborate the SAHB quad-rail 4-to-1 MUX cell; the other cells can be built based on the same concept.

Fig. 1 (a) depicts the block diagram of the SAHB quad-rail 4-to-1 MUX cell (with generic interface signals), which comprises 4 quad-rail input data (L_0, L_1, L_2, L_3), a quad-rail input select data (S), a quad-rail output data (R), an acknowledgement signal from the succeeding pipeline ($Rack$), and acknowledgement signals to the preceding pipeline ($Lack_0, Lack_1, Lack_2, Lack_3$ and $Lack_S$). The complimentary signals are bundled for simplifying the cell structure.

Fig. 1 (b) depicts the pipeline diagram of the SAHB quad-rail 4-to-1 MUX, which comprises 4 functional blocks (FB) + 2 Control-Logic cum Sense-Amplifier (CLSA), input completion detection (ICD), output completion detection (OCD) and C-Muller tree (CT). The (4 FBs + 2CLSAs) block propagates L_0, L_1, L_2, L_3 and S to R based on $Rack$. The ICD validates the input availability/nullity by generating input validity signal Val for each input data, the OCD validates the output availability/nullity, and finally CT generates $Lack$ for each input

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W.-G. Ho and K.-S. Chong are with Temasek Laboratories, Nanyang Technological University, Singapore 637553 (e-mail: wgho@ntu.edu.sg; kschong@ntu.edu.sg).

K. Z. L. Ne, B.-H. Gwee and J. S. Chang are with the Virtus, IC Design Centre of Excellence, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: kzlne@ntu.edu.sg; ebhwee@ntu.edu.sg; ejchang@ntu.edu.sg).

Fig. 1: Proposed Quad-Rail SAHB 4-to-1 MUX Cell (a) Block Diagram, (b) Pipeline Diagram, (c) Cell Diagram, (d) 0th-rail Functional Block and (e) 0th-rail and 1st-rail Control-Logic cum Sense-Amplifier (CLSA)

data. The operation sequences are as follows. Initially, L_0, L_1, L_2, L_3 and S are empty, R is empty, $Val = '0'$, $Rack = '0'$, $Lack = '0'$. When all input data arrive (L_0, L_1, L_2, L_3 and S are valid), Val is triggered to '1' and R is evaluated to be valid, triggering $Lack$ to '1'. When the succeeding pipeline accepts R , $Rack$ is triggered to be '1'. When all input data precharge (L_0, L_1, L_2, L_3 and S are empty), Val is negated to '0' and R is precharged to be empty, triggering $Lack$ to '0'. When the succeeding pipeline is precharged, $Rack$ is negated to be '0'. The pipeline is now ready for a new operation cycle.

Fig. 1 (c) depicts the cell diagram of the SAHB quad-rail 4-to-1 MUX, which comprises 4 FBs, 2 CLSAs, 5 ICDs, an OCD and a CT. The FBs, as depicted in Fig. 1(d), evaluate/precharge L_0, L_1, L_2, L_3 and S to R , depending on $Rack$. The CLSAs, as depicted in Fig. 1(e), control the sequence of async operation, and help amplifying/latching R . The ICDs generate $Val_{L,0}, Val_{L,1}, Val_{L,2}, Val_{L,3}$ and Val_S to validate the input availability/nullity. The OCD and CT generate $Lack_0, Lack_1, Lack_2, Lack_3$ and $Lacks$ to acknowledge the preceding stage.

In the quad-rail SAHB 4-to-1 MUX cell, there are two supply voltages, namely V_{DDA} for FBs, and V_{DD} for remaining blocks (CLSA, ICD, OCD and CT). For proper operation, $V_{DD} \geq V_{DDA}$. V_{DDA} is fixed as sub-threshold voltage ($\sim 0.3V$) to fully minimize the switching power without comprising the evaluation/precharge speed since the output is amplified through CLSA. On the other hand, V_{DD} is adjustable from nominal voltage (1.2V) for speed-critical applications, to near-threshold voltage ($\sim 0.6V$) and even sub-threshold voltage ($\sim 0.3V$) for low power low speed applications.

The overall SAHB cell approach abides by QDI attributes where the input-completeness [17] and acknowledgement (between pipelines) are preserved [15] for high operational robustness. For the input-completeness, the transistor configuration of the quad-rail input data signals of the CLSA (in Fig. 1(e)) validates the data availability/nullity, and switch 'on'/'off' the CLSA for evaluate/precharge operation. For the acknowledgement, both FB and CLSA embody the output

acknowledge signal ($Rack$) sending from the succeeding pipeline to repeatedly run the alternate 4-phase evaluate and precharge operation cycles.

To analyze and evaluate our proposed quad-rail SAHB cells, we compare their transistor-count and number of transitions per-cycle against the reported dual-rail SAHB cells [18]. Since the quad-rail cells propagate 2-bit data in the pipeline, we normalize the readings to single-bit for fair comparison with dual-rail counterparts (propagate 1-bit data). The comparison is made for 4 basic NoC functions: 1-to-1 buffering, 1-to-2 de-multiplexing, 2-to-1 multiplexing and 4-to-1 multiplexing. For sake of simplicity, we only analyze 4-to-1 multiplexing function; the other functions can be analyzed similarly.

First, from the circuit-level perspective, the transistor-count per-bit, $TC(4\text{-to-1 MUX})$ with the transistor-count of the cell's components such as FB, CLSA, ICD, OCD, CT and Inverter (Inv) can be calculated, as expressed in (1).

$$TC(4\text{-to-1 MUX}) = \frac{1}{2} [4 \cdot TC(FB) + 2 \cdot TC(CLSA) + 5 \cdot TC(ICD) + TC(OCD) + TC(CT) + 4 \cdot TC(Inv)] \quad (1)$$

where $TC(FB) = 22$, $TC(CLSA) = 14$, $TC(ICD) = 10$, $TC(OCD) = 8$, $TC(CT) = 48$, $TC(Inv) = 2$

Second, from the pipeline-level perspective, we depict the 3-stage marked graph behavior for our proposed quad-rail SAHB cell approach in Fig. 2. This graph illustrates evaluate operation (F^e , Inv^e , ICD^e , OCD^e and CT^e) and precharge operation (F^p , Inv^p , ICD^p , OCD^p and CT^p) to propagate the data within i -th, $(i+1)$ -th and $(i+2)$ -th pipeline stages in cycle basis. In Fig. 2, the bold lines represent the signal transitions that constitute to cycle time, the longest time for completing one local cycle within 3 pipeline stages [15]. The non-bold lines represent the internal signal transitions within these 3 pipeline stages. The dotted lines represent the external signal transitions outside the pipelines not shown in Fig. 2. After completing one cycle, another new cycle can be initiated.

Fig. 2: 3-stage Marked Graph Behavior of SAHB Quad-Rail 4-to-1 MUX Cell

From the 3-stage marked graph behavior, the number of transitions per-bit for one cycle, $T(4\text{-to-1 MUX})$ with delay, t of the cell's components can be calculated, as expressed in (2).

$$T(4\text{-to-1 MUX}) = \frac{1}{2} [t(F^e_i) + t(Inv^e_i) + t(F^e_{i+1}) + t(Inv^e_{i+1}) + t(F^e_{i+2}) + t(Inv^e_{i+2}) \\ + t(OCD^e_{i+2}) + t(CT^e_{i+2}) + t(F^p_{i+1}) + t(Inv^p_{i+1}) + t(OCD^p_{i+1}) + t(CT^p_{i+1})] \quad (2)$$

where $t(F^e) = t(F^p) = 2$ trans., $t(Inv^e) = t(Inv^p) = 1$ tran., $t(OCD^e) = t(OCD^p) = 1$ tran. and $t(CT^e) = t(CT^p) = 2$ trans.

Figs. 3 (a) and (b) depict the quad-rail and dual-rail SAHB realizations of 2-bit 4-to-1 multiplexing function respectively. In Fig. 3(a), the quad-rail SAHB requires only 1 quad-rail 4-to-1 MUX cell, resulting in $TC = 111$ and $T = 9$. In Fig. 3(b), the dual-rail SAHB requires 6 dual-rail 2-to-1 MUX cells, resulting in $TC = 240$ and $T = 54$. In short, the quad-rail SAHB reduces $2.16\times$ lower TC and $6\times$ lesser T than the dual-rail SAHB. This is because the quad-rail SAHB 4-to-1 MUX cell can select 1 out of 4 input data by matching each input data to each wire of the quad-rail (i.e. 4-wire) select data; 4 input data are matched to 4 wires. Whereas the dual-rail SAHB 2-to-1 MUX cell can only select 1 out of 2 input data, hence more number of dual-rail cells are required to perform the same function.

For completeness, Table I tabulates the logic gate combinations, TC and T for quad-rail and dual-rail SAHB cell approaches in 4 different 2-bit ANoC functions. In realizing 1-to-1 buffering, 1-to-2 demultiplexing and 2-to-1 multiplexing functions for 2-bit data, the dual-rail SAHB embodies 2 dual-rail cells, in contrast to the quad-rail SAHB which embodies only 1 quad-rail cell. Although the quad-rail cells require $\sim 2\times$ more transistor-count than the dual-rail cells, the quad-rail SAHB function is advantageous in terms of TC , i.e. $\sim 7\%$ lower TC than the dual-rail SAHB due to the sharing of completion detection circuits for 2-bit data propagation in the quad-rail SAHB. In terms of T , the quad-rail SAHB cells only trigger 1 out of 4 wires, in contrast to dual-rail SAHB cells, which trigger 2 out of 4 wires in 2-bit ANoC functions. The dual-rail SAHB suffers from $2\times$ more T than the quad-rail SAHB.

In summary, the quad-rail SAHB cells, on average, reduce $1.33\times$ TC and $3\times$ T respectively than the dual-rail SAHB cells, resulting in better performance.

Fig. 3: Realization of 2-bit SAHB 4-to-1 Multiplexing Function (a) Quad-Rail and (b) Dual-Rail

III. PROPOSED ANoC ROUTER ARCHITECTURE

The targeted ANoC router design, as depicted in Fig. 4, comprises five interfaces, each having an input port (IP) and an output port (OP). Four interfaces are used to transfer data to/from four directions (i.e. north (N), east (E), south (S) and west (W)) between two neighboring ANoC routers/I/Os, and the last interface to transfer data between the ANoC router and its respective processing core.

Fig. 4: ANoC Router Interfaces

Figs. 5 (a) and (b) depict the block diagram of the ANoC router's IP and OP respectively. The bold dark arrows represent the data packet, the straight arrows represent the control signals and the dotted arrows represent the acknowledge signals. In the IP and OP, every data packet and control signal are accompanied by an acknowledge signal for one complete async handshake 4-phase QDI operation. More details of the IP and OP could be found from the literature [19]. In the implemented ANoC router, the Buffer, Virtual Channel (VC) DeMux, Direction Switch and VC Switch blocks respectively embodies SAHB quad-rail BUF cells, 1-to-2 DEMUX cells, 4-to-1 MUX cells, and 2-to-1 MUX cells.

IV. MEASUREMENT RESULTS

The proposed quad-rail SAHB ANoC router is implemented by the full-custom approach based on the 65nm standard-threshold-voltage CMOS process ($V_t \sim 0.5V$) and fabricated through STMicroelectronics's Circuits Multi-Projects (CMP) solutions. Fig. 6 depicts the microphotograph of the proposed quad-rail SAHB ANoC router and the test structure.

TABLE I. COMPARISON OF 2-BIT NOC FUNCTIONS BETWEEN QUAD-RAIL AND DUAL-RAIL SAHB CELL APPROACHES

2-bit SAHB ANoC's Functions	Logic Gate Combination		Transistor-Count/bit, TC		No. of Transitions/(cycle $\times$ bit), T	
	Quad-Rail	Dual-Rail	Quad-Rail	Dual-Rail	Quad-Rail	Dual-Rail
1-to-1 Buffering	1 QR BUF	2 DR BUF	33 (1 $\times$)	34 (1.03 $\times$)	6 (1 $\times$)	12 (2 $\times$)
1-to-2 De-Multiplexing	1 QR 1-to-2 DEMUX	2 DR 1-to-2 DEMUX	87 (1 $\times$)	90 (1.03 $\times$)	7 (1 $\times$)	14 (2 $\times$)
2-to-1 Multiplexing	1 QR 2-to-1 MUX	2 DR 2-to-1 MUX	73 (1 $\times$)	80 (1.1 $\times$)	9 (1 $\times$)	18 (2 $\times$)
4-to-1 Multiplexing	1 QR 4-to-1 MUX	6 DR 2-to-1 MUX	111 (1 $\times$)	240 (2.16 $\times$)	9 (1 $\times$)	54 (6 $\times$)
Average	-	-	1 $\times$	1.33 $\times$	1 $\times$	3 $\times$

Fig. 5: ANoC Router Interface (a) Input Port, and (b) Output Port

Fig. 6: Microphotograph of the Proposed SAHB ANoC Router

Figs. 7 (a) and (b) depict the area breakdown of the implemented quad-rail and dual-rail SAHB ANoC routers respectively. The quad-rail SAHB ANoC router occupies 0.105mm^2 , $1.47\times$ smaller area than the dual-rail counterpart. This is due to the simpler implementation in quad-rail SAHB library cells than the dual-rail implementation (which requires on average $1.33\times$ more transistors, in Table I). As seen, the area of direction switch (4-to-1 multiplexing function) reduces significantly from 53% in dual-rail design to 38% in quad-rail design; this mainly reduces the overall area.

To demonstrate the operational robustness towards PVT variations, we compare the throughput and energy dissipation of the proposed quad-rail SAHB ANoC router against three related QDI counterparts, i.e. dual-rail SAHB [18], quad-rail Weak-Conditioned Half-Buffer (WCHB) [9] and quad-rail Pre-Charged Half-Buffer (PCHB) [10]. These comparison are evaluated under various variations of supply

voltages (0.3V, 0.6V, 0.9V, 1.2V), operating temperatures (-40°C , 27°C , 100°C) and process threshold voltages (LVT, SVT, HVT), as depicted in Figs. 8 (a), (b) and (c) respectively.

Fig. 7: IC Area for SAHB ANoC Routers (a) Quad-Rail and (b) Dual-rail

Now we elaborate the overall comparison in these variations. When compared to the dual-rail SAHB, the proposed design features $\sim 50\%$ lower energy dissipation due to the adoption of quad-rail data encoding which reduces $1.33\times$ transistor-counts and $3\times$ transitions/cycle. The trade-off is slightly low throughput partly due to a more complex completion detection. When compared to the quad-rail WCHB, the proposed design features $\sim 15\%$ higher throughput and $\sim 13\%$ lower energy dissipation. When compared to the quad-rail PCHB, the proposed design features $\sim 27\%$ lower energy dissipation. These improved attributes are achieved because the proposed SAHB approach embodies FBs that operate in sub-threshold region ($V_{DDA} = 0.3\text{V}$) to dissipate significantly low power ($<1\mu\text{W}$), and CLSAs that employ sense-amplifiers to enhance the speed, resulting in high energy efficiency.

Fig. 8: Energy vs Throughput of ANoC Routers for Variations of (a) Supply Voltage, (b) Operating Temperature and (c) Process Threshold Voltage

Fig. 9 depicts the latency and throughput of the proposed SAHB ANoC router by varying V_{DD} from 1.2V to 0.3V; the results are normalized with respect to the readings @1.2V. As seen, V_{DD} is adjustable from nominal voltage, 1.2V (with 5.7ns latency, 258MHz throughput) for speed-critical applications, to near-threshold voltage, 0.6V (with 2.7 $\times$ latency, 0.35 $\times$ throughput), and sub-threshold voltage, 0.3V (with 38 $\times$ latency, 0.03 $\times$ throughput) for low power low speed applications.

Fig. 9: Normalized Latency and Throughput of Proposed SAHB ANoC Router for Various V_{DD}

For completeness, Table II tabulates the comparison of various ANoC routers, where the results, i.e. area, latency, throughput and energy dissipation per-bit of the reported ANoC routers [4]-[13] are normalized with respect to the proposed SAHB ANoC router @65nm CMOS, 1.2V based on technology scaling [20]. In terms of robustness towards PVT variations, the ANoC routers based on the QDI handshake protocol features high operational robustness as compared to those based on bundled-data and timed handshake protocols. This is due to the absence of timing issues in QDI handshake protocol.

Furthermore, their process technology, design architecture and implementation are different, hence a direct comparison of various ANoC routers is somewhat contentious. For example, the reported ARGON [13] and ONIZAWA [12] appear to dissipate lower normalized energy per-bit than our SAHB design, but they are not robust towards PVT variations. In addition, the reported ARGON needs to be associated by an external controller for complete operations, hence dissipating additional energy overhead. When compared within all QDI ANoC routers, our SAHB design is respectively 35%, 56% and 85% more energy-efficient than the reported FAUST [7], ALPIN [9] and ALHUSSIEN [10].

V. CONCLUSIONS

We have proposed an async QDI quad-rail SAHB approach with emphases on low area overhead and power-efficient, for ANoC router design. Based on the 65nm CMOS process, we have implemented and prototyped an 18-bit quad-rail SAHB ANoC router. When

benchmarked against the dual-rail counterpart, the proposed quad-rail SAHB ANoC router features 32% smaller area and dissipates 50% lower energy under the same excellent operational robustness towards PVT variations. When compared to the other reported ANoC routers, our proposed quad-rail SAHB ANoC router is one of the high operational robustness, smallest area, and most energy-efficient designs.

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TABLE II. COMPARISON OF VARIOUS ANOC ROUTERS

ANoC Routers	Word-length	Handshake Protocol	Data-encoding	Cell Design Approach	Robustness to PVT Variations	CMOS	V_{DD}	Normalized Area (mm ²) [#]	Normalized Latency (ns) [#]	Normalized Throughput (MHz) [#]	Normalized Energy Dissp. per-bit (fJ/bit) [#]
QNoC [4]	10-bit	Bundled-data	Single-rail	Standard	Low	350nm	-	0.016	1.86	404	-
MANGO [5]	33-bit	Bundled-data	Single-rail	Standard		130nm	1.2V	0.069	4.10	1300	-
SCAFFI [6]	8-bit	Bundled-data	Single-rail	Standard		180nm	1.8V	0.043	-	252	2468
ASPIN [8]	32-bit	Bundled-data	Single-rail	Standard		90nm	1.2V	0.019	1.37	989	587
HORAK [11]	32-bit	Bundled-data	Single-rail	Mousetrap		90nm	1.2V	0.012	0.40	1482	506
ARGO [13]	32-bit	Bundled-data	Single-rail	Mousetrap		65nm	1.2V	0.008	3.02	746	262
ONIZAWA [12]	34-bit	Timed	Dual-rail	LEDR		130nm	1.2V	0.023	1.37	1052	247
FAUST [7]	32-bit	QDI	Dual-rail	WCHB	High	130nm	1.2V	0.113	3.00	320	635
ALPIN [9]	32-bit	QDI	Quad-rail	WCHB		65nm	1.2V	0.170	2.30	550	938
ALHUSSIEN [10]	66-bit	QDI	Dual-rail	PCHB		65nm	1.0V	0.025	10.40	100	2824
Proposed SAHB	18-bit	QDI	Quad-rail	SAHB		65nm	1.2V	0.105	5.69	258	413

[#]The readings are normalized with respect to the proposed SAHB ANoC Router @65nm CMOS, 1.2V