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A Micropower Low-Voltage Multiplier With Reduced Spurious Switching

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***Abstract*—We describe a micropower 16×16-bit multiplier (18.8 μW/MHz @1.1 V) for low-voltage power-critical low speed ($\leq$ 5 MHz) applications including hearing aids. We achieve the micropower operation by substantially reducing (by $\sim$62% and $\sim$79% compared to conventional 16×16-bit and 32×32-bit designs respectively) the spurious switching in the Adder Block in the multiplier. The approach taken is to use latches to synchronize the inputs to the adders in the Adder Block in a predetermined chronological sequence. The hardware penalty of the latches is small because the latches are integrated (as opposed to external latches) into the adder, termed the Latch Adder (LA). By means of the LAs and timing, the number of switchings (spurious and that for computation) is reduced from $\sim$5.6 and $\sim$10 per adder in the Adder Block in conventional 16×16-bit and 32×32-bit designs respectively to $\sim$2 in our designs. Based on simulations and measurements on prototype ICs (0.35 μm three metal dual poly CMOS process), we show that our 16×16-bit design dissipates $\sim$32% less power, is $\sim$20% slower but has $\sim$20% better energy-delay-product (EDP) than conventional 16×16-bit multipliers. Our 32×32-bit design is estimated to dissipate $\sim$53% less power, $\sim$29% slower but is $\sim$39% better EDP than the conventional general multiplier.**

***Index Terms*—Arithmetic, low power, low-voltage, multiplier, switching activity.**

I. Introduction

THE current art in hearing instrument (hearing aid) design is to replace most of the analog signal processing circuit with a digital signal processor (DSP) for increased signal processing capabilities. For aesthetic and light weight for comfort of wear considerations, this portable digital electronic device is powered remotely and its power source is typically a low capacity ($\sim$100 mA·h) low-voltage (1.1 –1.4 V) miniature pill-size cell. This power-critical application necessitates the embodied digital circuits and peripheral circuits [1] to be micropower and power efficient. The degree of complexity of the signal processing is usually limited by the amount of power dissipation tolerable that in turn determines the life span of the battery. In the hearing instrument, the life of the battery is usually expected to be $\sim$100 hours or more. In view of this tight power constraint, highly desirable complex signal processing algorithms such as real-time noise reduction [2] are yet to be fully realized.

Technological advances to meet the challenges of low-voltage, low power and yet realize complex computation in the mixed-signal digital hearing instrument include analog signal conditioning [3] and digital circuit designs. Digital design methodologies [4] for low power operation span from system-level design to transistor-level design and the fabrication process. The system-level design includes the system architecture (including pipelining, parallel processing, etc.), minimum voltage operation (limiting the speed of the transistors), type of signaling protocol, etc. [4]–[6]. One mid-level design consideration is the design architecture of the digital circuit cells (for the cell library) including the adder, multiplier, accumulator, etc. [4], [6], [7]. In general, where the operating voltage is low, for example, 1.1 V, the conventional static CMOS logic (as opposed to pass-transistor logic, etc.) is often employed because of its full swing rail-to-rail output for noise margin considerations.

Of the digital cells, the parallel multiplier is one of the highest power dissipative cells and is a basic module of a DSP. Of the different parallel multiplier designs, the tree-based (Wallace tree, Wallace & Dadda's scheme, algorithmic approach) [8]–[10] and array-based structures [10], [11] are ubiquitous for their respective high speed and regular layout (small area) attributes. In terms of power dissipation, the tree-based structure is potentially lower power than the array-based structure if the former is properly designed [12]. This is because the tree-based multiplier embodies a smaller number of rows of adders in the Adder Block (refer to Fig. 1 later) compared to the array-based multiplier, hence the consequent lower spurious switching (see later) but at the cost of the increased layout difficulty and possibly increased parasitic. In other words, the power dissipation (and speed and integrated circuit (IC) area) of a tree-based multiplier would, to a large degree, depend on layout and fabrications technology specifics. In view of our intended hearing instrument application where small IC area and ease of implementation (many power critical circuit blocks are custom designed) in layout are imperative, and where speed is secondary (<5 MHz), we will only consider the parallel array-based multiplier for comparisons with our design (see Section V). At this outset, it would be worthwhile to note that the method we propose in this paper to reduce

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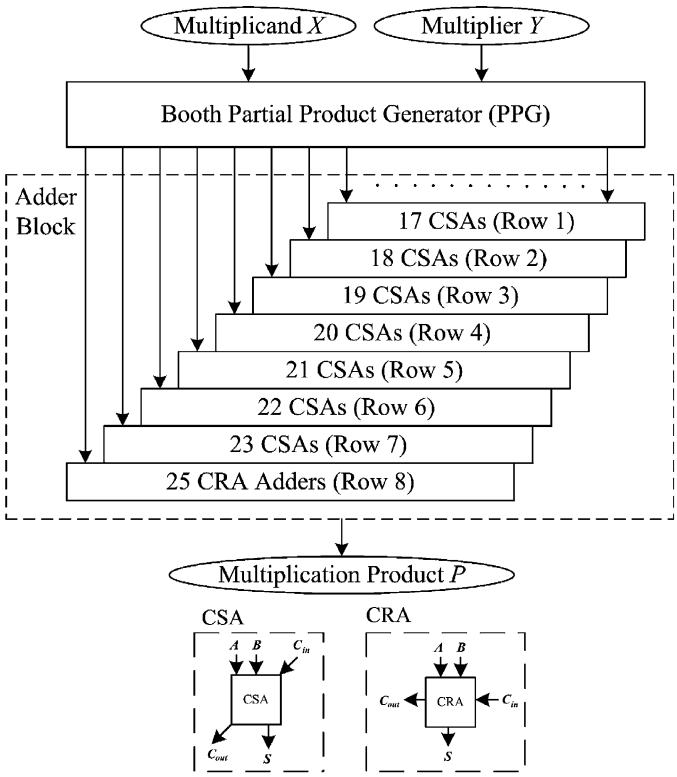

Fig. 1. Block diagram of a 16×16-bit booth general array multiplier.

spurious switching applies to both array-based and tree-based multipliers.

It is well established that the primary power dissipation mechanism of the multiplier is dynamic switching power. In typical designs, there is substantial spurious (redundant) switching in the Adder Block in a multiplier, resulting in wasted power. The spurious switching is largely attributed to the different arrival times of the input signals to the adders in the Adder Block. The spurious switching propagates from the adders in the first row of the Adder Block to the adders in the latter rows where the amount of spurious switching increases. The wasted power due to spurious switching is substantial, typically in the order 40% of the total power of 16×16-bit multipliers, and is large for longer wordlength multipliers, for example ∼60% for 32×32-bit multipliers.

To reduce spurious switching in the Adder Block in a multiplier, reported designs include adders with output C^2MOS latches [13] (for a pipelined multiplier-accumulator), ECDL-based (Enabled/Disable CMOS Differential Logic) adders [14], dynamic adders (DAs) with delayed-evaluation [15], a different array-based structure design such as the Leapfrog multiplier [11], delay matching for the intermediate adder signals [16], delay balancing for the partial products (PPs) [17], dynamic range determination units with flip-flops placed in front of the multiplier [18] and more direct designs that employ latches placed in front of the adders [19]. Although the output C^2MOS latch does reduce the spurious switching by latching the output signal (thereby preventing the spurious switching from propagating to the following stage), substantial spurious switching within the adders remains, in particular where the arrival of the input signals into the adders is poorly synchronized. The ECDL-based adders/DAs, on the other hand, require reset/pre-charge and enable/evaluate operations to appropriately time the turning on/off of the ECDL adders/DAs and these additional switchings defeat the advantages gained. Furthermore, the ECDL-based adders require complementary signals which double the switching activity, and require a larger IC area.

The Leapfrog array-based structure in a multiplier can reduce the switching to some degree. However, substantial spurious switching remains especially if the input signals to the adders are poorly synchronized. The delay matching for the intermediate adder signals by means of delay circuits (delay lines) to synchronize the input to the adders is somewhat impractical for a large ($\geq$ 16 × 16-bit) multiplier design because of the high cost (area and power) of numerous delay circuits. The delay balancing technique for the PPs reduces the power dissipation in the Adder Block but the power dissipation advantage may then be offset by the higher power dissipation in the partial product generator (PPG) and larger IC area. The dynamic determination units with flip-flops placed in front of the multiplier are advantageous in reducing the spurious switching in the PPG and to some extent, in the Adder Block. However, the degree of spurious switching reduction in the latter strongly depends on the input data and the dynamic range determination unit, and the flip-flops incur expensive power overhead. Similarly, the advantage gained from the simplistic design of placing latches in front of the adder is defeated by the cost in hardware and the added power dissipated by the added latches.

In this paper, we describe a low-voltage (1.1 V) micropower (∼18.8 μW/MHz) 16×16-bit 2's complement array multiplier that features low switching (∼657 switchings/multiplication) operation. We achieve the micropower attribute by replacing most of the adders in the Adder Block by our proposed Latch Adders (LAs). In the LA, the novelty is the realization of latches as an integral part of the adder (as opposed to the latch being a separate circuit entity), resulting in small power and hardware overheads. These integrated latches are effectively placed in the front (input) of the adders, and serve to synchronize the inputs to the adder. With the latch function and by means of simple delay circuits, we synchronize the inputs to the adders in the Adder Block in a predetermined chronological sequence, thereby substantially reducing the spurious switching. It is interesting to note that an adder with an integrated latch [13] where the latch is effectively placed at the output of the adder, was previously reported. However, as discussed earlier, this approach serves to pipeline the multiplication operation and the power reduction is small as substantial spurious switching remains.

We analyze the switching activity in 16×16-bit and 32×32-bit multiplier designs and show that the number of switchings (spurious and that for computation) is respectively reduced from ∼5.6 and ∼10 per adder in the Adder Block of conventional designs to ∼2 in our designs. We verify our 16×16-bit multiplier design by computer simulations and on

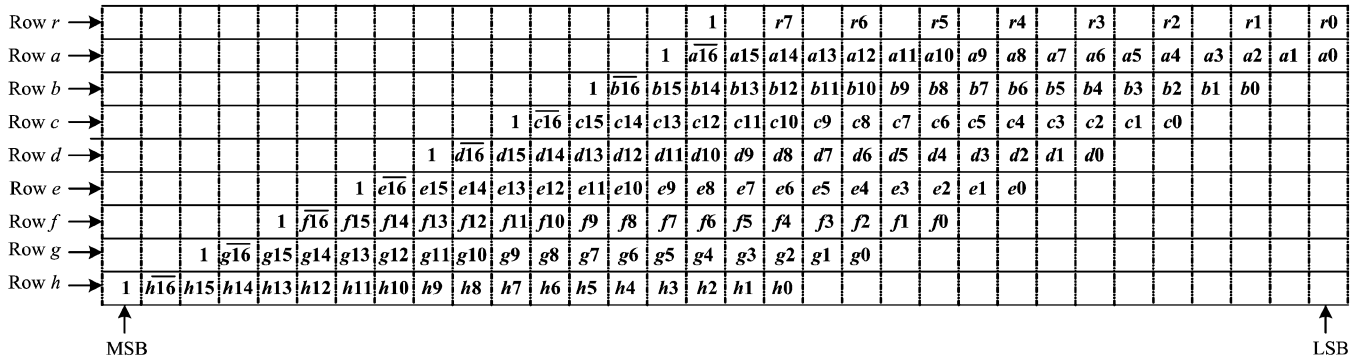

Fig. 2. The partial products in a 2's complement 16×16-bit Booth radix-4 multiplier.

the basis of experimental measurements on prototype ICs and show that our design dissipates ∼32% less power, is ∼20% slower but has ∼20% better energy-delay-product (EDP) than conventional designs. In the case of a 32×32-bit multiplier design, our design dissipates ∼53% less power, is ∼29% slower but has ∼39% better EDP than the conventional general array multiplier. The prototype IC and the conventional array multipliers are realized using a 0.35 μm three metal dual poly CMOS process.

II. A Review of 2's Complement Booth Array Multiplier Architecture

In this section, we will briefly review the architecture of the Booth array multipliers. This review will provide a perspective to our design in Section IV.

Fig. 1 depicts a multiplier comprising two function blocks, namely the PPG and the Adder Block. From the multiplicand X and multiplier Y inputs, the PPG generates the PPs which are subsequently added in the Adder Block to obtain the multiplication product, P. The majority of multipliers employ the modified Booth's algorithm [10] for the PPG. This is because the use of the Booth algorithm results in a small number of PPs and this in turn reduces the number of rows (and hence the number of adders) in the Adder Block. In the case of the 2's complement format, a correction term is usually added so that the hardware required for the sign-bit extensions (that would otherwise incur substantial hardware overheads) is small [20]. Fig. 2 depicts the PPs of a 16×16-bit 2's complement Booth radix-4 multiplier generated by the Booth PPG. Rows a to h contain the PPs and the least significant bit (LSB) and the most significant bit (MSB) are respectively at the extreme right and at the extreme left sides. The PPs in row r correspond to modified Booth encoded carry-in signals.

In a parallel array multiplier, the multiplication process simply involves the summation (by means of full adders) of the PP's row by row in a regular fashion in the Adder Block. Although the regularity of the array structure is changed slightly to accommodate the signed bit in 2's complement format, the majority of the full adders are still placed in a regular fashion. The array structure has the advantage (over a tree-based structure) of simple interconnects between the full adders.

Fig. 1 earlier depicted the block diagram of a 16×16-bit Booth radix-4 array multiplier. The first 7 rows of the Carry Save Adders (CSAs) compress the 9 rows (PPs in Row a to h and in Row r in Fig. 2) to 2 rows of PPs. These final 2 rows are added by the Carry Ripple Adders (CRAs in Row 8) functioning as a carry propagation adder, and the product, P, is obtained.

III. Proposed Latch Adder Design

Full adders are the most rudimentary cells in an array multiplier. The prevalent adder designs for low-voltage operation that provide rail-to-rail output include the T28 [21], T18 [21], T16 [22], N-P DA [23] and Domino DA adders [see Fig. 3(a)–(e)]. Other adder designs with a small transistor count (<15-transistor per adder), for example designs in [22], [24], [25], operate unreliably under low-voltage conditions ($V_{\rm DD} \approx |V_{\rm Tp}| + V_{\rm Tn}$), and are hence unsuitable. The T28 adder is a conventional 28-transistor static CMOS design. The T18 and T16 adders are transmission-gate/pass transistor designs and they comprise 18 transistors and 16 transistors respectively. These full adders (except the DAs) are asserted when their inputs change, and substantial spurious switching results if their inputs are poorly synchronized. The amount of spurious switching increases as the signal propagates through the Adder Block because the input signal to the adders in the latter rows becomes less synchronous. The N-P DA comprises 24 transistors (or 22 transistors if only one p-MOS and one n-MOS weak transistors are used) and is a variation of the NORA CMOS serial adder. The Domino DA comprises 31 transistors (or 29 transistors if only two p-MOS weak transistors are used) and its sum output is a 3-way XOR function.

A simple way to reduce spurious switching is to place separate latches in front of the adder to synchronize the inputs. However, the cost in hardware in terms of IC area (three latches are required per full adder) and in terms of the added power dissipated by these latches is high [19]. To circumvent this cost and yet obtain a latch function at the input to the adder to reduce the spurious switching, we propose to integrate a latch into an adder, termed the Latch Adder (LA). By integrating a latch (that latches all the 3 inputs simultaneously) within an adder instead of being separate and external latches, the overheads are low

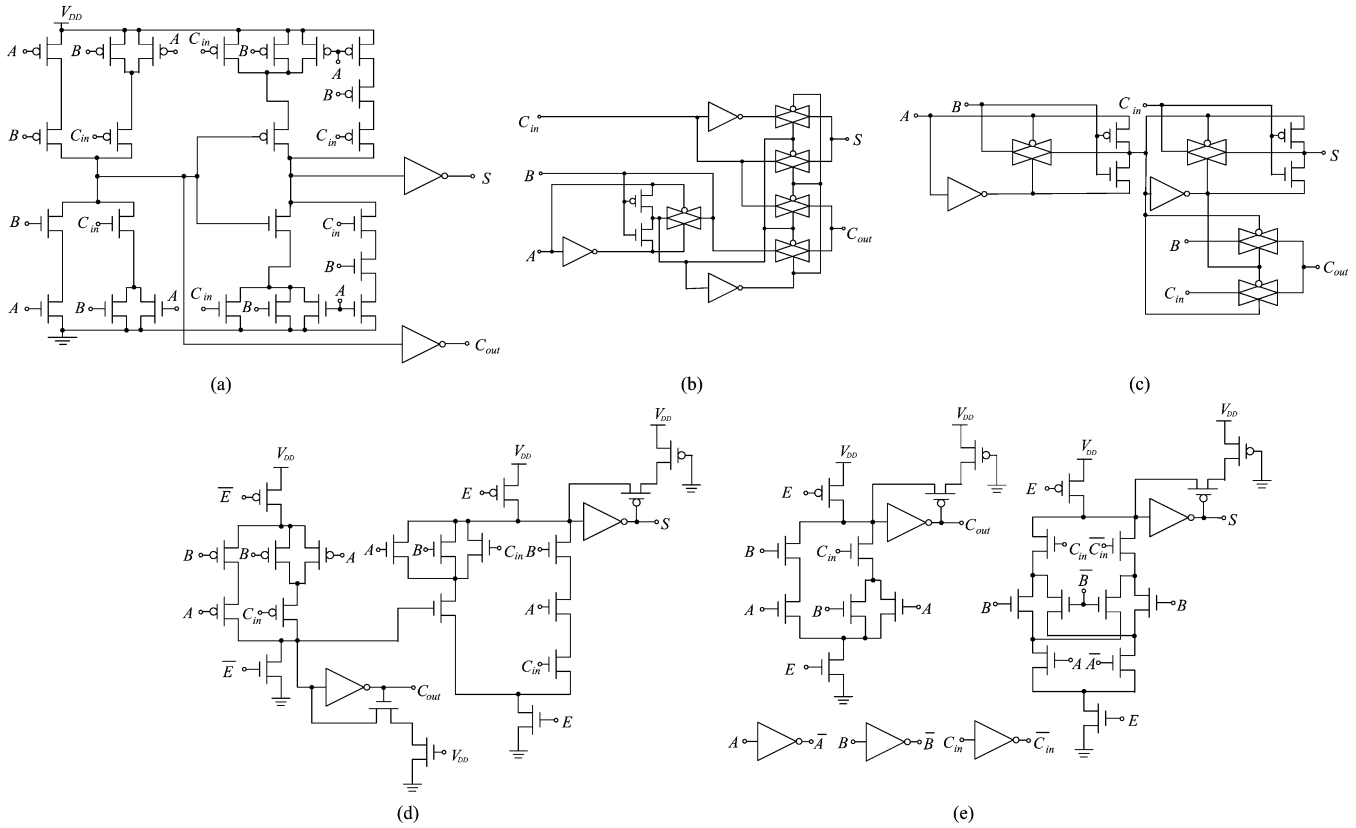

Fig. 3. Conventional full adders that provide rail-to-rail signal swing at low-voltage operation. (a) T28 Adder. (b) T18 Adder. (c) T16 Adder. (d) N-P DA. (e) Domino DA.

(see Sections IV and V later). We depict our proposed LA in Fig. 4, a modification of our earlier LA designs [26], [27].

The latch function within the LA is controlled by means of the control signals, E_i and $\overline{E_i}$, and serves to synchronize the 3 input signals to the LA. The 3 inputs are A, B, and $C_{\rm in}$, and the output sum is denoted S and the Carry-out, $C_{\rm out}$. In Fig. 4, when $E_i = \text{`1'}(\overline{E_i} = \text{`0'})$ or asserted, the LA functions as a full-adder. When $E_i = \text{`0'}(\overline{E_i} = \text{`1'})$ or negated, the LA will hold its output signals by means of weak (small W/L ratio) feedback p-MOS transistors ($P1$ to $P4$), and the output of the adder is hence latched. Note that although the LA design depicted in Fig. 4 is a semi-static CMOS design, its operation is robust. We will now describe why this is the case by considering the following two scenarios. First, assume that S is initially '1'. If $E_i = \text{`1'}$, there is no ambiguity. For the same initial condition, if $E_i = \text{`0'}$, $\bar{S}$ is at a high impedance state, hence an undesirable condition. This is because charge leaking into $\bar{S}$ may result in an undesirable change in state. This is, however, not an issue because for $E_i = \text{`0'}$, the output is not used. Put simply, for $E_i = \text{`0'}$, the output is inconsequential because the LA is in idle state. Second, assume that S is initially '0'. If $E_i = \text{`1'}$, there is again no ambiguity. For the same initial condition, if $E_i = \text{`0'}$, $\bar{S}$ is a well-defined '1' due to feedback inverter. The same scenarios apply to signal $C_{\rm out}$. In short, the operation of our LA is robust.

To retain the low power advantage in our design, we design the weak feedback inverters by cascading $P1$ and $P2$ to $P3$ and $P4$ respectively. In this manner, these transistors present a low capacitive loading. This is as opposed to the conventional method where only $P3$ and $P4$ (both with much longer L) are used, thereby presenting a larger capacitive load. To ensure that the short-circuit current is negligible, we choose a process where $|V_{\rm Tp}| + V_{\rm Tn} = 1.08\ {\rm V} \approx V_{\rm DD} = 1.1\ {\rm V}$. As indicated in Fig. 4, we size the transistors (other than $P1$-$P4$) in our LA close to the minimum values.

It would be of interest to note that if the supply voltage is relatively low ($V_{\rm DD} < |V_{\rm Tp}| + V_{\rm Tn}$), there is no power dissipation due to short-circuit current, and the dynamic CMOS approach can be adopted (without weak feedback p-MOS transistors, $P1$ to $P4$). If the supply voltage is relatively high ($V_{\rm DD} > |V_{\rm Tp}| + V_{\rm Tn}$), for the robustness, for reducing the short-circuit current and for enhancing its logic state, weak n-MOS transistors can be included (fully static CMOS approach) at the expense of relatively slower speed, larger area and higher switching power dissipation (compared to dynamic CMOS approach). The semi-static CMOS approach provides a good compromise between the dynamic CMOS and fully static CMOS approaches. Compared to the former approach, the semi-static CMOS approach results in some short-circuit current reduction. Compared to the latter approach, the semi-static CMOS approach results in a

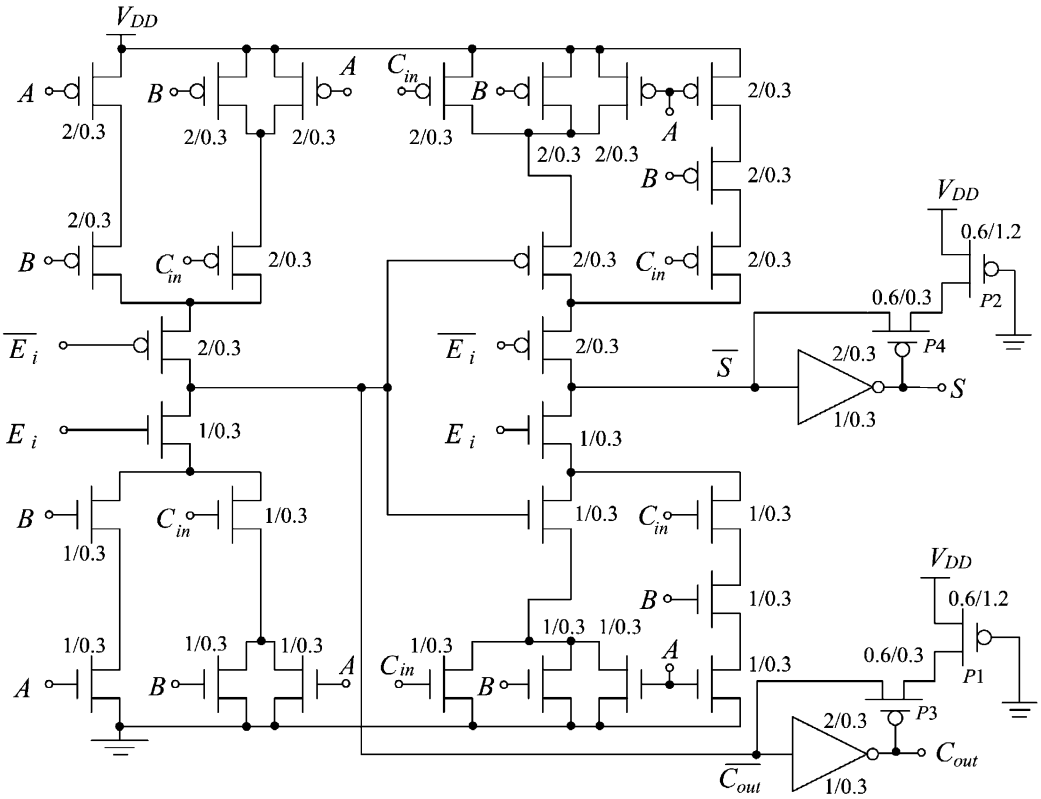

Fig. 4. Circuit schematic of the latch adder.

lower switching power dissipation and higher speed due to relatively smaller output loads.

IV. Proposed Adder Block for Array Multiplier Design

Fig. 5 depicts the block diagram of the proposed 16×16-bit array multiplier embodying the Booth PPG, delay circuits (D_1–D_7) and Adder Block. The Adder Block comprises 7 rows (Row 1–Row 7) of LAs and a final row of CRAs that serves a carry propagation adder.

The operation of the multiplier is as follows. When a multiplication is initiated with the Multiplicand X and Multiplier Y inputs, the Start signal asserts D_1. After a predetermined delay in D_1 that is at least equal to the duration required of the PPG to generate the PPs, E_1 and $\overline{E_1}$, will assert the latches in the LAs of Row 1 and assert D_2. As the inputs to the adders in the LAs in Row 1 are synchronized, there is little, if any, spurious switching in this row. In the remaining rows of the Adder Block, there is no switching as the LAs there remain negated. Subsequently, after a predetermined delay in D_2 that is at least equal to the duration of the delay in the adders in Row 1, E_2 and $\overline{E_2}$, will assert the latches in the LAs in Row 2 and assert D_3. Similarly, as the inputs to the adders in the LAs in Row 2 are synchronized, there is little, if any, spurious switching in this row. Similarly, there is no switching in the remaining rows as the LAs there remain negated. The process repeats until Row 7, and the spurious switching in Rows 1–7 of the Adder Block is virtually eliminated. The last row of CRAs computes the final multiplication product P.

The delay circuit is usually implemented using an inverter chain with appropriate W/L transistor sizing. We do not consider increasing L (thereby decreasing the W/L ratio) as a means to increase the delay because this would compromise the load capacitance. Instead, we design the inverter depicted in Fig. 6 where transistors $P5$ and $N5$ are used to adjust the equivalent W/L ratio of the $p((W/L)_{\mathrm{eq},p})$ and $n((W/L)_{\mathrm{eq},n})$-type transistors of the inverter, hence the amount of delay. With this implementation, the input gate capacitance is determined by transistors, $P6$ and $N6$, both having a small diffusion area. For example, based on post-layout simulations, the total node capacitance at the input of our delay circuit and at the conventional delay circuit (simple inverter) is 11.5 fF and 24.9 fF respectively, for the same delay of 5 ns. The energy required for the preceding input driver (a standard inverter) to drive our delay circuit and the conventional delay circuit is 12.5 fJ and 30.8 fJ respectively @1.1 V. This translates to ∼59% less energy if our delay circuit is adopted. The output of the delay circuit is buffered by two standard inverters to drive the control signals E_i and $\overline{E_i}$, depicted in Fig. 5.

To delineate the efficacy of our approach to reduce spurious switching, we depict in Fig. 7, from simulations with 10 000 random inputs and based on the circuit arrangement depicted in Fig. 8, the detailed breakdown of the power dissipation of the different blocks of different 16×16-bit and 32×32-bit array

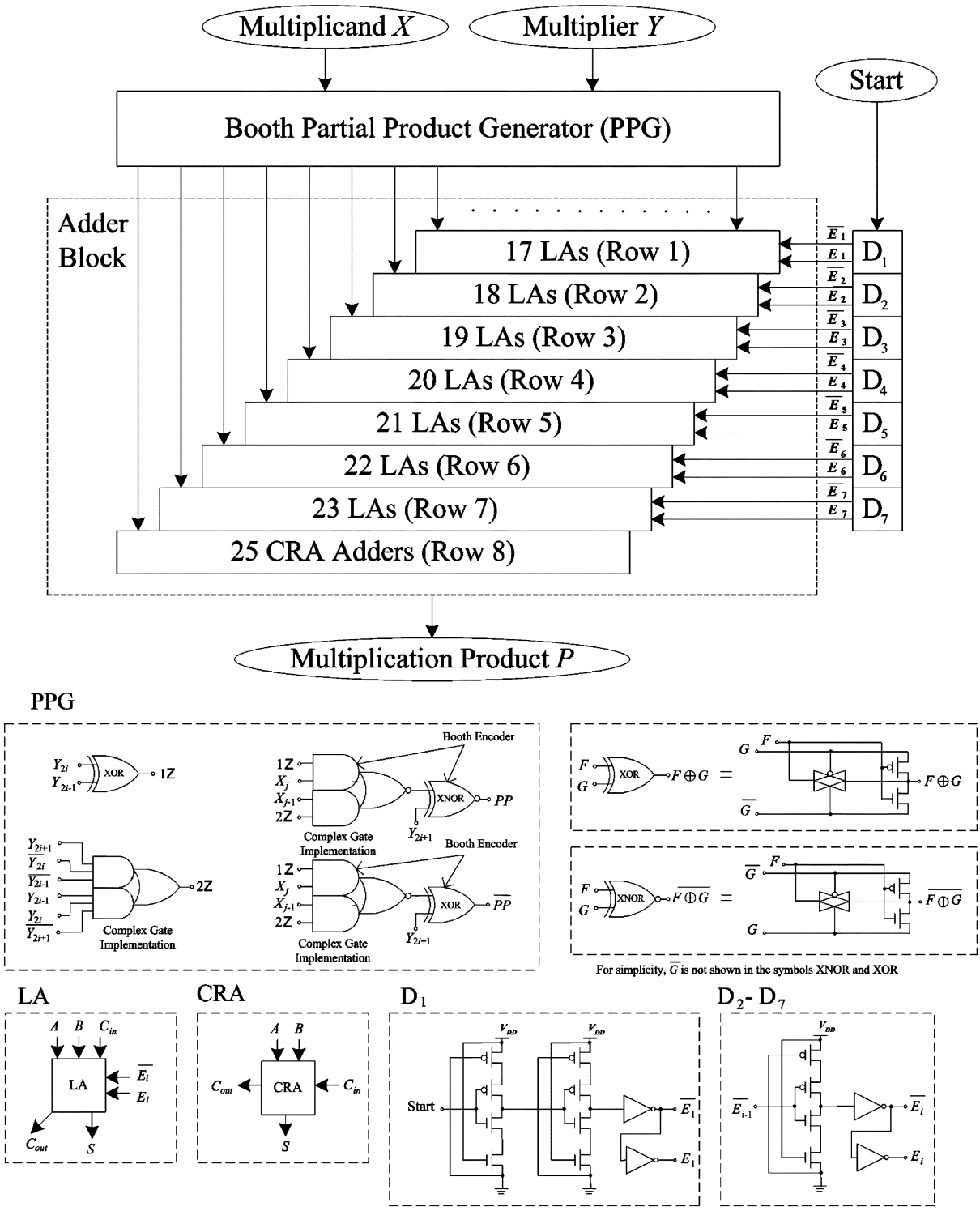

Fig. 5. Block diagram of the proposed 16×16 bit Booth array multiplier (SB-Proposed16).

multipliers operating at 1 MHz @1.1 V. The different blocks include the Booth PPG, Adder Block and Input Drivers (buffers for inputs). For the Dynamic and our proposed multipliers, the 'Overhead' block refers to the power dissipated by the delay circuits to control the Domino DAs[1] and LAs, respectively. The T28 adders [21] are used in the Leapfrog and General designs and are used as the CRA in our design. Note that the total power dissipation of the multipliers is based on the post-layout simulations but the power breakdown distribution is estimated from pre-layout simulations.

In Fig. 7, we consider two different PPGs in the General array multipliers. The first PPG (embodying 12-transitor Booth en-

[1]The Domino DA embodied in the SB-Dynamic16 comprises 29 transistors and is ∼2% higher power than the Domino DA depicted in Fig. 3(e).

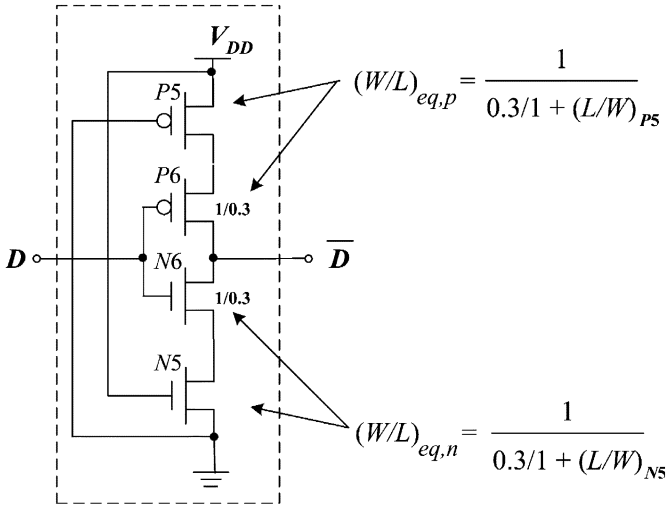

Fig. 6. Circuit schematic of the delay circuit.

coders, see PPG in Fig. 5) is the standard Booth PPG and we denote this standard Booth PPG as 'SB' PGG. The second PPG (embodying 18-transistor Booth encoders [17]) is used to balance (equalize) the arrival times of PPs to the Adder Block, resulting in potentially reduced spurious switching in the Adder Block and we denote this balanced Booth PPG as the 'BB' PPG.

From Fig. 7, we note that although the BB-General16 embodying the BB PPG reduces the power dissipation in the Adder Block (compared to the SB-General16 employing the SB PPG from 65% (18.1 μW) to 52% (14.4 μW)), the overall power dissipation of the two multipliers is approximately the same. This is because the reduced power in the Adder Block embodied in the BB-General16 is offset by the higher power dissipation in the BB PPG and the input drivers. Furthermore, the BB PPG is more sensitive to W/L ratio sizing, parasitic effect, floorplan in layout, and voltage violations. Consequently, design considerations to minimize these undesirable susceptible effects in the BB PPG are critical—the BB PPG may otherwise generate PPs with very different times, much less synchronous than expected. These different times consequently results in larger amount of spurious switching in the Adder Block, hence higher power dissipation in the multiplier. Furthermore, the IC area required for the BB PPG is larger (compared to the SB PPG). In view of the potentially higher power dissipation, undesirable added design considerations and larger IC area required of the BB PPG, we do not consider the BB PPG and instead consider only the SB PPG and other reported multiplier designs (except BB-General16).

From Fig. 7, we note that for the reported SB-Dynamic [15], SB-Leapfrog [11], SB-General [10], and BB-General [10], [17] 16×16-bit multipliers, an average of 59% (16.1 μW) of the total power is dissipated in the Adder Block. Put simply, the Adder Block dissipates the largest power in typical 16×16-bit multipliers. By means of our approach to significantly reduce the spurious switching and with little overhead, the Adder Block now dissipates 39% (7.2 μW) of the total power. In other words, our design on average dissipates $\sim$32% less power than the reported designs compared herein, and $\sim$30% less power than the lowest power reported design, the SB-Leapfrog multiplier.

To quantify the degree of reduced spurious switching, we depict in Fig. 9 the number of switchings per adder in the different rows of the Adder Block based on information obtained from pre-layout simulation. The average number of switchings per adder for the SB-Leapfrog16, SB-General16, and BB-General16 multipliers is 5.3, 6, and 5.3 respectively, and the amount of switching increases as the row number increases. This is not unexpected as the inputs to the adders become increasingly less synchronous in the latter rows. In the case of the multiplier with Domino DAs (termed SB-Dynamic16), the number of switchings per adder remains largely unchanged, an average of 5.6 switchings per adder. This is because the Domino DAs always first pre-charge and then evaluate when the inputs are ready. The high number switching in the Domino DAs is due to its dynamic operation (constant precharge and evaluation). By comparison, the number of switchings per adder in our design is substantially lesser at two switchings per adder, leading to the much desired micropower attribute. The average 3 switchings per adder (instead of 2) in the last row of the SB-Proposed16 and SB-Proposed32 multipliers is largely due to the carry ripple effect of the multiplication product in the CRAs in the last row.

The efficacy of our approach is more pronounced in longer wordlength multipliers, for example a 32×32-bit multiplier. This is because there is a larger number of rows and because the input signals to the adders in the latter rows are even less synchronous. We depict in Fig. 9 the number of switchings per adder of a SB-General 32×32-bit array multiplier. On average, there are $\sim$10 switchings per adder @1 MHz. By means of our approach, the number of switchings per adder remains approximately the same as our 16×16-bit design -2.1 switchings per adder. We show this in Fig. 7 where in power terms @1 MHz, 1.1 V, from Fig. 7, the Adder Block dissipates 74% (120.5 μW) and 36% (27.6 μW) of the total power of the SB-General32 multiplier and our multiplier design respectively. In other words, our design dissipates $\sim$53% less power than the SB-General32 multiplier.

Although the drawback of our approach is the increase in the delay, the EDP of our design is the lowest of the designs compared. We will present this in the next section.

V. Simulation and Measurement Results

In view of the micropower attribute of our multiplier design due to the chronological timing of the integrated latches in the LA, we will now compare the LA against reported full adders, namely the T28, T18, T16, N-P DA and Domino DA (refer to Fig. 3), and the T28, T18, and T16 with separate low power semi-static noninverting C^2MOS latches (with two series weak p-MOS transistors implementation). In all designs, the transistors are sized close to the minimum value, specifically (2 μm/0.3 μm) and (1 μm/0.3 μm) for p-and n-MOS, respectively (except for the weak n-and p-MOS transistors). At the outset, we remark that all designs are based on the same 0.35 μm CMOS fabrication process. The low transistor-count pass-logic adders, such as [22], [24], [25], that do not operate reliably at 1.1 V are not considered.

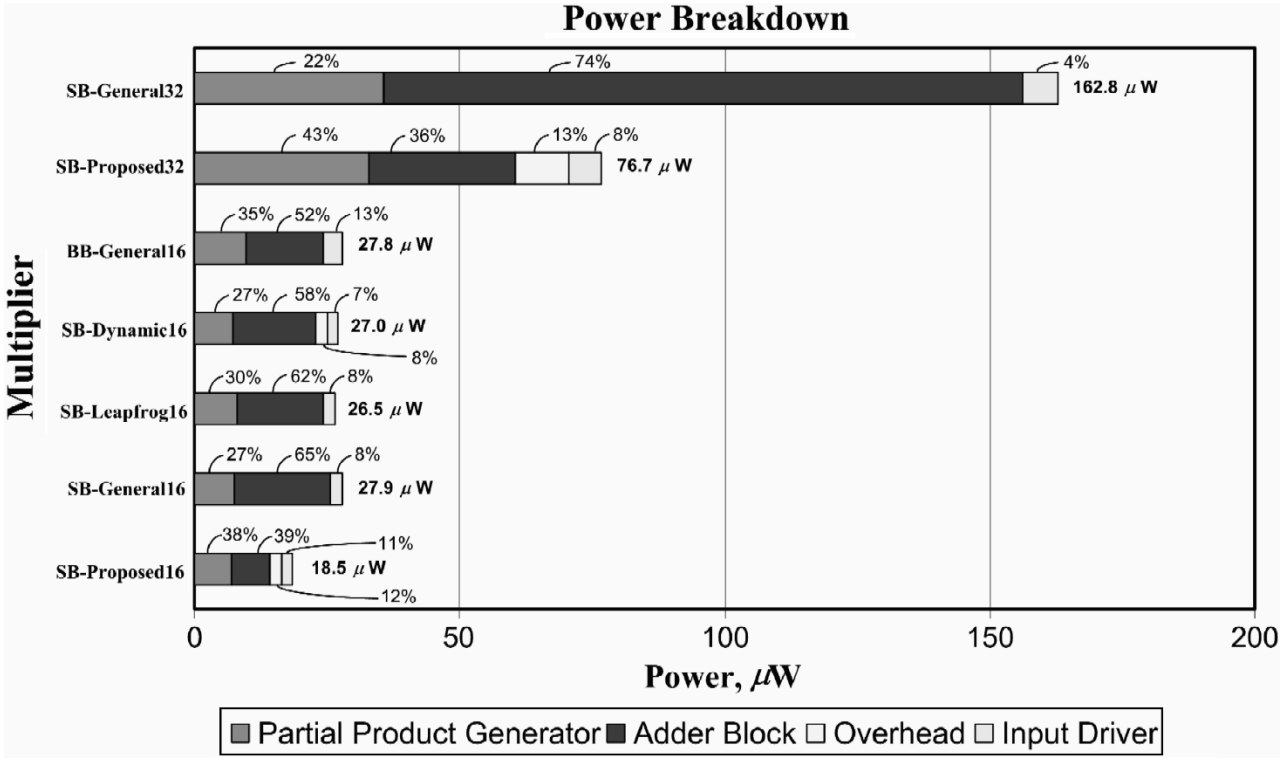

Fig. 7. Breakdown of power (in % and μW) of different array multipliers based on simulations.

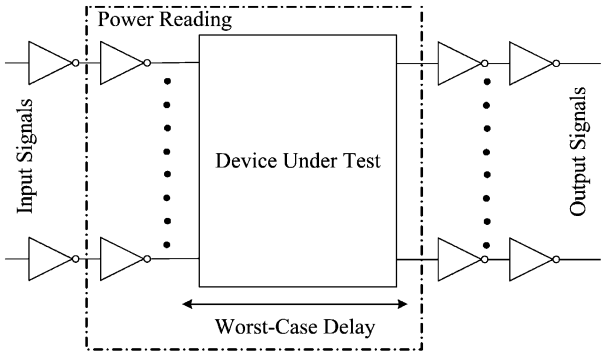

Fig. 8. Simulation arrangement.

On the basis of 500 random input signals and on simulations, we summarize the power dissipation, delay, EDP and IC area of the different adders in Table I. The EDP is calculated by the product of the average energy per operation (power per MHz) and the delay of the operation. From Table I, we note that among the conventional adders (T28, T18, T16) and the LA, the LA dissipates the highest power, is the slowest and occupies the largest IC area. This is not unexpected due to the added integrated latch function. On the other hand, among all adders compared, the Domino DA is the fastest adder but dissipates the highest power due to its dynamic operation. Despite N-P DA featuring 7 less transistors than Domino DA, the N-P DA features high power dissipation, comparable to the Domino DA. This is because of its dynamic operations, additional control line $\bar{E}$ and the p-MOS tree having a larger capacitance. The low mobility of the p-MOS transistor (lower than the n-MOS transistor) makes the p-MOS tree (and its associated n-MOS weak transistor for charge sharing prevention) less attractive in the N-P DA. As a result, the N-P DA features a relatively poorer speed performance compared to the Domino DA.

When compared against the T28, T18, and T16 adders with separate latches, the LA features the lowest power dissipation, is the fastest and occupies the smallest area. As described previously, we attribute these desirable parameters to the integrated latch in the LA.

We realize two 16×16-bit multiplier designs, our SB-Proposed16 and the SB-General16, in monolithic form. The microphotographs of these designs are depicted in Fig. 10. On the basis of measurements on prototype ICs and on simulations, we summarize the parameters of the different multipliers in Table II. We note that the measurement results agree well with the simulations.

Of the 16×16-bit designs in Table II, our design features the lowest power dissipation, one of the slowest designs but the lowest EDP. In some applications, such as that for the intended hearing instrument application where the embodied DSP is clocked at low speed (<5 MHz), the delay is inconsequential. The speed of our design can be increased by adopting a more aggressive timing for the delay controlled by the delay elements D_1–D_7 in Fig. 5. However, this may compromise the degree of spurious switching reduction, and hence the power dissipation. We can also increase the speed by replacing the CRAs in the final row of the adder to a faster adder such as a carry look-ahead

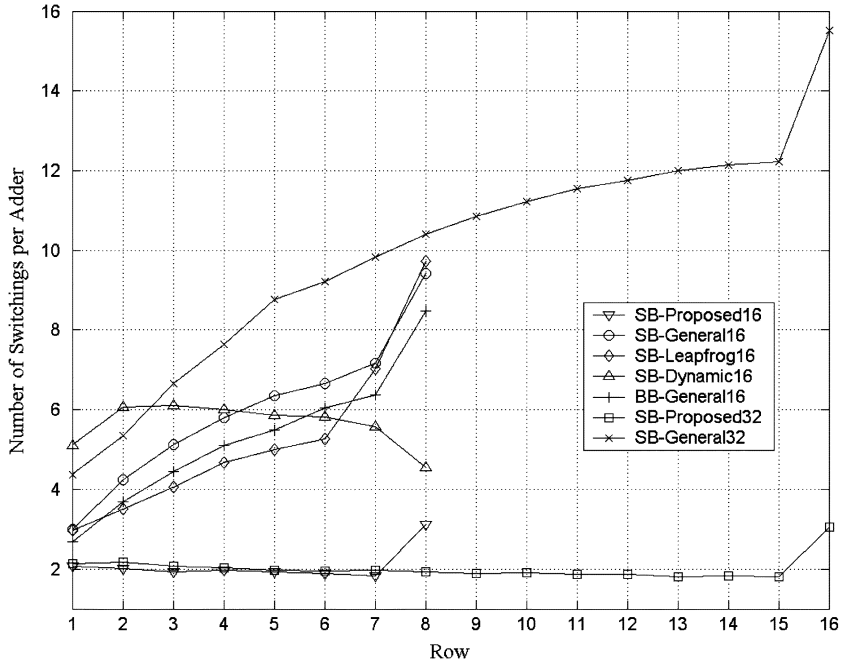

Fig. 9. Switching analysis in the adder block of various multipliers.

TABLE I
POWER, DELAY, ENERGY-DELAY-PRODUCT (EDP) AND IC AREA OF VARIOUS ADDERS @$V_{DD} = 1.1$ V, 1 MHZ BASED ON POST-LAYOUT SIMULATIONS

Adder	Power (10^{-8} W)	Delay (ns)		EDP (10^{-23} J.s)	Core Area (μm^2)
		C_{out}	S		
T28	6.0	3.4	4.8	28.8	389
L_T28	15.4	5.6	7.3	112.4	1180
T18	7.3	4.1	4.3	31.4	374
L_T18	15.8	8.3	8.3	131.1	970
T16	7.2	5.0	5.9	42.5	387
L_16	15.8	9.4	11.0	173.8	1000
N-P DA	11.7	7.0	8.3	97.1	486
Domino DA	11.8	1.9	2.7	31.9	660
LA	10.1	4.4	7.0	70.7	501

L_XXX denotes an adder with latches where the latches and adder are separate circuits

adder but at the slight cost of increased power dissipation. For even higher speed operation, V_{DD} would need to be increased, for example from 1.1 V to 3.3 V—in this case, for the same degree of spurious switching reduction, the delay of our design reduces from 131 ns (7.6 MHz) to 26 ns (38 MHz) and the power dissipation remains low at $\sim$273 μW/MHz. Note that at 3.3 V operation, the short-circuit current is no longer negligible, dissipating $\sim$30% of the total power. For the other multipliers, the short circuit current is similarly not negligible. To reduce the short circuit power dissipation, the adders and delay lines would need to be resized.

For the 32×32-bit multipliers, we had earlier depicted the comparison in Fig. 7 and made comments earlier therein.

In terms of IC area, both our 16×16-bit and 32×32-bit designs are slightly larger than the 16×16-bit SB-General and SB-Leapfrog multipliers, and the 32×32-bit SB-General multiplier. This is due to the overheads of the LA and the delay circuits. However, our design is smaller than the 16×16-bit SB-Dynamic multiplier and is comparable to the 16×16-bit BB-General multiplier.

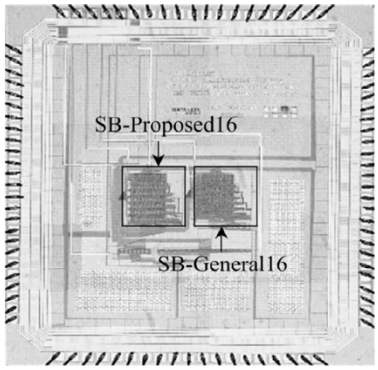

Fig. 10. Microphotograph of the SB-Proposed16 and SB-General16 16×16-bit 2's Complement Booth Array Multipliers (0.35 μm CMOS process).

In summary, our multiplier design features very low power dissipation owing to the substantially reduced spurious switching, and is suitable for power critical applications including hearing instruments.

VI. CONCLUSION

We have proposed a low-voltage micropower multiplier with substantially reduced spurious switching. This is obtained by means of our proposed integrated latch in Adders, termed LAs, placed in the Adder Block of the multiplier. We have analyzed the switching activity in the Adder Block and have shown that by means of our approach, the amount of switching in our design is $\sim$38% and $\sim$21% that of reported 16×16-bit and 32×32-bit

TABLE II
AVERAGE NUMBER OF SWITCHINGS, POWER, DELAY, AREA, AND ENERGY-DELAY-PRODUCT (EDP) OF VARIOUS ARRAY MULTIPLIERS @$V_{DD} = 1.1$ V, 1 MHz BASED ON POST-LAYOUT SIMULATIONS AND MEASUREMENTS ON PROTOTYPE ICS

Array Multiplier	Simulations based on Post-Layouts					Measurements based on prototype ICs		
	Average Switchings	Power (μW)	Delay (ns)	Area (mm^2)	EDP (a J.s)	Power (μW)	Delay (ns)	EDP (a J.s)
SB-General16	1412	27.9	104	0.18	2.9	28.3	122	3.5
SB-Leapfrog16	1320	26.5	103	0.17	2.7	–	–	–
SB-Dynamic16	1375	27.0	134	0.24	3.6	–	–	–
BB-General16	1291	27.8	96	0.20	2.7	–	–	–
SB-Proposed16	657	18.5	131	0.20	2.4	18.8	145	2.7
SB-General32	8350	162.8	201	0.45	32.7	–	–	–
SB-Proposed32	2752	76.7	260	0.51	19.9	–	–	–

designs. This translated to a $\sim$32% and $\sim$53% power reduction respectively. Although the slight penalty is the increased delay, our design still featured the lowest EDP. Our design is well suited for low-voltage power-critical low speed applications including hearing instruments.

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