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An Untrimmed CMOS Amplifier with High CMRR and Low Offset for Sensor Applications

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Abstract—This paper presents a new CMOS amplifier with high common-mode rejection ratio (CMRR) and low offset, dedicated to integrated sensors, using total continuous-time design technique but without the need of trimming. This is based on cascading two high-gain differential stages to form a composite front-end gain stage for enhancing CMRR as well as reducing systematic errors, and incorporating an averaging layout technique to reduce the random mismatch errors. Powered by a total 3.3V supply, measurements on 15 samples have shown that the mean and standard deviation of the input-referred offset are 50.4 μ V and 0.678mV respectively. The proposed amplifier has also achieved CMRR greater than 110dB (0 - 150Hz), offset drift less than 0.8 μ V/ $^{\circ}$ C for temperature ranging from -55° C to $+125^{\circ}$ C, input-referred noise less than 17.47 $nV/\sqrt{Hz}$ at 1kHz and active area of 0.117 mm² in a 0.6 μ m CMOS technology.

Index Terms – CMOS amplifier, precision amplifier, instrumentation, CMRR, offset, offset drift, integrated sensors

I. INTRODUCTION

Amplifiers play an important role in many sensor circuit applications such as sensing interface, low-level signal conditioning circuit, sensor reference circuit and so forth. For instance, the autonulling bridge for gas sensors and chemical sensors or the well-known Wheatstone bridge for pressure sensors etc. often require amplifiers having intrinsically high CMRR, low offset, low offset drift and low noise for floating differential sensing function. There are several approaches to deal with the design challenges. Trimming of amplifier's components is one of the common methods. It is straightforward but it increases the testing cost. Another drawback is that the trimmed circuits may be valid for certain temperature range or constrained conditions due to the added sensitivity of the trimming network. Alternatively, the amplifiers in sensors can be designed using auto-zeroing technique [1], correlated double sampling technique [2], chopper stabilization technique [3]-[4] or baseline subtraction technique [5] so as to increase CMRR and/or to reduce both the offset and low frequency flicker noise in CMOS sensor circuits. However, the key disadvantages of these techniques can be observed as (i) the clock circuit coupling unavoidable interference into sensitive analog circuitries or into the amplifier itself via the common substrate in silicon and the supply line, adding design concern of power supply rejection ratio (PSRR), (ii) the

generation of residual nonlinear switch errors arising from mismatch or inadequate compensation of switches and (iii) the use of high-order continuous-time filter for rejection of unwanted spectral components. All of these techniques increase the silicon overhead indirectly. As a result, turning to the amplifier design using continuous-time technique for low-cost solution as one of the focuses, the circuit architecture and device matching are considered as two critical issues because they dictate the instrumentation-based performance in terms of CMRR and offset parameters. One representative example is the use of analytical yield modeling approach [6] to achieve the primary goals. Unfortunately, this design methodology demands substantial resources in device characterization and measurements so as to obtain optimized sizing for transistors. The recent reported circuit architecture [8] is also complicated in the input stage design. Therefore, this paper presents the design of a compact and total continuous-time mode amplifier to meet the required instrumentation performance in an economical way.

II. PROPOSED AMPLIFIER

Figure 1 shows the simplified schematic of the precision amplifier. The composite input stage concept is applied to design the front-end input stage instead of the input stages using either operational transconductance amplifier (OTA) structures [6]-[7] or folded-cascode structure with dedicated biasing technique [8]. Herewith, the proposed amplifier comprises three gain stages. The first stage (formed by transistors M1-M4 and M9) and the second stage (formed by transistors M5-M8 and M10) are standard differential amplifier stages whereas the third stage (formed by transistors M11-M12) is a class-A output stage. The key front-end structure is that of the outputs of the first differential stage being clamped directly by the second gain stage to form a single composite gain stage. This ensures that the dc operating point at the gates of the transistors M5 and M6 are approximately at the same level. Therefore, the node voltages V_A and V_B of the first stage will be forced to follow each other by the second differential gain stage. Hence, the composite gain stage provides intrinsic tracking mechanism to reduce the systematic offset, leading to the improvement of stability in context of environmental variations due to process, temperature and supply. To enhance the device matching as a means to reduce the random offset, the layout technique for increasing randomness in placement of critical matched devices is employed and discussed in the subsection D of section III. This ensures that the geometrical mismatch does not contribute significantly to

the offset, particularly offset drift performance with low temperature range [7].

Figure 1. Simplified Schematic Diagram of Proposed Amplifier

It is important to note that the node A in Figure 1 exhibits low impedance, but high impedance for the node B. When the differential-to-single-ended active load (formed by transistors M3-M4) in stage one is cascaded with second stage, several key advantages are obtained as follows: (i) the dc biasing point at node B is defined without using the common-mode feedback circuit whereas the high open-loop gain in the clamping circuit suppresses the systematic offset error effectively despite of input-referred offset error from the clamping circuit, (ii) the residue common-mode signal arising from the first differential stage will be strongly rejected by the second differential gain stage to increase the CMRR significantly and (iii) the balanced structures contributed by the first and second differential stages ensure the common-mode offsets contributed by transistor junction leakage currents can be cancelled even at high temperature range [7].

For frequency compensation, the Nested-Miller compensation technique was employed, as shown in the arrangement of two compensation capacitors C_{C1} and C_{C2} . The compensation resistor R_{C1} is added to improve the phase margin of the amplifier. The transistor M13 is added to improve the large-signal slew-rate performance [9] in a class-A output stage topology.

III. DESIGN CONSIDERATIONS

A. Low-Offset Design

Due to imperfect fabrication together with non-ideal design parameters, circuit offsets are unavoidable. Therefore, the input-referred offset voltage dominated by the first stage of the precision amplifier in Figure 1, can be obtained [10] as

$$V_{OS1} = V_{t1} - V_{t2} + \frac{|V_{ovp}|}{2} \left[\frac{V_{t3} - V_{t4}}{V_{ovN}} + \frac{(W/L)_3 - (W/L)_4}{(W/L)_3 + (W/L)_4} - \frac{(W/L)_1 - (W/L)_2}{(W/L)_1 + (W/L)_2} \right] \quad (1)$$

where V_{ti} is the threshold voltage of transistor M_i in Figure 1 with subscript number defined by i , V_{ovp} denotes the gate-overdrive biasing for p-channel differential pair, and V_{ovN} denotes the gate-overdrive biasing for n-channel

active load. Refer to (1), the offset can be minimized by choosing large size for the matching transistor pairs (M1-M2), small gate-overdrive biasing voltage for the differential input pairs (M1-M2), and large gate-overdrive biasing voltage for the active loads (M3-M4). It is the same treatment for the second gain stage. Apart from circuit design, the random offset improvement relies on the averaging layout technique in this untrimmed, unclocked continuous-time method.

B. Common Mode Rejection Ratio

CMRR provides a good measure on assessing how well the matching degree among the critical devices or components in the amplifier design. It can be classified as systematic CMRR and random CMRR. The systematic CMRR relates to the circuit topology, the circuit design with devices having finite transconductance or insufficient large output resistance, whereas the random CMRR originates from the random mismatch effect of the supposedly matched device pairs. A standard differential amplifier would typically display 60-80dB in overall CMRR performance. It is because the typical mismatching factor is on the order of 0.1%. In order to achieve CMRR greater than 100dB, the circuit architecture is modified to a cascade differential structure as the front-end amplifier stage in conjunction with the averaging layout technique. The systematic CMRR for the proposed precision amplifier can be analyzed as

$$CMRR \approx \frac{8g_{m1}(r_{o2}/r_{o4})g_{m3}r_{rail}9g_{m5}r_{o5}g_{m7}r_{tail}10}{1 + \frac{r_{o4}}{r_{o2} + r_{o4}}} \quad (2)$$

where the symbols have their usual definitions with reference to the relevant devices in Figure 1. From (2), it can be seen that the total systematic CMRR for the precision amplifier is enhanced significantly due to the number of product terms $g_{mir}r_{oj}$, which are defined by the device transconductance and the output resistance. For reducing the impact of the mismatching factor that would dominate the overall CMRR in the design of precision amplifier, the averaging layout using the common centroid in centroid methodology is applied to enhance matching accuracy in comparison to the standard well-known common-centroid technique at the expense of increasing layout area.

C. Noise Optimization

The noise sources of the CMOS operational amplifier originate from flicker noise and thermal noise components. The flicker noise component is usually larger than the thermal noise component for typical frequency below 1kHz under typical bias conditions and device geometries [10]. The noise contributions are usually dominated by the first gain stage. Noise analysis of the first PMOS differential stage of precision amplifier in Figure 1 gives

$$\frac{v_{eq}^2}{\Delta f} \approx \frac{2K_{Fdp}}{C_{OX}W_{dp}f} \left[\frac{1}{L_{dp}} + \left(\frac{K_{Fmir}\mu_n}{K_{Fdp}\mu_p} \right) \times \frac{L_{dp}}{L_{mir}^2} \right] \quad (3)$$

where the symbols have their usual meanings, and the subscript n represents n-channel device, subscript p

represents p-channel device, subscript dp represents differential pair and subscript mir represents current mirror. Refer to (3), it can also be observed that the larger the values of L_{mir} and W_{dp} , the smaller the $1/f$ noise is. By differentiating (3) with respect to L_{dp} and setting the derivative to zero, the value of L_{dp} yielding minimum input-referred voltage [11] is

$$L_{dp_opt} = \frac{L_{mir}}{\sqrt{\frac{K_{Fmir}\mu_n}{K_{Fdp}\mu_p}}} \quad (4)$$

Therefore, by choosing the optimum value for the channel length of the differential input pair and choosing larger values for L_{mir} and W_{dp} , the input-referred $1/f$ noise will be minimized.

D. Layout Technique

In order to achieve high CMRR, low offset amplifier, the random mismatch effect is the most critical non-ideal effect in layout consideration. It becomes the dominant effect to the impact of the circuit performance parameters as stated above if the layout is not considered critically from the perspectives in randomness, symmetry, matching characteristics and topological placement of devices. In this layout work, the unit transistors are used rather than the merged transistors for better matching characteristics. The large transistors are divided into a number of unit transistors. All the unit transistors are placed in the same orientation with common centroid pattern. All the matched transistor pairs are placed in the same well for better matching environment. For the proposed precision amplifier, the common-centroid in a quad technique is employed [12]. Figure 2 shows the placement for two large matched transistors being split into sixteen unit devices. Two common-centroid units named sub-group A and sub-group B are established for the formation of another common-centroid pattern. This type of common-centroid in common-centroid technique will be advantageous in minimizing the mismatching error between the transistors and increasing the randomness in topological placement. Hence, the mismatch due to uneven gradients that exists in the fabrication process for the precision amplifier can be greatly reduced.

Figure 2. Layout of Two Identical Transistors using Cross-Coupled Common Centroid in Centroid Technique

IV. RESULTS AND DISCUSSIONS

The proposed amplifier was implemented using a standard $0.6\mu\text{m}$ N-well CMOS process. The overall measured performance at typical condition ($\pm 1.65\text{V}$, 25°C) is summarized in Table I. It can be seen that the DC gain of the precision amplifier under loaded condition is no less than 114dB. This high open-loop gain is essential for minimizing gain error in feedback. The measured power consumption is 0.76mW at a total of 3.3V supply. The microphotograph is shown in Figure 3. The silicon area of the complete amplifier is 0.117 mm^2 .

Figure 3. Microphotograph of the Proposed Amplifier

Table I summaries the performance parameters of the amplifier. The measured noise spectral density at 1 kHz in unity-gain configuration is $17.47\text{ nV}/\sqrt{\text{Hz}}$, which is thank for the noise optimization. As expected, CMRR exhibits high values from dc up to 150Hz. These frequencies are crucial for sensor applications needed to reject a potential large common-mode signal at low frequency, for instance, the 50 Hz hum noise.

TABLE I. MEASURED PERFORMANCE OF THE PROPOSED AMPLIFIER

Parameter	Proposed Amplifier ($\pm 1.65\text{ V @ } 25^\circ\text{C}$)
DC Gain	114 dB
Unity Gain Bandwidth	2.3 MHz
Phase Margin	64 degree
CMRR at DC (Mean)	120 dB
CMRR at 50Hz (Mean)	113 dB
CMRR at 150Hz (Mean)	110 dB
Positive Slew Rate	$2.2\text{ V}/\mu\text{S}$
Negative Slew Rate	$2.1\text{ V}/\mu\text{S}$
Offset (Mean)	0.0504 mV
Offset (Standard Deviation)	0.678 mV
Offset Drift (Mean) (-55°C to $+125^\circ\text{C}$)	$0.78\text{ }\mu\text{V}/^\circ\text{C}$
$1/f$ Noise @1kHz	$17.47\text{ nV}/\sqrt{\text{Hz}}$
Positive PSRR at DC	110 dB
Negative PSRR at DC	115 dB
THD at 1Vrms (20dB Gain)	81 dB
Silicon Area	0.117 mm^2
Supply Current	231 μA
Load	100k // 100pF

Figure 4 displays the histogram of CMRR performance at dc. Of all the 15 samples measured, the mean value of 120dB CMRR at dc has revealed that the tendency of the yield for achieving very high CMRR values is excellent. For offset evaluation, Figure 5 displays the measurement results on 15 samples in a histogram. The mean offset is

50.4 μ V whereas the standard deviation of offset is 0.678mV. However, the standalone dc offset term does not represent the entire offset performance. Temperature tests were also conducted on the prototypes. Figure 6 depicts the offset drift of 15 chips over a wide temperature range, -55°C~125°C. The mean offset drift is 0.78 μ V/°C, which is very low for all the chip samples despite various minute offset values. Of particular interest is the fact that the additional offset contribution arising from the offset drift does not swamp the nominal offset. It has confirmed the combined techniques that (i) the averaging layout permits low geometry mismatches, maintaining low offset in low temperature range whereas (ii) the composite front end on the basis of second differential gain stage clamping the first differential gain stage gives a good common mode rejection to the leakage currents in NMOS active loads, leading to low offset at high temperature range. As a result, the amplifier circuit is able to sustain low offset over a wide temperature range. In final remark, the measured CMRR and offset results, summarized in Table I, outperform the recently reported work of amplifier [8] having 100dB CMRR and 3mV offset. The intrinsic low sensitivity of the proposed structure to the mismatching factors is therefore validated, confirming the effectiveness and robustness of the circuit architecture when using both circuit design technique and averaging layout technique.

Figure 4. Histogram of CMRR at DC

Figure 5. Offset Distribution of Proposed Amplifier

Figure 6. Offset versus Temperature

V. CONCLUSION

The design of a new precision amplifier is presented. The experimental results have validated that the untrimmed low-noise amplifier can offer significantly enhanced metrics in terms of CMRR, offset and offset drift, suggesting that the composite front-end input stage architecture has the key advantage of simplicity with instrumentation-based performance. The amplifier is particularly useful for analog sensor signal processing.

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