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Design and Analysis of Transmit/Receive Switch in Triple-Well CMOS for MIMO Wireless Systems

Andrew Poh and Yue Ping Zhang

Abstract—This paper presents the design and analysis of an RF transmit/receive switch in CMOS for multiple-input multiple-output (MIMO) wireless systems. First, both full-range and abridged quad-pole quad-throw (4P4T) switch architectures for MIMO systems with four antenna elements are comparatively studied. The full-range 4P4T switch is selected for circuit implementation because of its more switching states and lower insertion loss. The series connection and body-floating techniques are then employed in the circuit design to achieve an acceptable performance. Fabricated in 0.12- μm triple-well CMOS with an effective die area $0.35 \times 0.19 \text{ mm}^2$, the 4P4T switch exhibits less than 2.7-dB insertion loss and higher than 20-dB isolation over the frequency range from 2 to 10 GHz. It also attains measured power-handling capability more than 25 dBm at 2.4 and 5.8 GHz.

Index Terms—CMOS, multiple-input multiple-output (MIMO), transmit/receive (T/R) switch, wireless communications.

I. INTRODUCTION

MULTIPLE-INPUT multiple-output (MIMO) technology is currently being considered for use in cellular communication broadband wireless access, as well as for wireless local area networks [1]. MIMO technology is enabled by the presence of multiple transmit antennas and multiple receive antennas in the communication link. Spatial diversity and spatial multiplexing are two mechanisms by which MIMO enhances capacity and robustness of the link. Spatial diversity represents the existence of multiple signal paths between the multiple transmit and receive antennas that fade independently. As such, the probability of having all the signal strength falling below detection threshold would be very low. In other words, the probability of having all the antennas in adverse locations is significantly reduced with the presence of multiple receive antennas. Therefore, spatial diversity improves the robustness of the link. Spatial multiplexing involves the transmission and reception of multiple data streams from multiple antennas at either the same time or in the same frequency spectrum. The multiple antennas are primarily used to split the different data streams at the receiver. Spatial multiplexing facilitates an increase of data rate without the requirement for a larger

frequency spectrum as the gains arise from a resolution of parallel spatial paths in the channel.

Regardless of whether spatial diversity or spatial multiplexing is used, the key problem of any MIMO system is an increased complexity, which often translates to higher cost. Hybrid selection is a popular method in overcoming the complexity issues. It involves a reduction in the number of active antennas used in the course of transmission or reception. The hybrid selection scheme necessitates the use of a transmit/receive (T/R) switch. The T/R switch has been designed in GaAs for MIMO systems [3]. To the best of our knowledge, the design of the T/R switch in CMOS for MIMO systems has not yet been reported. It is known that the design of the T/R switch in CMOS is rather desirable for high-level integration of MIMO systems.

There have been several T/R switches designed in CMOS for non-MIMO systems [4]–[11]. Key figures-of-merit of a T/R switch includes insertion loss, isolation, and power-handling capability measured by the 1-dB compression point ($P_{1\text{ dB}}$). Regarding the performance of insertion loss and isolation, the effect of substrate resistance is studied in [4] and [5], where low insertion loss is obtained by minimizing the substrate resistance and dc biasing the T/R nodes. A high isolation is achieved using CMOS silicon-on-insulator technology [6]. In both cases, however, the power-handling capability is limited due to the parasitic capacitance and source/drain junction diodes. Thus, techniques of body floating are developed for higher power-handling capability. An LC-tuned substrate bias technique is firstly reported in [7], where the bulk is not separated from the substrate. Using an on-chip inductor can tune the bulk of the switching transistor to be floating at certain frequencies. 28-dBm $P_{1\text{ dB}}$ in the transmit mode is obtained. The disadvantages of this approach are the design complexity and large silicon area consumed. Taking advantage of the modern triple-well CMOS process, the idea of body floating can be simply realized by using a large resistor to bias the bulk [8]. As resistors are intrinsically wideband, the power-handling improvement of this approach is also wideband. 20-dBm $P_{1\text{ dB}}$ was achieved at 5.8 GHz. Another approach to the power-handling improvement is using stacked transistors; however, insertion loss will be degraded and has to be compensated, e.g., by the special depletion layer extended transistor process [9]. A 15-GHz T/R switch is reported in [10], the impedance matching network was employed to improve the power handling, while the isolation performance is degraded. The power-handling capability can also be improved by using differential architectures [11]; 3-dB power-handling capability improvement can be obtained.

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Fig. 1. Full-range 4P4T architecture [3].

This paper presents the first T/R switch designed in CMOS for MIMO systems. Section II evaluates two T/R switch architectures for MIMO systems. Section III describes the circuit design in a 0.12- μm triple-well CMOS. Section IV discusses the experimental results. Finally, Section V summarizes the conclusions.

II. SWITCH ARCHITECTURES FOR MIMO SYSTEMS

Traditionally, a T/R switch serves to assign a single antenna between the transmitter and receiver according to the time division duplexing command. A MIMO system, however, shifts the paradigm to which the T/R switch functions. It utilizes multiple antennas to attain true full duplexing and, therefore, does not require the switch to specify the transmitting or receiving operations. The number of antenna elements used in the MIMO system dictates the configuration of the T/R switch. It is suggested that the antenna elements for a base station be limited to a moderate number such as four, as a large number of antennas pose environmental problems [1], [2]. In addition, it is also predicted that a maximum of four dual polarized patch antennas with half-wavelength spacing can be exploited for terminal operations. However, there are concerns that space constraints in handsets may pose a challenge to the use of more than one antenna. Nevertheless, we believe that four antenna elements are proper for most MIMO systems.

Two 4P4T T/R switch architectures have been proposed for MIMO systems with four antenna elements [3]. Unfortunately, neither has been thoroughly evaluated. Here, the two architectures are comparatively studied according to their complexity and performance. Fig. 1 shows the full-range 4P4T architecture. The switch exhibits a total of 16 states determined by four bias controls, V_{c1} to V_{c4} . The architecture allows a full-range switching states, which means that there is no redundant port. Fig. 2 shows the abridged quad-pole quad-throw (4P4T) architecture. The abridged 4P4T architecture offers a reduction in complexity through a decrease in the number of bias controls. However, the reduction is made at the expense of switching

Fig. 2. Abridged 4P4T architecture [3].

states. There are eight possible states for the architecture; however, the number of usable states is limited to only four. The redundant four states involve the direct connection of a transmitter to the receiver of a different set, thereby eliminating any possibilities of use for on-chip calibration operations. As such, the limitations of the switch architecture present several implications. Foremost, the configuration only allows for a single transmitting and receiving operation at any one time, which implies that the switch is only capable of single-in-single-out operations. Another concern is that individual transmitting and receiving operations are each limited to two antennas, which imposes constraints on the degrees of freedom, thereby severely crippling the exploitation of antenna diversity advantages.

Both architectures perform differently for insertion loss and isolation. The insertion loss of the full-range 4P4T architecture is smaller than that of the abridged 4P4T architecture because the signal passes through an additional transistor in the abridged 4P4T architecture. The isolation of the full-range 4P4T architecture is lower than that of the abridged 4P4T architecture maximally by 3 dB because there are two off-state transistors in parallel in the full-range 4P4T architecture, while there is only one off-state transistor in the abridged 4P4T architecture connecting the transmitter and the receiver of the same set. Our simulations show that the insertion loss of the full-range 4P4T architecture is 0.7 dB better than that of the abridged 4P4T architecture, but the isolation of the full-range 4P4T architecture is 1.5 dB worse than that of the abridged 4P4T architecture. Both architectures perform similarly for power-handling capability because they share the same mechanisms limiting power handling. Based upon the above evaluation, the full-range 4P4T architecture is selected for circuit implementation in this study. The full-range 4P4T architecture can support both a one-uplink-three-downlink antenna operation as well as a two-uplink-two-downlink antenna operation.

III. CIRCUIT DESIGN IN TRIPLE-WELL CMOS

The circuit was designed using Cadence SpectreRF in the 0.12- μm triple-well CMOS from ST Microelectronics, Grenoble, France. Two circuit techniques known as body floating and series connection of transistors were employed to enhance the switch performance. It is shown that an increase in body resistance can improve the insertion loss and that the floating of the body can improve the power handling [8]. The body-floating technique is not viable with bulk CMOS, as it involves manipulation to the substrate conditions. With triple-well CMOS, the body is isolated from the substrate. Therefore, a resistor can be introduced to the body contact of the transistor to float the body. Besides improving the power handling, the introduction of resistors to the body contact

Fig. 3. Series-connected transistors for the switch.

serves to reduce the insertion loss by diminishing capacitive coupling losses through the body contact. Furthermore, the body resistors function to eliminate the coupling between transistors that increases the insertion loss in the configuration of series-connected transistors. The series connection of transistors is a potential method to increase the power handling. A major setback for the technique lies with the fact that it yields a significant increase in the insertion loss. The series connection of transistors is viable with triple-well CMOS as the addition of resistors to the body contact can prevent losses through the body, thereby facilitating an equal voltage division, as well as manageable insertion losses. It was highlighted that the series connection of transistors results in a different impedance to ground at each successive drain/source node [9]. The asymmetry produces an unequal splitting of the RF voltage causing the transistor nearest to the signal source to experience the largest voltage and breakdown first. Again, the concern is unwarranted with triple-well CMOS as the body is floated at RF and isolated from the substrate. Hence, the series connection of transistors does not exhibit any symmetry issues reported in conventional bulk CMOS.

Fig. 3 shows the series-connected transistor structure proposed for the switch. As shown, both the gate and body nodes are biased using individual large resistors R_G and R_B . The use of individual resistors is necessary to prevent signal coupling between the series-connected transistors. To date, only the advantages of implementing resistors at the gate node have been widely covered in the literature [4]. Increasing the number of series-connected transistors effectively improves the power handling and isolation, while compromising the insertion loss. Therefore, it is expected that there exists an optimum number of series-connected transistors for which the switch performance is optimized.

The size of a transistor is a critical aspect of design as it determines the on-state resistance, as well as the parasitic capacitance. Foremost, the design of the switch should use the minimum length transistors so as to minimize the on-state resistance for each transistor in the proposed series-connected configuration. It is known that there exists an optimum transistor width for insertion loss. With reduction of the capacitive losses due to the introduction of the body resistance, the insertion loss of the switch can be attributed predominantly to the on-state resistance. Based upon the assumption that the capacitive coupling through the n-well isolation is negligible, for a series-connected

Fig. 4. Annotated cross-sectional view of triple-well nMOS transistor.

transistor, the insertion loss is given by

$$IL = 20 \log \left| 1 + \frac{N}{2Z_o} \left(\frac{L}{K_n W (V_{CTRL} - V_T)} \right) \right| \quad (1)$$

and the isolation is given by

$$ISO = 20 \log \left| \sqrt{1 + \left(\frac{N}{Z_o} \left(\frac{1}{\omega W (2LC_{dsc} + C_{G1})} \right) \right)^2} \right| \quad (2)$$

where $C_{ds} = WL \cdot C_{dsc}$ and $C_{G1} = C_{gs} = C_{gd}$ such that $C_G = W \cdot C_{G1}$, N defines the number of series-connected transistors used in the switch, Z_o is the source/load impedance, and others have their usual meanings.

Fig. 4 depicts an annotated cross-sectional view of a triple-well nMOS transistor with the relevant parasitic components and introduced resistors. In a triple-well implementation, there exist two pn-junction diodes, one between the p-well and deep n-well and the other between the deep n-well and p-substrate. These two junction diodes have to be maintained in reverse bias in order to prevent a breakdown in isolation between the p-well, deep n-well, and p-substrate.

As seen in Fig. 4, a large resistor R_{SUP} is also introduced to the deep n-well node in addition to the resistors connected that are to the gate and body nodes. The large resistor R_{SUP} serves to float the deep n-well node at RF. This allows the RF voltage level in the deep n-well to adjust according to the RF voltage swing in the p-well, thereby ensuring that the p-well to deep n-well junction diode is always in reverse bias. The capacitance between the p-substrate and deep n-well junction can be kept minimum by isolating each transistor with an individual deep n-well. For our implementation, each transistor is placed into a p-well of area $211.5 \mu\text{m}^2$ within a deep n-well area of $345.83 \mu\text{m}^2$, yielding a capacitance of 171 fF between the p-well and deep n-well interface and 71-fF capacitance between the deep n-well and p-substrate interface. As such, the effective series parasitic capacitance between the p-well and p-substrate can be neglected and, therefore, the body node of the transistor can be considered as a floating node at RF.

To reiterate, the power-handling limitations of conventional CMOS switches have mainly been attributed to either the unintentional forward biasing of the source/drain-to-body junction diodes of the off-state transistors or the turning on of the off-state switch transistors by a gate-drain/source voltage that

Fig. 5. Equivalent circuit of an N -series-connected transistor switch in the off state. (For the 20-finger 285- μm off-state transistor used: $C_{gs} = 145$ fF, $C_{gd} = 144$ fF, $C_{db} = 2.6$ aF, $C_{sb} = 2.8$ aF, $C_{ds} = 15$ aF).

is greater than the magnitude of the threshold voltage [9]. However, it can be shown that the power-handling limitation of the switch implemented with a floating body and series-connection technique would predominantly depend upon the voltage at which the off-state switch transistors are turned on.

As illustrated in Fig. 5, the drain and source nodes of the off-state N -series-connected transistor switch are coupled by a series of capacitance. In most cases, the drain/source-to-body capacitances and the drain-source capacitance are relatively smaller compared to the drain/source-gate capacitances and, therefore, can be neglected. Hence, the overall isolation can be attributed mainly to the drain/source-gate capacitance. The voltage across the overall drain and source node will be divided equally by symmetry and, therefore, the effective drain/source-gate voltages across each transistor will be reduced significantly. Hence, the gate-source voltage at which the off-state transistors are turned on limits the power handling. By this analysis alone, the power handling would be independent of transistor width as long as the resistance of the on-state switch is kept small. It is well known that the application of dc bias to both the source and drain nodes can also boost power handling [4]. However, the main drawback of applying a dc bias to both the source and drain node would be the increase in the on-state resistance in the on-state switch. When smaller transistor width is used, the on-state resistance may increase to significant values, which may result in a significant increase to the equivalent input impedance seen at the input of the switch. The increase in equivalent input resistance would result in a larger input voltage swing and, hence, the switch would compress at a lower input power than expected. Hence, it is desirable to keep the on-state resistance as low as possible and, therefore, larger transistor width is desirable. The series connection of transistors allows for the achieving of lower on-state resistance through a selection of transistors with larger width while maintaining an acceptable isolation. The 1-dB compression for an optimized N series-connected transistor switch can be estimated by

$$P_{1\text{-dB}} = 10 \log \left(\frac{2N^2 (V_{gs(\text{off})} - V_{th})^2}{50} \right) + 30 \text{ (dBm)} \quad (3)$$

where $V_{gs(\text{off})}$ is the effective dc voltage between the gate and source of the N th transistor in the series connection. The derivation of the above equation is as follows. A single off-state tran-

Fig. 6. Variation of the insertion loss with respect to the transistor width and gate resistance at $N = 1$.

sistor remains off as long as

$$V_{gs(\text{off})} + \frac{V_{d\text{max}}}{2} \leq V_{th}. \quad (4)$$

Thus, N -series-connected transistors remain off as long as

$$V_{gs(\text{off})} + \frac{V_{d\text{max}}}{2N} \leq V_{th}. \quad (5)$$

This leads to the maximum input voltage swing that can be tolerated, which is

$$V_{d\text{max}} = 2N (V_{th} - V_{gs(\text{off})}). \quad (6)$$

Since the maximum handling power is determined by

$$P_{1\text{-dB}} = 10 \log \left(\frac{(V_{d\text{max}})^2}{2Z_0} \right) + 30 \text{ (dBm)}. \quad (7)$$

Equation (3) can be obtained by substituting (5) into (7).

An insight to the design of the switch is provided below. The initial analysis is based upon the optimization of a SPDT switch. It is known that the insertion loss increases as the frequency of operation increases as the capacitive loss mechanisms predominate at higher frequencies. The capacitive loss partially occurs through the gate of the transistor. The gate capacitance increases as the transistor width increases; therefore, the gate capacitance appears as a path for the high-frequency signals, thereby resulting in increased loss. Introducing a resistor to the gate of the transistor can reduce the loss. Fig. 6 illustrates the variation of the insertion loss with respect to the transistor width and gate resistance at 10.6 GHz. The insertion loss is suppressed with increasing gate resistance. However, the insertion loss increased significantly when the gate resistance was approximately 100 Ω . This is consistent with the maximum point indicated in [4], whereby the maximum insertion loss is predicted to occur when the gate resistance is equivalent to the impedance of the total loss capacitance $R_G = 1/\omega C$ within an $R-C$ series network. As such, it is ideal to use a large gate resistance to achieve lower insertion loss. A typical value of 10 k Ω is recommended. However, it is also observed from Fig. 7 that the capacitive loss still dominates at larger width even after 10-k Ω gate resistance has

Fig. 7. Variation of the insertion loss with respect to the transistor width and frequency at $R_G = 10 \text{ k}\Omega$ and $N = 1$.

Fig. 9. Variation of the isolation with respect to the transistor width and frequency at $R_G = 10 \text{ k}\Omega$ and $N = 1$.

Fig. 8. Variation of the isolation with respect to the transistor width and gate resistance at $N = 1$.

Fig. 10. Variation of the insertion loss with respect to the transistor width and body resistance at $R_G = 10 \text{ k}\Omega$ and $N = 1$.

been introduced, which indicates that there is another capacitive path for loss.

As seen in Fig. 8, the isolation is generally degraded by 40 dB with the introduction of the gate resistor. This is due to the fact that the resistor floats the gate node at RF. Hence, the loss mechanism in the off state through the gate node is eliminated. As such, the isolation is determined mainly by the coupling of the parasitic gate capacitance. It can be observed from Fig. 9 that the isolation mechanism is purely capacitive in nature, as there is no convergence for isolation at different frequencies. It should be mentioned that the maximum power handling is improved by 3 dB to 11.5 dBm with the inclusion of the gate resistor for the case of $N = 1$.

As mentioned earlier, there is another capacitive coupling loss mechanism that affects the switch insertion loss. Fig. 8 shows that the introduction of the body contact resistance is able to suppress this capacitive loss mechanism. Similar to that observed in Fig. 10, the insertion loss increases considerably with the body resistance of 100Ω . As explained earlier, it may be attributed to the series $R-C$ loss effect, whereby the impedance of the loss capacitance is equivalent to the body resistance. Therefore, the body resistance of $10 \text{ k}\Omega$ is selected. As observed in Fig. 11, the insertion loss is constant throughout all frequencies. Hence, the capacitive coupling

Fig. 11. Variation of the insertion loss with respect to the transistor width and frequency at $R_B = R_G = 10 \text{ k}\Omega$ and $N = 1$.

loss mechanisms have been suppressed entirely by the gate resistance of $10 \text{ k}\Omega$ and the body resistance of $10 \text{ k}\Omega$. As such, the on-state resistance solely characterizes the insertion loss. In comparison with the earlier results, the addition of the body resistance reduces isolation by 10 dB. This is indicative that the loss mechanism through the gate node in the off state is more significant than that through the body. Nevertheless, the isolation mechanism is shown to depend upon the capacitive coupling via both the gate and body capacitance.

Fig. 12. Variation of the insertion loss with respect to the transistor width and the number of series-connected transistors at $R_B = R_G = 10 \text{ k}\Omega$.

Fig. 13. Variation of the isolation with respect to the transistor width and the number of series-connected transistors at $R_B = R_G = 10 \text{ k}\Omega$.

Fig. 12 shows the variation of the insertion loss with respect to the transistor width and the number of series-connected transistors at 10.6 GHz, $V_{CNTRL} = 1.2 \text{ V}$, and $V_r = 0 \text{ V}$. It is observed that although the insertion loss increases as the number of series-connected transistors is increased, the difference does not appear significant when the large transistor width is used. Fig. 13 shows the variation of the isolation with respect to the transistor width and the number of series-connected transistors at 10.6 GHz, $V_{CNTRL} = 1.2 \text{ V}$, and $V_r = 0 \text{ V}$. It is evident that the isolation is improved by approximately 5 dB for every additional series-connected transistor used. The power handling is also improved as the number of series-connected transistors is increased while maintaining a constant isolation close to 20 dB at 10.6 GHz. For $N = 4$, the power-handling capability reaches 28 dBm.

The performance of the full-range 4P4T switch using single-transistor ($N = 1$) switches is nonviable. The replacement of the single-transistor ($N = 1$) switches with the switches of four series-connected transistors ($N = 4$) resolves the performance problems. Fig. 14 shows the variation of the insertion loss with respect to the transistor width and the frequency of operation. It is seen that the insertion loss depends slightly on the frequency. Fig. 15 shows the variation of the isolation with respect to the transistor width and the frequency of operation. The isolation for the 4P4T switch was simulated between the transmitter

Fig. 14. Variation of the insertion loss with respect to transistor width and frequency.

Fig. 15. Variation of the isolation with respect to the transistor width and frequency.

and receiver ports of the same set as they yield the worst case isolation. As shown, the minimum isolation of 20 dB can be achieved by using transistors of larger widths. The transistor width to yield an isolation of 20 dB at 10.6 GHz is approximately $270 \mu\text{m}$ with a control on voltage of 1.2 V and a source/drain bias of 0 V. With the control on voltage increased to 1.8 V and the source/drain bias to 0.6 V, the transistor width can be increased up to $310 \mu\text{m}$ in order to maintain an isolation of 20 dB at 10.6 GHz.

Transistors of width $285 \mu\text{m}$ are finally chosen for the switch, as it yields an isolation of more than 20 dB at 10.6 GHz. The power-handling capability is significantly improved, as compared with the 4P4T switch using the single-transistor switches. The implementation of the proposed techniques of floating body and series connection showed that power handling could be improved by at least 13 dB. The application of 1.8-V control voltage with 0.6-V drain/source biasing produced an additional 9-dB improvement. Periodic steady-state simulation for the 4P4T switch indicated a 1-dB compression point of approximately 28 dBm, which concurs with the value that was estimated using (3).

In order to fully appreciate the power-handling improvements brought about the techniques utilized, consider the case with reference to Fig. 1, when a $50\text{-}\Omega$ source is connected to the transmitter A (TXA) port and the ports are all matched to 50Ω . The

Fig. 16. Simulated waveforms of the RF voltage swing at the input with an input power of 30 dBm for transistors with a width of 60 μm and 285 μm , respectively.

Fig. 17. Simulated waveforms of the RF voltage swing at the junction between the p-well and deep n-well of each 285- μm transistor with an input power of 30 dBm for SW2.

drain/source node voltage (V_r) was biased at 0.6 V and the control voltage was set to 1.8 V. Switch SW1 is on and switch SW2 is off. The input signals at the nodes of each transistor in the switches were simulated. As shown in Fig. 16, for an input signal of 30 dBm, the voltage swing at the input of the switch comprising of switches of transistors of 60- μm width is larger than that for the switch with transistors of 285- μm width. This is because the increased on-state resistance of the switch with smaller transistor width has significantly increased the equivalent input resistance looking into the switch. Therefore, a larger input RF swing develops at the input and, hence, the switch with smaller transistor width would compress with a lower input power.

Fig. 17 illustrates the voltage between the p-well (body) and deep n-well node for the case with the transistor width of 285 μm for SW2. As observed, the junction is never forward biased as the voltage swings are well below the turn-on voltage for the junction diode of 0.57 V.

From Figs. 18 and 19, the gate-drain and gate-source voltages are shown to be relatively equal for all the series-connected transistors concurring with our analysis that the input voltage swing is divided equally between the gate-source/drain capacitances. Compression has occurred as the off-state transistors are turned on, as seen in Figs. 18 and 19.

Fig. 18. Simulated waveforms of the RF voltage swing of the gate-drain voltage of each 285- μm transistor with an input power of 30 dBm for SW2.

Fig. 19. Simulated waveforms of the RF voltage swing of the gate-source voltage of each 285- μm transistor with an input power of 30 dBm for SW2.

Fig. 20. Die microphotograph of the full-range 4P4T switch in 0.12- μm triple-well CMOS.

IV. MEASUREMENT RESULTS

The switch was fabricated in a 1.2-V two-poly six-metal 0.12- μm triple-well CMOS process. The switch die microphotograph is shown in Fig. 20. The overall die size is $0.98 \times 0.5 \text{ mm}^2$ owing to the large number of pads. The effective area without a pad is only $0.35 \times 0.19 \text{ mm}^2$.

The switch measurements were performed on-wafer. The control on voltage was 1.8 V and the source/drain bias was 0.6 V. Fig. 21 shows the simulated and measured insertion loss

Fig. 21. Simulated and measured insertion loss.

Fig. 22. Simulated and measured isolation.

Fig. 23. Measured insertion loss versus input power level.

from antenna 1 (ANT1) to receiver A (RXA). The measured insertion loss is less than 2.7 dB over the frequency range from 2 to 10 GHz. Fig. 22 compares the simulated and measured isolation between transmitter A (TXA) and RXA. The isolation is 20 dB better over the frequency range from 2 to 10 GHz. The simulations agree reasonably with the measurements. The power-handling capability was measured at 2.4 and 5.8 GHz, respectively. The maximum 25-dBm input power was limited by our testing setup. Estimated from Fig. 23, the switch should have power-handling capability over 25 dBm.

Table I shows the comparison of this full-range 4P4T switch in CMOS with the abridged 4P4T switch in GaAs at 5.8 GHz. It is seen that the full-range 4P4T switch in CMOS achieves lower

TABLE I
PERFORMANCES OF MIMO T/R SWITCHES

Process	Loss dB	Isolation dB	P_{1dB} (dBm)	Chip size mm^2	Ref
0.12- μm CMOS	2.7	22	25	0.98×0.5	This work
0.25- μm GaAs	2.7	20	35	1.125×0.75	[3]

insertion loss, comparable isolation, but worse power-handling capability.

V. CONCLUSION

This paper has described the design and analysis of an RF T/R switch in CMOS for MIMO wireless systems. Both full-range and abridged 4P4T switch architectures for MIMO systems with four antenna elements were comparatively studied. The full-range 4P4T switch has 16 switching states and lower insertion loss was, therefore, selected for circuit implementation. Both series connection and body-floating techniques were employed in the circuit design of the full-range 4P4T switch to achieve an acceptable performance. The 4P4T switch was fabricated in 0.12- μm triple-well CMOS with an effective die area $0.35 \times 0.19 \text{ mm}^2$. The 4P4T switch achieved less than 2.7-dB insertion loss and higher than 20-dB isolation over the frequency range from 2 to 10 GHz. It was also found that the measured power-handling capability was more than 25 dBm at 2.4 and 5.8 GHz.

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REFERENCES

- [1] A. F. Molisch and M. Z. Win, "MIMO systems with antenna selection," *IEEE Micro*, vol. 5, no. 1, pp. 46–56, Mar. 2004.
- [2] D. Gesbert, M. Shafi, D. S. Shiu, P. J. Smith, and A. Naguib, "From theory to practice: An overview of MIMO space-time coded wireless systems," *IEEE J. Select. Areas Commun.*, vol. 21, no. 4, pp. 281–302, Apr. 2003.
- [3] C.-H. Lee, B. Banerjee, and J. Laskar, "Novel T/R switch architectures for MIMO applications," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1137–1140, Jun. 2004.
- [4] F.-J. Huang and K. O., "A 0.5- μm CMOS T/R switch for 900-MHz wireless applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 486–492, Mar. 2001.
- [5] Z. Li, H. Yoon, F.-J. Huang, and K. O., "5.8-GHz CMOS T/R switches with high and low substrate resistance in a 0.18- μm CMOS process," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 1, pp. 1–3, Jan. 2003.
- [6] C. Tinella, J. M. Fournier, D. Belot, and V. Knopik, "A high-performance CMOS-SOI antenna switch for the 2.5–5-GHz band," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1279–1283, Jul. 2003.
- [7] N. A. Talwalkar, C. P. Yue, H. Gan, and S. S. Wong, "Integrated CMOS transmit-receive switch using LC-tuned substrate bias for 2.4-GHz and 5.2-GHz applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 863–870, Jun. 2004.
- [8] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin, Y.-T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 31–39, Jan. 2006.

- [9] T. Ohnakado, S. Yamakawa, T. Murakami, A. Furukawa, E. Taniguchi, H. Ueda, N. Suematsu, and T. Oomori, "21.5-dBm power-handling 5-GHz transmit/receive CMOS switch realized by voltage division effect of stacked transistor configuration with depletion-layer-extended transistors (DETs)," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 577–584, Apr. 2004.
- [10] Z. Li and K. O., "15-GHz fully integrated nMOS switches in a 0.13- μ m CMOS process," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2323–2328, Nov. 2005.
- [11] Y. P. Zhang, Q. Li, W. Fan, C.-H. Ang, and H. Li, "A differential CMOS T/R switch for multi-standard applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 8, pp. 782–786, Aug. 2006.

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