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Robust On-Chip Signaling by Staggered and Twisted Bundle

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Existing shield insertion for multiple signal nets can lead to a nonuniformly distributed, capacitive-coupling length and inductive return paths, introducing large delays and delay variation by crosstalk. This article discusses a twisted, staggered interconnect structure that reduces both inductive and capacitive crosstalk. The proposed design reduces delay by 25% and reduces delay variation by 25 $\times$ compared to designs employing coplanar shields.

■ **CHIP MULTIPROCESSORS (CMPs)** are becoming the semiconductor industry's dominant hardware paradigm because they do not lead to unmanageable power dissipation, which often results from the technology scaling of uniprocessor designs. On-chip components can be easily shared in CMPs, improving the throughput rate. However, because of the additive effect of improved component utilization, the increased integration density and data sharing in a CMP exacerbate soft errors by the global interconnect when delivering signal or clock data. It is a well-known challenge for the gigascale integration of uniprocessor designs to consider delay variation and distribute a low-skew or low-jitter global signal or clock data in the presence of crosstalk.¹⁻³ Because of the highly compact integration of the CMP interconnect, the adjacent coupling capacitance of the global interconnect increases. In addition, inductance also becomes significant when the signal's slew rate is sharp, to switch from one state to another.^{4,5}

Crosstalk, resulting from capacitive and inductive coupling, could severely affect the timing and signal integrity of clock or signal nets. Because each interconnect experiences a different capacitive-coupling length or a different inductive-coupling return path, the interconnect exhibits varying signal or clock delay under different switching patterns.

Consequently, high-speed digital circuits in CMPs that use dynamic logic are more susceptible to crosstalk compared to circuits that use static logic.

In this article, we introduce a *twisted and staggered shielding* (TSS) structure for robust on-chip signaling that minimizes both inductive

and capacitive coupling, by means of uniformly distributing twisted shields (see the "Related Work" sidebar). We describe a transmission line model we developed to explain why TSS can reduce both capacitive and inductive couplings. Furthermore, we present an automatic layout synthesis for the design of a TSS bundle, which we validated with a Spice simulation of the worst-case delay and the worst-case noise. What's more, we fabricated a test chip to verify the delay and its variations of all these structures under different switching patterns. As our results will show, compared to the coplanar shielding (COS) structure, the TSS structure reduces delay by 25% and reduces delay variation by 25 $\times$. When compared to the twisted and normal interconnects with shields (TNS) structure, the proposed TSS structure also reduces delay by 7.5% and reduces delay variation by 33 $\times$.

Twisted signal and shield pairs

In explaining the design of our TSS structure, we begin by discussing key characteristics of a pair of twisted and normal wires. The use of twisted wire is well-known in wired transmissions such as in telephone lines and cables. This approach interleaves the polarity of magnetic flux and so cancels inductive coupling and can

Related Work

Researchers have proposed various techniques to improve the robustness of on-chip signaling. Compared to buffer insertion, which is one way to improve robustness, *shields* are an effective approach but with a smaller implementation cost.^{1,2} Because *coplanar shielding* (COS) reduces the capacitive-coupling length and provides a local return path for inductive coupling, designers commonly use COS to reduce crosstalk in layouts. To minimize self-inductance, for example, Massoud et al. introduced an interdigitized coplanar shielding technique.¹ In other work, Kaul et al. described an active shielding method that applies complementary signals on shields,² and Qi et al. have experimentally demonstrated coplanar shielding's effectiveness.³ However, because chip multiprocessors have many global signal nets, the use of COS in a CMP design would excessively consume the signal net's routing resource. As a result, many signal nets typically share only one shield, which can lead to delay variation.

In another approach to shield distribution, interconnects are twisted together with shields, using via arrays in copper interconnects with small via resistive loss and improved reliability. Hidaka et al. were the first to introduce the twisted pair into differential signaling to reduce crosstalk in DRAM design.⁴ Recently, Mensink et al. conducted further studies of the optimal twist position for *RC*-dominant interconnects.⁵ Like COS shielding, in which each signal net is designed with its differential net, the use of differential pairs increases the design cost for multiple signal nets—or what in this article we call a *bundle*. To minimize that cost, Zhong et al. introduced a method to distribute shielding for multiple signal nets, that is, bundles.⁶ Using both *twisted and normal interconnects with shields* (TNS), they minimize inductive coupling by compensating for the polarity-interleaved magnetic fluxes between the twisted group and the

normal group. Sato and Masuda further measured the delay variation of TNS by twisting only shields,⁷ a simplified design of work done by Zhong et al.⁶ However, with normal interconnects, shields are not uniformly distributed. Capacitive coupling is therefore significant not only between the twisted and normal interconnects but also among those interconnects inside the normal group. As a result, each bit in TNS could have a different capacitive-coupling length, which means delays can still be largely varying for signal nets.

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be explained by a derivation based on a pair of transmission lines.

Pair of twisted and normal wires

As Figure 1 shows, a twisted pair means that each signal has a shield as the local ground. Moreover, the aggressor—which has a switching input—is a normal interconnect with a shield, and the victim—which is quiet (does not switch)—is a twisted interconnect with another shield. Note that due to the symmetry,

the victim and its shield experience an equal coupling in the twisted pair.

The wire is divided into N segments with $(N - 1)$ stages. Each segment has unit length l . To analyze the crosstalk, the aggressor is modeled by the voltage source V_{ASrc} with the source and load impedance Z_{ASrc} and Z_{Ald} , and the victim is modeled by the source and load impedance Z_{Vsrc} and Z_{Vld} . The crosstalk-introduced noise at the receiver contains two parts: inductive noise V_{ind} and capacitive

Figure 1. Typical twisted pair signaling with six ($N = 6$) segments and five stages of twists.

noise V_{cap} . Next, we derive the induced crosstalk voltage in frequency domains.

We first determine the inductive-coupling introduced noise, V_{ind} . As Figures 2a and 2b show, we assume that the current at the i th stage of the aggressor is I_{Ai} , and the mutual inductance (unit length) is M_0 between two loops: one loop composed by the aggressor with its local ground, and the other composed by the victim with its local ground.

Figure 2. Detailed crosstalk model (a) and simplified equivalent model for inductive crosstalk (b); detailed crosstalk model (c) and simplified equivalent model for capacitive crosstalk (d).

Then the superposed total $V_{induced}$ is

$$V_{induced} = (sM_0l)(I_{A1} - I_{A2} + I_{A3} - \dots) \quad (1)$$

where the aggressor current I_{Ai} is approximated by

$$I_{A1} \approx I_{A2} \approx I_A = \frac{V_{Asrc}}{(Z_{Asrc} + Z_{Ald})} \quad (2)$$

Because the equivalent model works as a voltage divider, the inductive noise V_{ind} observed at the receiver becomes

$$V_{ind} = \frac{Z_{Vld}}{(Z_{Vld} + Z_{Vsrc})} \times V_{induced}$$

Based on Equations 1 and 2, V_{ind} becomes

$$V_{ind} = \begin{cases} \text{if } N \text{ is even, } 0 \\ \text{else, } \frac{Z_{Vld}}{(Z_{Vld} + Z_{Vsrc})} \times (sM_0l)I_A \end{cases} \quad (3)$$

Therefore, when the pair is twisted into an even number of segments, the inductive crosstalk is 0.

When the pair is twisted into an odd number of segments, the inductive crosstalk is as small as the coupling of one divided segment with length l .

We reached this conclusion on the basis of a low-frequency analysis in which the current at each twisted stage was approximately the same according to Equation 2. As shown by the experiment later in this section, this assumption still approximately holds in the high-frequency range when compared to the calculation by the exact 3D field solver.

We can further determine the capacitive-coupling-introduced noise, V_{cap} . As Figures 2c and 2d show, we assume that the coupling capacitance (unit length) is C_0 between the aggressor and victim when there is no shielding. The coupling is αC_0 when shielding exists. The α factor reflects the effect of shielding between the aggressor and victim. Its value can be larger than 1.0

and depends on both aggressor and victim switching patterns.

We can determine a superposed total, I_{induced} :

$$I_{\text{induced}} = (sC_0 l)(V_{A1} + \alpha V_{A2} + V_{A3} + \dots) \quad (4)$$

with the aggressor voltage V_{Ai} calculated at each stage as

$$V_{A1} \approx V_{A2} \approx V_A = \frac{Z_{\text{Ald}}}{Z_{\text{Asrc}} + Z_{\text{Ald}}} V_{\text{Asrc}} \quad (5)$$

The capacitive crosstalk V_{cap} observed at the receiver is

$$V_{\text{cap}} = Z_{\text{Vsrc}} \times (0.5sC_0 Nl)(1 + \alpha) V_A \quad (6)$$

where the interconnect length, Nl , is a constant. Clearly, for the twisted pair, the capacitive coupling contributes to the dominant crosstalk, and it differs from the inductive crosstalk by a factor N .

In the TNS design by Zhong et al.,⁶ the two signals experienced capacitive coupling (with no shield inside) in a range only half that of the interconnect length. This situation worsens with more signal nets—that is, in a twisted bundle structure—that share one shield. Therefore, the TNS structure has limited usefulness if we don't reduce capacitive coupling.

Pair of twisted and staggered wires

We have found that we can alleviate the capacitive-coupling situation by staggering twists as Figure 3b shows, in which shields are alternatively routed between signals.

To see how to reduce the crosstalk by the capacitive coupling, let the number of staggered twists be N_{stag} . We can easily verify that the capacitive-coupling-introduced noise is effectively reduced by a factor of $2N_{\text{stag}}$:

$$V_{\text{cap}} = Z_{\text{Vsrc}} \times (0.5sC_0 Nl) \left(\frac{1 + \alpha}{2N_{\text{stag}}} \right) V_A \quad (7)$$

Thus, by staggering the twisted interconnect in a chip design such as a CMP, we can reduce

the capacitive-coupling length compared to the TNS structure.

Furthermore, by uniformly distributing staggered and twisted shields, we can compensate for flux. As a result, the signal-net flux also approaches 0. In the example shown in Figure 4b, with a 4,000-micron wire length, 1-micron width, and 2-micron spacing, we extracted the loop inductance matrix at 1 GHz using the FastHenry tool (http://www.rle.mit.edu/cpg/research_codes.htm). For a twisted pair with normal wires, the matrix is

$$L_{\text{TNS}} = \begin{bmatrix} 3.501 \times 10^{-9} & 4.069 \times 10^{-14} & 5.159 \times 10^{-11} & 3.147 \times 10^{-15} \\ 4.069 \times 10^{-14} & 3.504 \times 10^{-9} & 4.069 \times 10^{-14} & 5.160 \times 10^{-11} \\ 5.159 \times 10^{-11} & 4.069 \times 10^{-14} & 3.501 \times 10^{-9} & 4.069 \times 10^{-14} \\ 3.147 \times 10^{-15} & 5.160 \times 10^{-11} & 4.069 \times 10^{-14} & 3.504 \times 10^{-9} \end{bmatrix}$$

For a staggered and twisted pair, the matrix is

$$L_{\text{TSS}} = \begin{bmatrix} 3.491 \times 10^{-9} & 5.796 \times 10^{-14} & 5.151 \times 10^{-11} & 4.640 \times 10^{-15} \\ 5.796 \times 10^{-14} & 3.491 \times 10^{-9} & 5.796 \times 10^{-14} & 5.151 \times 10^{-11} \\ 5.151 \times 10^{-11} & 5.796 \times 10^{-14} & 3.491 \times 10^{-9} & 5.796 \times 10^{-14} \\ 4.640 \times 10^{-15} & 5.151 \times 10^{-11} & 5.796 \times 10^{-14} & 3.491 \times 10^{-9} \end{bmatrix}$$

We applied finer discretization (4×4) at each wire cross section to consider skin and proximity effects.

Figure 3. Twisted and normal interconnect (a) and twisted and staggered interconnect (b).

Figure 4. Staggered and twisted interconnects are synthesized using four groups of unit cells (a). An example of a routing matrix on the left for 3-bit signal nets plus 1-bit shielding nets (b).

Here, each signal net and its nearest-neighboring shield comprise a pair, and one end of the signal net is the port to extract the loop inductance. Clearly shown by the extracted L_{TSS} , inductive coupling between adjacent groups of wires is also reduced by several orders of magnitude for the staggered and twisted pair. Therefore, the staggered and twisted pair design can simultaneously reduce both capacitive and inductive couplings. However, routing resources are excessively consumed if we design one shield for each signal net in forming a twisted pair with staggering. Instead, we want one shield shared among multiple signal nets—that is, a shield shared by an interconnect bundle.

Synthesis for staggered and twisted bundle

Once we have our TSS structure, we need a systematic synthesis methodology to design a layout for a bundle of signal-nets using twisted and staggered shields. We can summarize the problem formulation as follows:

TSS synthesis problem: Given the number of signal nets N_{sig} , the number of signal/shield ratios N_{cell} , and the number of staggering stages N_{stag} , the objective of synthesizing a staggered and twisted bundle is to find a routing topology with N_{gp} ($N_{gp} = \frac{N_{sig}}{N_{cell}}$) groups of wires (N_{gp} stands for ratio). Each group has N_{stag} stages formulated by connecting a unit's twisting cell (T), a unit's normal cell (N), and their complements (T_b and N_b) alternatively. Then, we generate adjacent groups of wires by cyclically shifting unit cells.

Figure 3b shows the wire diagram with unit cells for an example in which $N_{sig} = 6$, $N_{cell} = 3$, and $N_{stag} = 1$. We can define four kinds of unit cells (T , N , T_b , N_b) as we construct them.

First, we discuss how to synthesize a twisting cell. A twisting cell consists of N_{cell} signal nets with N_{cell} segments per net. If we assume that each bit of interconnect is equally divided into n ($n = N_{cell} + 1$) segments, we can describe the twisted pattern through a routing matrix T :

$$T = \begin{bmatrix} t_{1,1} & t_{1,2} & \cdots & t_{1,n} \\ t_{2,1} & t_{2,2} & \cdots & t_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ t_{n,1} & t_{n,2} & \cdots & t_{n,n} \end{bmatrix} \quad (8)$$

where its i th row is

$$T = [t_{i,1} \quad t_{i,2} \quad \cdots \quad t_{i,n}]$$

to represent wire segments in the i th bit. The changes between each neighboring column represent changes of routing connections. For example, a pair $(t_{k,i}, t_{k,j})$ means that the k th bit will change from the i th-bit track to the j th-bit track.

As Figure 3a shows, to minimize the inductive crosstalk, we must twist both the signal and shield segments such that the polarity of the current loop for each cell could change symmetrically. In the following, we discuss how to generate the staggered and twisted pattern for multiple signal nets with one shield.

When n is even, we can synthesize the routing matrix for one unit twisting cell as follows, similar to the approach of Zhong et al.⁶

1. Begin with an initial row, $T_0 = (n-1 \ n-2 \ \dots \ 1)$.
2. Cyclically shift T_0 up by one segment $(n-1)$ times, obtain $(n-1)$ number of permuted rows, and construct a cyclic permutation matrix C .
3. Replace the diagonal element in the cyclic permutation matrix by 0 (representing a shield), attach the diagonal element to an additional column (row), and form an $n \times n$ routing matrix T .

On the other hand, when n is odd, we can apply the same procedure by adding one more dummy wire such that the total wires $(n+1)$ in one unit's twisting cell is still even. This avoids the additional design cost that Zhong et al. incurred to enforce permeability for an odd number of wires.⁶

Let's return for a moment to the example in Figure 3b and consider the leftmost cell in the top row. We take the following steps to construct one twisting cell. First, the initial row is

$$T_0 = [3 \ 2 \ 1]$$

Second, the cyclic permutation matrix becomes

$$C = \begin{bmatrix} 3 & 2 & 1 \\ 1 & 2 & 3 \\ 2 & 3 & 1 \end{bmatrix}$$

Third, the complete routing matrix is obtained by

$$T = \begin{bmatrix} 0 & 1 & 2 & 3 \\ 1 & 0 & 3 & 2 \\ 2 & 3 & 0 & 1 \\ 3 & 2 & 1 & 0 \end{bmatrix}$$

We can't synthesize the staggered and twisted bundle solely by using the above-constructed twisting cell; we also need to synthesize the other three unit cells. We obtain the complementary matrix T_b for the twisting cell T in Equation 7 by reversing the order of each row in Equation 8:

$$T_b = \begin{bmatrix} t_{1,n} & t_{1,n-1} & \cdots & t_{1,1} \\ t_{2,n} & t_{2,n-1} & \cdots & t_{2,1} \\ \vdots & \vdots & \ddots & \vdots \\ t_{n,n} & t_{n,n-1} & \cdots & t_{n,1} \end{bmatrix} \quad (9)$$

Furthermore, we can define a normal cell (N) and its complementary (N_b) by the following routing matrices:

$$N = \begin{bmatrix} t_{1,1} & t_{1,1} & \cdots & t_{1,1} \\ t_{2,2} & t_{2,2} & \cdots & t_{2,2} \\ \vdots & \vdots & \ddots & \vdots \\ t_{n,n} & t_{n,n} & \cdots & t_{n,n} \end{bmatrix}$$

$$N_b = \begin{bmatrix} t_{n,n} & t_{n,n} & \cdots & t_{n,n} \\ t_{n-1,n-1} & t_{n-1,n-1} & \cdots & t_{n-1,n-1} \\ \vdots & \vdots & \ddots & \vdots \\ t_{1,1} & t_{1,1} & \cdots & t_{1,1} \end{bmatrix} \quad (10)$$

With these four unit cells defined by the routing matrices in Equations 8, 9, and 10, we can construct the staggered and twisted pattern by interleaving the twisted cell (T, T_b) and the normal cell (N, N_b). The synthesis procedure is the same as the one we used to form one twisted cell.

First, we construct an initial staggered row:

$$R^0 = [T//N_b//T_b//N, \dots, T//N_b//T_b//N]$$

where we repeat the pattern N_{stag} times. We then cyclically permute R^0 one unit cell at a time to obtain the routing matrix for each group as follows:

$$R^1 = P^1 R^0 = [N//T//N_b//T_b, \dots, N//T//N_b//T_b]$$

$$R^2 = P^2 R^0 = [T_b//N//T//N_b, \dots, T_b//N//T//N_b]$$

$$R^3 = P^3 R^0 = [N_b//T_b//N//T, \dots, N_b//T_b//N//T]$$

Figure 4a shows the resulting general structure of the staggered and twisted pattern composed of those unit cells (T, T_b, N, N_b). We further illustrate this procedure in Figure 4b, which is an example of 18 signal nets with 1-stage staggering. This means we have six groups to synthesize when the signal/shield ratio is 3:1. The routing matrix in Figure 4b is shown with dashed lines in different styles to indicate different unit cells. The initial staggering row is cyclically permuted six times, one cell at a time, and the resulting patterns form the overall routing matrix.

Validation by circuit simulation

With this synthesis, we next devised a circuit simulation in which we designed a more complicated layout for the staggered and twisted bundle, which enabled us to further study the TSS (interconnect) structure's impact on worst-case delay (WCD) and worst-case noise (WCN).

We used 180-nm and 70-nm technologies (with a copper interconnect) in the Berkeley predictive model. We considered three interconnect structures for the simulation: the coplanar wire with shielding (COS), the twisted and normal wire with shielding (TNS), and the twisted and staggered wire with shielding (TSS). We assumed the use of M6 to lay out the signals and shields; a minimum wire width of 0.45 micron for 180 nm technology, and 0.2 micron for 70-nm technology; the spacing is 0.5 micron for 180 nm, and 0.2 micron for 70 nm. The via we chose was a 2×2 array of the minimum size (0.2 micron $\times$ 0.2 micron). The wire length was 4,000 microns, and the driver size was about $100\times$ the minimum inverter size. In the test structures we designed, the inductive effect is significant. Their driver strength and resistive loss are less than their characteristic impedance. Furthermore, we used an exponential voltage source for input signals, with a 50-ps rising time. We modeled the nonlinear driver with the Berkeley BSIM3 model (<http://ngspice.sourceforge.net>). We extracted the capacitance using the FastCap tool with wire discretized into 100 boxes along the length. We used the FastHenry tool to extract the resistance and inductance, with an additional 4×4 discretization at the cross section. We then used a distributed *RLC* circuit to model the signal wire.

Tu et al. showed that the WCN occurs when the victim line switches in the same direction as neighboring aggressor lines.⁵ Because it would be too expensive to explore every switching pattern during design, for our simulation we measured the WCN and WCD according to Chen and He's work,⁴ which involved keeping the victim line quiet. Moreover, we assumed the aggressor and victim had a switching window of 200 ps—that is, the earliest and latest arrival times differed by 200 ps. The computational time depended linearly on the number of signal nets and the Spice simulation time for each alignment. To reduce the simulation time for large circuits, we applied model order reduction to generate macro-models for interconnects.

In our validation efforts, we compared the WCD and WCN of COS, TNS, and TSS shielding using six signal wires with a 3:1 signal-to-shield ratio in 180-nm technology. We used three shields for COS and two shields for both TNS and TSS. Figure 5 compares the WCD and WCN when each wire acted as the victim for all three structures. As Figure 5a shows, the variation of WCD between signal nets was smaller in TSS than in COS and TNS. In terms of the average WCD among all six bits, the delay in TSS was 11 ps shorter than in COS (51 ps vs. 62 ps).

Figure 5b shows the WCN. The WCNs of TSS were also uniform among six signal nets. Because of the large capacitive coupling between normal wires, the

WCNs of signal nets—especially for the WCNs of TNS shielding—in the normal group (net 4, net 5, net 6) were much larger (they averaged a 15% delay variation) than those in the twisted group (net 1, net 2, net 3). As a result, the TSS structure in the simulation was optimal in terms of both delay and noise.

Layout and delay measurement circuit

Finally, using the simulation we just described, we designed and fabricated a test chip: a layout and measurement circuit with IBM 130-nm technology with a copper interconnect. Our objective was to learn whether and when inductance becomes

Figure 5. Worst-case delay (WCD) and worst-case noise (WCN) comparison for each signal net of COS, TNS, and TSS structures with a 3:1 signal-to-shield ratio: worst-case delay for each signal (a) and worst-case noise for each signal (b).

important to delay variation, and how the interconnect structure affects delay and delay variation.

As the die diagram in Figure 6 shows, our measurement circuit has four components. The first component is the device under test (DUT)—that is, four groups of interconnect structures. The second component is the testing generation module, including the programmable driver and delay element, and control logic to generate different logic patterns. The third component is a ring receiver. It forms an oscillator with the programmable driver by including DUTs in its signal path. The last component is the read-out circuitry.

We used a 16-bit synchronized counter to directly record the ring oscillator's oscillation frequency. Finally, we applied a slow sampling clock to shift out the counted result. We could then infer the DUT's delay information. Because the DUT is located in the signal paths, we achieved an overall operating frequency of approximately 1 GHz.

Layout of interconnect structure under test

Typically, in the IBM 130-nm technology, the top-layer metal, called MQ, is used for the normal signal net with $L = 800$ micron, $W = 4$ micron, and $S = 6$ micron. The third-bottom-layer metal, called M3, is used for the grounded interconnect (shield), and the second-top-layer, called MG, is used for twisting. To improve the reliability and reduce the resistance of vias, we used four 2×2 via arrays.

Figure 7 shows the four groups of interconnect structures we tested. Figure 7a shows 6-bit normal (NO) interconnects. In this case, the delay variation at each bit is determined by both the inductive-coupling return path and the capacitive-coupling length. Figure 7b shows 6 bits of coplanar (CO) interconnects with 3 bits of shielding. There are 6 bits of straight signal wires and 3 bits of shielding with the same wire length, width, and spacing. In this design, there are two groups each with three straight signal wires sharing two shields, and M3 for logic ground. Because multiple signals share only one shield, the results are a biased inductive return path, unequal capacitive coupling length, and, consequently, a non-uniform delay variation for the bit in the middle and at the boundary.

In addition, Figure 7c shows 6-bit twisted and normal (TN) interconnects with 2-bit shielding. There are 3-bit twisted signal wires, 3-bit straight signal wires, and 2-bit shielding. In this case, one normal group

Figure 6. Die diagram of the layout and delay measurement circuit.

has three straight wires and one shield, and one twisted group has three twisted wires and one shield, which is also twisted. Because twisting interweaves the polarity of flux, the twisted group cancels the mutual inductances of the normal group. However, the

Figure 7. Four groups of interconnect structures under test: 6-bit normal interconnects (a), 6-bit coplanar interconnects with 2-bit shielding (b), 6-bit twisted and normal interconnects with 2-bit shielding (c), and 6-bit twisted and staggered interconnects with 2-bit shielding (d).

Figure 8. Layout showing how to design a typical twist with use of two layers of metals and a via array.

shield distribution is still nonuniform in these two groups, so the delay variations are still significant.

Finally, Figure 7d shows 6-bit twisted and staggered (TS) interconnects with 2-bit shielding. There are two twisted groups, with each group having 3-bit twisted signal wires and 1-bit shield. In this design, the

shielding is uniformly distributed among signal nets to minimize both capacitive and inductive coupling. In addition, Figure 8 further shows how to design a typical twist layout with use of two layers of metals and one via array.

Test-generating circuits

In the actual test-chip design, we used three components to generate test signals: the decoder to select the aggressor and the victim, the control circuit for the switching pattern, and the driver with programmable driving strength. As Figure 9 shows, we first used the 3:8 decoder to select one from five aggressors. Then, each aggressor was enabled to switch by a pattern of 0 to 1 (rising) or 1 to 0 (falling), controlled by a preset 1:2 multiplexer, and the victim was disabled to stay at 0 (quiet). In addition, we could change the driver strength from $1\times$ to about $8\times$ by selecting three drivers in parallel with exponentially increasing widths (NMOS $W = 2.56$ microns, $W = 5.12$ microns, and $W = 10.24$ microns), which drove the interconnect structure under test.

Sampling circuits

When measuring a device's inductance in the frequency domain, both the impedance mismatch and the parasitic from the probe can impair the measurement's accuracy. Consequently, in our work, we measured delay through an on-chip sampling system by including test structures in the signal path of a ring oscillator and using an on-chip counter to record the delays.

We also used three components to sample the delay, as Figure 10 shows. The first component was the ring-oscillator consisting of the programmable driver and the receiver, connected into an odd stage of inverter chain with the selected victim in the signal path to be measured. The second component was the 16-bit synchronous counter, which directly counted the output of the ring-oscillator when enabled by an external fast-clock signal. The last component was the shift register, for serially shifting out the counter outputs when enabled by another external slow-clock signal.

By setting a different input switching pattern for aggressors, we measured the delay at one selected victim bit in the signal path. The delay, reflecting the impact from crosstalk, can be calculated as follows:

$$T_{\text{delay}} = \frac{t_{\text{Enable}}}{N_{\text{counter}}} \quad (11)$$

Figure 9. Schematic overview of the test-generating circuit.

Figure 10. Schematic overview of the sampling circuit.

where t_{Enable} is the enable time of the fast clock, and N_{counter} is the counter output shifted by the slow clock.

Our work focused chiefly on the design of a signal-net bundle, in which delay variation naturally differs from that found in a design for a pair of signals.³ The delay uncertainties we discuss, therefore, are defined as the mean and standard deviation of measured delays by iterating each bit as the victim from a group of 6-bit lines.

Measurement results

In our measurements, we used a Tektronix CSA 907A pattern generator to generate a 20-MHz sampling clock, an HP 8130A pulse generator to generate control for counter enabling and shifting, and an Agilent 8867 logic analyzer to measure counter output. The enabling time for the ring oscillator was 50.5 μs (with a 90-ms period), the reset time was 100 ns (with a 90-ms period), and the sampling clock was 8.15 MHz.

We investigated three different switching patterns, and selected the driver strength to be $1\times$. For the first switching pattern, all 6 bits switched from 0 to 1. As a result, there was no dynamic capacitive coupling, and the impact of inductive coupling was amplified. For the second switching pattern, two adjacent bits switched in the opposite direction. In this case, the inductive current could be returned locally by its neighbor, which reduced inductive coupling.

Dynamic capacitive coupling, however, was magnified because of the Miller effect. Therefore, we used the second switching pattern to study the impact of capacitive coupling. As for the third switching pattern, only one bit in each group switched; all other bits were quiet. Accordingly, we were able to study a combined inductive and capacitive coupling.

Tables 1, 2, and 3 summarize the counter outputs and extracted delays for the three switching patterns. Table 4 lists calculations for the mean delay and its standard deviation of 6 bits for the three switching patterns.

The results we achieved with switching-pattern 1, shown in Tables 1 and 4, show that the NO interconnect has the largest delay variation (0.07 ns) among the four groups. Capacitive coupling was minimized because all bits switched in the same direction. Because there were no local shields serving as the return paths, each bit had a different return path and hence a different loop inductance. As a result, the delay of each bit in the NO interconnect had the largest deviation. In contrast, the CO, TN, and TS interconnects provided similar (although among different bits) return paths for the inductive coupling. Their delay variations, therefore, were all similar and smaller than in the NO interconnect. The TS interconnects had the smallest mean delay (0.9 ns) and delay variation (1 ps).

Table 1. Measured counter outputs and delays of 6 bits by switching-pattern 1.

Type of interconnect	Delay (s)					
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5
NO	1.1067×10^{-9}	9.2942×10^{-10}	9.8144×10^{-10}	9.4500×10^{-10}	1.0103×10^{-9}	1.1036×10^{-9}
CO	9.3382×10^{-10}	9.1012×10^{-10}	8.9061×10^{-10}	8.8264×10^{-10}	9.1434×10^{-10}	9.3938×10^{-10}
TN	8.9262×10^{-10}	9.2506×10^{-10}	8.5490×10^{-10}	9.2182×10^{-10}	9.4614×10^{-10}	9.3715×10^{-10}
TS	8.7870×10^{-10}	8.7773×10^{-10}	8.7870×10^{-10}	8.7773×10^{-10}	8.7675×10^{-10}	8.76×10^{-10}

* NO: normal interconnect; CO: coplanar interconnect; TN: twisted and normal interconnect; TS: twisted and staggered interconnect

Table 2. Measured counter outputs and delays of 6 bits by switching-pattern 2.

Type of interconnect	Delay (s)					
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5
NO	1.0577×10^{-9}	1.1193×10^{-9}	1.0116×10^{-9}	1.0208×10^{-9}	1.1129×10^{-9}	1.0129×10^{-9}
CO	1.1129×10^{-9}	1.0026×10^{-9}	1.0410×10^{-9}	1.0301×10^{-9}	1.1098×10^{-9}	9.7658×10^{-10}
TN	9.2724×10^{-10}	9.0594×10^{-10}	9.1753×10^{-10}	9.5762×10^{-10}	9.2833×10^{-10}	1.0026×10^{-9}
TS	8.7481×10^{-10}	8.7384×10^{-10}	8.7968×10^{-10}	8.7675×10^{-10}	8.7287×10^{-10}	8.7384×10^{-10}

Table 3. Measured counter outputs and delays of 6 bits by switching-pattern 3.

Type of interconnect	Delay (s)					
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5
NO	1.0142×10^{-9}	9.2724×10^{-10}	8.6144×10^{-10}	8.9161×10^{-10}	1.0649×10^{-9}	9.9255×10^{-10}
CO	1.0795×10^{-9}	1.0929×10^{-9}	1.0634×10^{-9}	1.0929×10^{-9}	1.0975×10^{-9}	1.1193×10^{-9}
TN	8.6238×10^{-10}	8.1432×10^{-10}	9.2724×10^{-10}	9.6229×10^{-10}	9.6523×10^{-10}	9.3826×10^{-10}
TS	8.7287×10^{-10}	8.6332×10^{-10}	8.6712×10^{-10}	8.6712×10^{-10}	8.6903×10^{-10}	8.6616×10^{-10}

Table 4. Extracted mean delays and their variations of 6 bits from three switching patterns.

Type of interconnect	Switching-pattern 1		Switching-pattern 2		Switching-pattern 3	
	Standard		Standard		Standard	
	Mean (s)	deviation (s)	Mean (s)	deviation (s)	Mean (s)	deviation (s)
NO	1.0127×10^{-9}	7.6942×10^{-11}	1.0559×10^{-9}	4.9629×10^{-11}	9.5866×10^{-10}	7.8045×10^{-11}
CO	9.1182×10^{-10}	2.2601×10^{-11}	1.0455×10^{-9}	5.5723×10^{-11}	1.0909×10^{-9}	1.8678×10^{-11}
TN	9.1295×10^{-10}	3.3751×10^{-11}	9.3988×10^{-10}	3.5194×10^{-11}	9.1162×10^{-10}	6.0476×10^{-11}
TS	8.7756×10^{-10}	1.1385×10^{-12}	8.7530×10^{-10}	2.5177×10^{-12}	8.6760×10^{-10}	3.1834×10^{-12}

Tables 2 and 4 show the results for switching-pattern 2. The CO interconnect had the largest delay variation (0.06 ns) among the four groups. The capacitive coupling was maximized and each bit experienced a constant inductive coupling because two adjacent bits switched in the opposite direction. In addition, because the capacitive-coupling length differed significantly for the bit at the boundary and the bit in the middle,

each bit's delay in the CO interconnect had the largest deviation, larger than in the NO interconnect. In contrast, because the TS interconnect uniformly distributed the shields among 6 bits to minimize both the capacitive and inductive coupling, it had the smallest delay (0.9 ns) and delay variation (3 ps).

As for switching-pattern 3, as shown in Tables 3 and 4, the TN interconnect had a 0.06-ns delay variation,

Table 5. Measured counter outputs and delays of 6 bits by switching-pattern 3 with 8× driver strength.

Type of interconnect	Delay (s)					
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5
NO	3.2600×10^{-9}	3.1993×10^{-9}	3.1471×10^{-9}	3.1718×10^{-9}	3.2916×10^{-9}	3.2456×10^{-9}
CO	3.3002×10^{-9}	3.3081×10^{-9}	3.2907×10^{-9}	3.3081×10^{-9}	3.3107×10^{-9}	3.3230×10^{-9}
TN	3.1479×10^{-9}	3.1059×10^{-9}	3.1993×10^{-9}	3.2248×10^{-9}	3.2268×10^{-9}	3.2075×10^{-9}
TS	3.1566×10^{-9}	3.1487×10^{-9}	3.1519×10^{-9}	3.1519×10^{-9}	3.1535×10^{-9}	3.1511×10^{-9}

and the NO interconnect had a 0.08-ns delay variation. Unlike the previous two switching patterns, in this case each bit's delay variation was determined by both the inductive-coupling return path and the coupling length. Although the TN interconnect provided return paths to minimize the inductive coupling, the capacitive coupling between the twisted and normal groups and inside the normal group is still significant. Consequently, the delay of each bit in the TN interconnect had a large deviation (0.06 ns), similar to the NO interconnect (0.08 ns). In contrast, both the CO interconnect (0.02 ns) and the TS interconnect (3 ps) exhibited uniform delay variations. In addition, because the TS interconnect minimized the inductive coupling and also had a smaller capacitive-coupling length than the CO interconnect, it showed the smallest delay (0.9 ns). Table 5 also shows the delays and delay variations under switching-pattern 3 but with 8× driving strength. Because of the increased strength, 8× drivers have a higher tolerance to crosstalk than the 1× driver, so the delay and delay variations were of course smaller than those for 1× drivers.

By comparing the results of all three switching patterns, we see that the TS interconnect structure reduced delay by 25% and reduced delay variation by 25× compared to the CO interconnect structure. In addition, the TS interconnect structure reduced delay by 7.5% and reduced delay variation by 33× compared to the TN interconnect structure.

STAGGERED AND TWISTED signaling presents a fabrication challenge for multilevel nonglobal interconnects because it requires an extra metal level to twist the interconnects together. However, because most global interconnects such as data buses and clocks are usually designed with top-level metals, our proposed interconnect structure still seems promising for intra- and interchip communication with many signal or clock nets. Such a staggered and twisted interconnect (TSS) structure is particularly suitable

for data communication in the design of CMPs. To fully utilize the proposed TSS interconnect structure in high-performance designs, more detailed studies are needed. For example, how can we optimally insert buffers for this kind of interconnect? Research is also needed to design a test chip with different interconnect structures and to test the delay variation impacted by the fabrication process. ■

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