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Impact of Programming Mechanisms on the Performance and Reliability of Nonvolatile Memory Devices Based on Si Nanocrystals

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Abstract—A nonvolatile memory based on silicon nanocrystals (nc-Si) synthesized with very-low-energy Si^+ implantation is fabricated, and the memory performance under the programming/erasing of either Fowler–Nordheim (FN)/FN or channel hot electron (CHE)/FN at both room temperature and 85 °C is investigated. The CHE programming has a larger memory window, a better endurance, and a longer retention time as compared to FN programming. In addition, the CHE programming yields less stress-induced leakage current than FN programming, suggesting that it produces less damage to the gate oxide and the oxide/Si interface. Detailed discussions on the impact of the programming mechanisms are presented.

Index Terms—Channel-hot-electron (CHE) injection, Fowler–Nordheim (FN) injection, memory device, silicon nanocrystal (nc-Si).

I. INTRODUCTION

SILICON nanocrystals (nc-Si) embedded in the gate oxide of MOS structures is promising for the application of nonvolatile memories (NVMs) [1]–[4]. Conventional NVMs can be programmed by using channel-hot-electron (CHE) injection [5]–[7] or Fowler–Nordheim (FN) tunneling [8], [9], but they are usually erased by FN tunneling regardless of the programming mechanisms [7]–[9]. For the NVMs based on nc-Si, the programming/erasing (P/E) operations by the FN/FN mechanism [10], [11] or the CHE/FN mechanism have been reported [4], [11]–[13]. However, there are no detailed studies reported on the impact of the programming mechanisms on the performance and reliability of the nc-Si-based NVMs. In this paper, we have fabricated NVM devices based on nc-Si synthesized with very-low-energy Si ion implantation, and we have examined the influence of the programming mechanisms including the FN and the CHE on the memory window, endurance, and charge retention of the fabricated memory devices.

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Fig. 1. Cross-sectional TEM image of the memory device.

II. EXPERIMENT

Except the additional steps for the nc-Si synthesis, the memory devices with nc-Si embedded in the gate oxide are fabricated on 6-in p-type (100) Si wafers with a conventional 2- μm CMOS process. An SiO_2 film is thermally grown to 17 nm on the p-type Si (100) substrate in dry oxygen at 950 °C. Si^+ ions with a dose of $5 \times 10^{16} \text{ cm}^{-2}$ are then implanted at 2 keV into the oxide. An additional 20-nm SiO_2 is deposited on top of the previously grown 17-nm SiO_2 by a low-pressure chemical vapor deposition (LPCVD) method. Thermal annealing is carried out at 1000 °C in N_2 ambient for 1 h to induce nc-Si formation. Fig. 1 shows the cross-sectional high-resolution transmission electron microscopy (TEM) image of the memory device. As can be seen from the TEM image, the memory devices have a tunnel oxide of $\sim 3 \text{ nm}$. The mean size of the nc-Si determined from the full-width at half-maximum of the Bragg peak of the X-ray-diffraction spectrum after correction for instrumental broadening is $\sim 4 \text{ nm}$. Electrical characterization is performed on the devices with a channel width/length (W/L) of $10 \mu\text{m}/2 \mu\text{m}$ with an HP4156A semiconductor parameter analyzer at both the room temperature and the hot temperature of 85 °C. The programming and erasing operations are carried out with an HP16440A pulse generator together with the HP4156A.

To program the memory devices, electrons are injected into the nc-Si from the channel by either CHE or FN mechanisms. For the CHE programming, a positive voltage is applied

Fig. 2. Transfer characteristics of the programmed and erased states under the P/E operation of (a) FN/FN or (b) CHE/FN. The P/E time is $1 \mu\text{s}$.

to both the gate and the drain (i.e., the gate voltage $V_g =$ the drain voltage $V_d > 0$) while both the source and substrate are grounded. For the FN programming, a positive voltage is applied to the gate (i.e., $V_g > 0$) while the other three terminals are grounded. To erase the memory devices, the electrons trapped in the nc-Si are expelled by the FN mechanism. For the FN erasing, a negative voltage is applied to the gate (i.e., $V_g < 0$) while all the other terminals are grounded. In the following discussions, “FN/FN” and “CHE/FN” denote the operations of FN programming/FN erasing and CHE programming/FN erasing, respectively.

III. RESULT AND DISCUSSION

Fig. 2(a) shows the shift of transfer characteristics of the device at room temperature under the FN/FN ($V_g = +10$ V for programming and $V_g = -10$ V for erasing) for $1 \mu\text{s}$. For comparison, the transfer characteristics under the CHE/FN ($V_g = V_d = +10$ V for programming and $V_g = -10$ V for erasing) for $1 \mu\text{s}$ are shown in Fig. 2(b). As can be seen from the figure, the FN/FN leads to a memory window of ~ 0.75 V, while the CHE/FN yields a memory window of ~ 1 V. It is observed that a larger memory window is always achieved by the CHE/FN than by the FN/FN for the same voltage magnitude and time of P/E. This situation is also clearly demonstrated by Fig. 3, which shows the memory window as a function of

Fig. 3. Memory window as a function of the magnitude of the P/E voltage for the FN/FN and the CHE/FN operations.

the program/erase voltage at room temperature for both the CHE/FN and the FN/FN. The P/E time is fixed at $1 \mu\text{s}$. It is evident from this figure that the CHE/FN leads to a larger memory window as compared to the FN/FN for any P/E voltage. A larger memory window is actually the consequence of a larger threshold-voltage shift caused by programming (i.e., a larger V_{th} at the programmed state) and a lower threshold voltage after erasing (i.e., a lower V_{th} at the erased state) in the CHE/FN operation, as discussed in the following.

As can be seen in Fig. 4, the CHE programming causes a larger threshold-voltage shift as compared to the FN programming. Under the CHE programming, the CHEs are generated by the lateral electric field near the drain junction. The generated hot electrons are injected into the nanocrystals and the gate oxide near the drain junction, leading to local charge trapping near the drain. This situation is similar to that observed for conventional NVMs [5]–[7]. In contrast, under the FN programming, electrons are injected from the Si substrate into the nanocrystals and the gate oxide over the channel, leading to charge trapping with an almost uniform lateral distribution over the whole channel. The difference in the distribution of trapped charges between the two programming mechanisms can explain the larger threshold-voltage shift caused by the CHE programming. In this paper, the threshold voltage is measured by reading the drain current with the source grounded (i.e., forward reading). With this measurement configuration, the threshold voltage is sensitive to the charge trapping near the drain, and it is larger for a larger amount of localized charge trapping near the drain. Therefore, the CHE programming can yield a larger threshold-voltage shift, as it can cause more charge trapping near the drain. On the other hand, as will be discussed later, the FN programming has more electrons trapped in the control oxide as compared to the CHE programming. The threshold-voltage shift due to the electron trapping in the control oxide should be not large, because the trapped electrons are far away from the channel. This may also be partially responsible for the relatively smaller threshold-voltage shift caused by the FN programming.

It is also evident in Fig. 4 that the threshold voltage after erasing (i.e., the V_{th} at the erased state) in the CHE/FN operation is lower than that in the FN/FN operation. As discussed

Fig. 4. Endurance characteristics for the CHE/FN and the FN/FN at (a) room temperature and at (b) 85 °C.

above, in the CHE/FN operation, the CHE programming leads to the localized charge trapping near the drain. However, during the FN erasing, the entire nc-Si layer is erased. In other words, the trapped charges in the region near the drain are removed; however, at the same time, electron tunneling from the nc-Si of all other regions to the Si substrate can occur under the influence of the uniform oxide electric field produced by the negative gate bias. This over erase leads to a lower V_{th} at the erased state. Actually, the over erase is evident from the fact that the initial V_{th} before any P/E is ~ 1.75 V, but the V_{th} decreases to ~ 1.65 V after a CHE programming. In contrast, in the FN/FN operation, both the charging trapping and the charge erasing are laterally uniform; thus, there is no over erase occurring.

Fig. 4 also shows the endurance characteristics of the memory device. For the endurance measurement, the voltage magnitude and the duration of P/E are 10 V and 1 μ s, respectively, for both the FN/FN and the CHE/FN. At room temperature, the threshold voltage (V_{th}) starts to drift up after 10⁴ and 10⁵ P/E cycles for the FN/FN and the CHE/FN, respectively. After 10⁶ P/E cycles, the FN programming shows a V_{th} drift-up of ~ 0.13 V, while the CHE programming shows a drift-up of only ~ 0.05 V. At the hot temperature of 85 °C, the V_{th} drift-up is more significant, and 0.25- and 0.13-V drift-up after 10⁶ P/E cycles are observed for the FN/FN and the CHE/FN, respectively. The drift-up in the V_{th} is attributed to the electron trapping in the control oxide. The nc-Si has a smaller capture

Fig. 5. Retention characteristics for the CHE/FN and the FN/FN at (a) room temperature and at (b) 85 °C.

cross section as compared to the continuous polysilicon floating gate; hence, a portion of the injected electrons from the channel are captured by the nc-Si while the rest are trapped in the control oxide [4]. During the erase process, an incomplete removal of the trapped electrons from the control oxide leads to an increase in the threshold voltage, and this effect is enhanced at a higher temperature. The more significant V_{th} drift-up in the FN/FN operation indicates that the FN programming leads to more electrons trapped in the control oxide than the CHE programming.

Fig. 5 shows the retention characteristics of the memory devices at room temperature [Fig. 5(a)] and at 85 °C [Fig. 5(b)]. The retention measurement was carried out after 1000 P/E cycles. It is observed from the figure that the charge retention for the CHE programming is better than that for the FN programming. For the programmed state at room temperature, $\sim 50\%$ and $\sim 70\%$ charge losses after ten years are expected for the CHE and the FN programming, respectively. The better charge retention is related to the localized charge trapping caused by the CHE programming. As discussed earlier, the trapped charges are distributed uniformly in the entire nc-Si layer for the FN programming, but the charge trapping is highly localized near the drain for the CHE programming. As such, the cross section (or area) for electron tunneling out from the nc-Si to the channel during the retention experiment should be much smaller for the latter case. This means that the charge loss is less in the case of the CHE programming. For the V_{th} at the erased

Fig. 6. Gate current before and after 10^4 P/E cycles for (a) the FN/FN and (b) the CHE/FN.

state at room temperature and for the case of FN/FN, it remains unchanged with time, showing no charge transfer during the retention experiment. However, for the case of CHE/FN, it starts to increase at the time of 10^4 s from ~ 1.65 V with a trend toward the initial value (i.e., the V_{th} before any P/E) of ~ 1.75 V, indicating the recovery from the over erase that has been discussed earlier. At room temperature, the expected memory window after ten years is ~ 0.5 V for the CHE/FN, which meets the retention requirement of NVMs. However, it is only ~ 0.2 V for the FN/FN. At the hot temperature of 85°C , the retention capability degrades significantly for both the CHE/FN and the FN/FN due to the enhancement of thermal tunneling of electrons from the nc-Si; however, for the CHE/FN, the expected memory window after 10 years is still larger than 0.3 V, which could be sufficient for proper memory functioning.

It is also observed that the CHE programming leads to fewer damages to the gate oxide and the oxide/Si interface. Fig. 6 shows the gate leakage currents before and after 10^4 P/E cycles for both the FN programming [Fig. 6(a)] and the CHE programming [Fig. 6(b)]. For the FN programming, a significant stress-induced leakage current (SILC) is observed after 10^4 P/E cycles. The SILC at low gate voltage ($< \sim 3$ V) is attributed to the displacement current associated with the interface traps and the oxide traps near the interface that are generated by the FN injection, while the SILC at high gate voltage ($> \sim 3$ V) can be explained in terms of the oxide-trap-assisted tunneling [14]. In contrast to the FN programming, the CHE programming leads to an insignificant SILC after

10^4 P/E cycles. Therefore, it is evident that the CHE programming produces fewer damages to the oxide and the interface and thus has a better reliability than the FN programming.

IV. CONCLUSION

In this paper, an NVM based on nc-Si synthesized with very-low-energy Si^+ implantation has been fabricated, and the memory performance under the P/E mechanism of either FN/FN or CHE/FN at both room temperature and 85°C has been evaluated. The impact of the FN programming and the CHE programming on the memory performance and reliability has been investigated. It is shown that, as compared to the FN programming, the CHE programming has a larger memory window, a better endurance and a longer retention time. In addition, the CHE programming does not produce a significant SILC, while the leakage current is significant for the FN programming. This suggests that the CHE programming produces fewer damages to the gate oxide and the oxide/Si interface than the FN programming. Explanations on the difference between the CHE programming and the FN programming are given.

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