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2009

Qiu, X., Siek, L., & Tiew, K. T. (2009). System-level design of a delta-sigma modulator target for next generation wireless application. In Proceedings of the IEEE International Symposium on Radio-Frequency Integration Technology(pp.303-306).

<https://hdl.handle.net/10356/90664>

<https://doi.org/10.1109/RFIT.2009.5383676>

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System-level Design of a Delta-Sigma Modulator Target for Next Generation Wireless Application

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ABSTRACT — Delta-sigma ($\Delta\Sigma$) converters have been widely used in wireless communications as they provide the most economic speed-accuracy tradeoff. This paper presents the system-level design of a multi-bit continuous-time (CT) $\Delta\Sigma$ analog-to-digital converter (ADC) targeting for the next generation wireless application. The modulator topology is determined based on the application requirements using MATLAB software. The nonidealities associated with the multi-bit CT $\Delta\Sigma$ modulator, such as excess loop delay, system clock jitter, integrator nonideality and multi-bit digital-to-analog converter (DAC) element mismatch, are also modeled in the system-level. With all the nonidealities included, the designed modulator achieves a dynamic range (DR) of 74dB (12 bits) in a 50-MHz signal bandwidth.

Index Terms — Analog-to-digital converter (ADC), continuous-time (CT), delta-sigma ($\Delta\Sigma$) modulation, multi-bit, system-level.

I. INTRODUCTION

Due to the increasing digital processing speed in the DSP, communication data is transferred in a channel bandwidth of 20 MHz according to the IEEE 802.11e standard [1]. It is reasonable to believe that the signal bandwidth of the next generation wireless applications will be much higher than current one, which stimulates the requirement for high-speed building blocks. One of the key blocks in the front-end of the WLAN receiver is the analog-to-digital converter (ADC). As a result, there is a stronger need for high resolution, high speed ADCs.

Comparing to other types of ADCs, delta-sigma ($\Delta\Sigma$) oversampling ADCs are preferred for this application because they provide the most economic speed-accuracy tradeoff [2]. Due to the severe requirement in amplifier bandwidth, discrete-time (DT) $\Delta\Sigma$ ADCs are less suitable for high-speed applications. While for continuous-time (CT) implementation, besides the possible higher sampling rates, it provides additional benefits: no need for sample-and-hold in front, inherent anti-aliasing function and lower circuit noise generated by the loop filter. Even though it suffers more from excess loop delay and clock jitter problems, solutions have already been proposed [3]. Multi-bit continuous-time $\Delta\Sigma$ ADCs are even more suitable for broadband communications. The internal multi-bit quantizer reduces the sampling frequency and the clock jitter effect. Moreover, the modulator stability is also improved.

This work presents the system-level design of a fifth-order multi-bit CT $\Delta\Sigma$ ADC for next generation wireless application in MATLAB environment. With block nonidealities incorporated, the target data conversion bandwidth is 50 MHz with dynamic range (DR) of 74 dB, which is sufficient for wireless communications. The oversampling ratio (OSR) is determined to be 8 and a 4-bit internal quantizer is used to improve the peak signal-to-noise ratio (SNR) and modulator stability.

This paper is organized as follows. Section II describes the system-level design steps for the modulator. In section III, the block nonidealities are discussed and modeled. Section IV presents the modulator performance when all the nonidealities are considered. Finally, conclusions are drawn in section V.

II. SYSTEM-LEVEL DESIGN

A. System-level Parameter

Due to large loop coefficients variations, single-stage topology is preferred to multi-stage one for CT $\Delta\Sigma$ modulators. The sampling rate is limited by the maximum device speed. For deep submicron CMOS process, 800 MHz is a reasonable upper limit for the modulator sampling rate considering the gain-bandwidth requirement of the opamp and for a given power consumption. Generally speaking, the higher the modulator order, the higher the peak SNR. However, the loop stability problem often limits the order. Usually, the order should be no more than 5. An effective method to reduce the in-band quantization noise power is by using multi-bit internal quantizer. Each additional quantizer bit will improve the DR by around 6 dB. In addition, it also introduces other benefits: more aggressive noise transfer function can be implemented; the modulator loop stability is improved; the clock jitter effect can be reduced if a non-return-to-zero (NRZ) multi-bit digital-to-analog converter (DAC) is used in the feedback path. However, the power consumption of the quantizer increases proportionally to the number of quantization levels. So the quantizer bits should be optimized to get the best tradeoff between the modulator performance and the power consumption. The noise-transfer-function (NTF) out-of-band gain (OOBG) is another important factor that affects the modulator performance; the higher the NTF OOBG, the higher the

peak SNR. However, the modulator becomes less stable. Based on extensive simulations and analysis, a fifth-order 4-bit single-stage topology is chosen with an OSR of 8. The NTF OOBG is set at 3.5 and the peak SNR is set to be 80 dB for 6 dB safety margin.

B. Loop-filter Topology

For delta-sigma modulators two architectures are commonly used: feedback (FB) and feed-forward (FF). The FB topology is less suitable for low-voltage, deep submicron technology implementation due to the large signal swing at the output of the first stage opamp. Whereas for FF architecture, the output swing of the first stage is much smaller, meaning that the gain of the first stage can be designed larger and hence performance requirements on the following stages can be relaxed. However, the FF topology has a drawback. There is an unavoidable out-of-band peaking in its signal transfer function (STF). This peak may reduce the modulator dynamic range in case of wireless applications if a lot of out-of-band interferences exist. A lot of methods have already been proposed to solve this problem[4]. According to [4] extra feed-in and feed-forward branches can be added to cancel the peaking effect and reduce the STF sensitivity to the coefficient mismatches.

In this design, NRZ DAC is used to reduce the clock jitter effect. Using the NRZ DAC, the tolerable excess loop delay is only about 16% of the sampling period T_s . To solve the excess loop delay problem, an explicit one-period delay is inserted to absorb the varying excess loop delay and a second feedback path is added to the input of the quantizer to make the impulse response equivalent to its DT counterpart, as proposed in [3]. The block diagram of such a designed modulator is shown in Fig. 1, where branches b_i and c_f are added to remove the peak in the STF.

Fig. 1. CT $\Delta\Sigma$ modulator with additional feedback path to alleviating excess loop delay effect.

C. Loop-filter Coefficient Assignment

Using the well-developed delta-sigma MATLAB toolbox written by Richard Schreier [5], the NTF of the

DT counterpart modulator can be determined as shown by (1), whose zeros are optimized to suppress the in-band quantization noise.

$$NTF(z) = \frac{(z-1)(z^2-1.995z+1)(z^2-1.875z+1)}{(z-0.4616)(z^2-0.9456z+0.2747)(z^2-1.108z+0.5907)} \quad (1)$$

Based on the NTF equation, the loop-filter transfer function can be derived as below:

$$L_1(z) = \frac{2.3149(z^2-1.387z+0.5051)(z^2-1.48z+0.7912)}{(z-1)(z^2-1.955z+1)(z^2-1.875z+1)} \quad (2)$$

For the modified cascade-of-integrators feed-forward (CIFF) architecture with additional feedback DAC, $L_i(z)$ is decomposed as shown by (3), where k is the gain of the extra feedback DAC2 and $L_{i_new}(z)$ represents the loop filter transfer function after the delay introduced. The expression for $L_{i_new}(z)$ is shown by (4).

$$L_1(z) = L_{i_new}(z) \times z^{-1} + k \times z^{-1} \quad (3)$$

$$L_{i_new}(z) = \frac{4.546z^{-1}-14.23z^{-2}+17.71z^{-3}-10.26z^{-4}+2.315z^{-5}}{1-4.83z^{-1}+9.496z^{-2}-9.496z^{-3}+4.83z^{-4}-z^{-5}} \quad (4)$$

Impulse Invariant Transform is a popular method to transfer the DT equation to its equivalent CT counterpart. However, this method incorporates large amounts of mathematical equations, which may easily introduce calculation errors. In this design, since NRZ DAC is used in the feedback path, the *d2cm* function provided by MATLAB is used to make the conversion easier. The CT version of $L_{i_new}(z)$ is shown by (5). The frequency responses of $L_0(s)$, STF and NTF are shown in Fig. 2.

$$L_0(s) = \frac{-0.0786(s-10.28)(s^2+0.8871s+0.4636)}{s(s^2+0.04471)(s^2+0.1266)} \quad (5)$$

Fig. 2. Frequency response of STF, NTF and L_0 .

The CT loop filter parametric equation can be derived from the system level architecture. By comparing the parametric equation and (5), the gains and coefficients can be computed. Since there are fifteen variables and seven equations, eight of them are assigned the initial values to solve the others. However, with these coefficients, the outputs of integrators may overflow and the modulator performance will be degraded. Dynamic scaling is

performed according to the method proposed in [6] while considering the power consumption optimization.

III. BLOCK NONIDEALITIES

A. Finite Integrator DC Gain

Due to power consumption and linearity consideration for high-speed applications, the first integrator is implemented with RC-integrator topology and the second to fifth integrators used GmC-integrator structure. In deep submicron applications, the opamp gain can seldom be boosted up to 60 dB and the transconductors usually have finite output impedances. Using the finite gain models, the minimum gain requirements on integrators can be found out as shown in Table I.

TABLE I
MINIMUM DC GAIN REQUIREMENTS OF INTEGRATORS

First Integrator minimum DC gain	40 dB
Second Integrator minimum DC gain	30 dB
Third Integrator minimum DC gain	15 dB
Forth Integrator minimum DC gain	15 dB
Fifth Integrator minimum DC gain	10 dB

B. Finite Opamp Gain Bandwidth Product (GBW)

In reality, the opamp has finite GBW due to its finite gain and poles and zeros in its transfer function. According to [7], the RC-integrator can be modeled by an ideal integrator cascaded by a single-pole system, based on which, the SNR versus opamp GBW plot with -3 dB full scale input is shown in Fig 3. To ensure the SNR drop within 3 dB, the GBW of the first integrator opamp has to be around three times the sampling frequency (f_s).

Fig. 3. SNR versus GBW with -3 dB full scale input.

C. RC Time Constant Variation

In CMOS process, the RC time constant could vary by as much as $\pm 30\%$ and this variation will be directly translated into the loop filter coefficients, which may make the modulator unstable and degrade the system

performance, as shown by the MATLAB simulation result in Fig. 4. The acceptable range of variation is from -8% to 12% of the RC time constant if 3 dB SNDR degradation is tolerable.

Fig. 4. SNR versus RC time constant variation with -3 dB full scale input.

D. Clock Jitter Effect

The timing error of the feedback signal transition edges caused by the DAC clock jitter is the same as the feedback signal error itself, which appears at the modulator output without any attenuation and hence degrade the modulator performance. To simulate the effect of clock jitter, a random error was added to the feedback signal to model the error caused by the DAC clock jitter. After then, a series of simulations were performed and the results are shown in Fig. 5, where the SNR is plotted against the clock jitter at -3 dB of full scale input. The higher the clock jitter, the lower the peak SNDR. If 3 dB degradation of SNR is allowable, the clock jitter cannot be higher than $0.08\%T_s$, which is 1 ps.

Fig. 5. SNR versus clock jitter with -3dB full scale input.

E. DAC Non-linearity

The multi-bit DAC mismatch error will appear at the modulator output without any attenuation, so the modulator linearity cannot be higher than that of the DAC. As a result, it is a limiting factor for the system

performance. Some methods have already been exploited to improve the DAC linearity, such as the dynamic element matching (DEM) and digital calibration [3]. Using the DEM method, the acceptable mismatch error is at most 0.1%, as shown by Fig. 6.

Fig. 6. PSD plot for DAC pulses.

IV. RESULTS

The nonidealities, except the minimum gain requirements of integrators, are summarized in Table II. They are all included to test the modulator performance. The input range is swept across the entire dynamic range to evaluate the SNR performance, as shown in Fig. 7. The dynamic range is 74 dB (12 bits) and the peak SNR is around 74 dB. The PSD plot for the modulator is also shown in Fig. 8.

TABLE II
NONIDEALITIES SUMMARY

Modulator Nonidealities	Value
Excess loop delay	T_s
First integrator opamp GBW	$3f_s$
RC constant variation range	-8%-12%
Clock jitter	$0.08\%T_s$
DAC mismatch error	0.1%

Fig. 7. SNR versus full dynamic range.

Fig. 8. PSD plot for modulators

V. CONCLUSION

The system-level design of a high-speed multi-bit continuous-time $\Delta\Sigma$ ADC is presented for the next generation wireless applications where the data conversion bandwidth can be as high as 50 MHz. To remove the STF peak and minimize the excess loop delay effect, the typical FF modulator architecture is modified. In this work, various block nonidealities are discussed and modeled to check the effect on the modulator performance. With all the nonidealities included, the modulator achieves a resolution of 12 bits with a signal bandwidth of 50 MHz.

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance and support of Chartered Semiconductor Manufacturing Ltd.

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