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Sub-mW Multi-GHz CMOS Dual-Modulus Prescalers Based on Programmable Injection-Locked Frequency Dividers

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ABSTRACT —Dual-modulus prescalers based on programmable Injection-Locked Frequency Dividers (ILFDs) are presented. With a multi-phase injection, variable division ratios are obtained by simply switching different number of input signals. Implemented in a 0.18 μ m CMOS process, the 4/5 dual-modulus prescaler achieves an operating range of 1.8-6GHz with 0.22mW measured power consumption from a 1V supply. Based on the same architecture, a 0.15mW 5GHz 2/3 dual-modulus prescaler and a 0.29mW 5.5GHz 8/9 dual-modulus prescaler are also demonstrated.

Index Terms —Dual-Modulus, Frequency Divider, Injection Locked, Prescaler.

I. INTRODUCTION

The high-speed frequency divider is a key block in frequency synthesizer for wireless communications. Dual-modulus prescalers are widely utilized in phase-locked frequency synthesizers to obtain programmable frequency division ratio. A dual-modulus prescaler usually consists of a divide-by- $N/N+1$ unit and several asynchronous divide-by-2 units [1]. Alternatively, the phase switching technique might be utilized to obtain dual-modulus dividing without divide-by- $N/N+1$ divider [2-3]. The high-speed multi-GHz prescaler usually consumes the largest portion of power in the frequency synthesizer because the prescaler is usually implemented with digital circuits with large power consumption at GHz range. In the design of multi-GHz high-speed prescalers, dividers based on the MOS Current Mode Logic (MCML) or the dynamic logic circuits are frequently used for their wide input frequency range and stable operation [2-4]. On the other hand, Injection-Locked Frequency Dividers (ILFDs) can usually achieve a higher operating frequency with lower power consumption [5-7]. However, conventional ILFDs are rarely utilized in prescalers due to their small input frequency locking range, limited output swing, and more importantly, non-programmable division ratio. The fixed division ratio of conventional ILFDs is the main reason for their limited applications in the design of high speed prescalers since dual-modulus dividers are not readily available using ILFDs, even the divide-by-2 or

divide-by-3 ILFD has been proposed in [6-7]. This restricts the usage of ILFDs in the frequency divider. For example, the ILFD pre-divide-by-2 makes the overall division ratio to be the multiplexer of two [5]. Hence, an ILFD with programmable division ratio is highly desired in the design of low power wide range high-speed frequency divider.

Fig. 1. The model of ILFD

II. MULTI-PHASE ILFD

An ILFD usually consists of an injector (mixer) and a filter (usually an oscillator). Fig. 1 shows the general model for an ILFD. The division ratio is determined by the order of the harmonic sustained by the oscillator. The oscillator can be an LC oscillator or a ring oscillator. The LC oscillator has a high Q and hence a small operating range. The ring oscillator usually has a low Q and a large operating range. ILFDs based on either oscillator have considerably higher operating frequencies than conventional digital frequency dividers. However, ILFDs based on the ring oscillator usually have smaller silicon area and larger output swing [6-7]. In nowadays commercial wireless communications standards, which are usually below 6 GHz, the ring oscillator based ILFD is more attractive for its wider tuning range which is suitable for multi-standards operations.

To design a dual-modulus prescaler based on ILFDs, it is intuitive to have an investigation of behavior of frequency division in ILFDs. Until now, the reported ILFDs are with a fixed division, most of them are divide-by-2 or divide-by-3. The division ratios of the ILFD is

based on the production of high order of signal mixing. Fig. 2 shows the operation of an ILFD based on N-stage

Fig. 2. The divide-by-N ILFD based on ring oscillator

ring oscillator. It is based on a ring oscillator which is formed by several stages of delay cells. The total phase shift for the N delay stages must be $360 \times n + 180$ degree

Fig. 3. The N stage signal mixing

and a sufficient gain must be maintained for the loop, where n is an integer. For example, if the number of stage is 3, each stage causes a phase delay of 180 degree to maintain oscillation. The total delay in phase is 540 degree. This also implies that the N should be an odd number to sustain the self-oscillation for inverter based ring oscillator.

In [6], the analysis of this circuit is based on voltage signals. However, it can be obviously seen that the currents of each stage are mixed/summed at the tail transistor which produces the divide-by-N operation.

Fig. 3 shows the mixing of currents from each stage at the tail transistor. For simplicity, it is assumed all the transistors are identical.

In the case of three stages, in order to achieve the sustained oscillation, the currents at each stage have to be $\sin(\omega t)$, $\sin(\omega t + 120)$ and $\sin(\omega t + 240)$, respectively.

The injected tail current I_{inj} , which is the sum of the currents from each stage, will then contain mostly the 3rd harmonic $\sin(3\omega t)$, since the lower harmonics are cancelled with 120 degree of phase delay at each stage. Therefore, the divide-by-3 operation is obtained for the injected tail current at each stage. Similarly, the divide-by-N operation can be obtained for the injected tail current if each stage produces a current with a phase delay of $360/N$ degree. The number of the oscillator's stages with injected signals determines the division ratio of the ILFD.

III. DESIGN OF DUAL-MODULUES PRESCALERS

From the above analysis, it is obvious that a feasible implementation of dual-modulus or multi-modulus operation of ILFD is to switch the phase delay at each stage. This can be done by simply switching the number of oscillator stages with the injected signal. Therefore, the programmability of the ILFD can be realized simply by injecting signals to different numbers of oscillator's stages, e.g., N stages for N division ratio or $N+1$ stages for $N+1$ division ratio. Moreover, the total number of ring oscillator stages must maintain an odd number during the switching in order to achieve sustained oscillation. This can be easily done with a MOSFET switch to achieve a programmable or dual-modulus ILFD with ultra-low power consumption.

Fig. 4. The proposed programmable ILFD

The proposed dual-modulus prescaler based on the programmable ILFD is shown in Fig. 4. The programmable ILFD consists of an $(N+1)$ -stage ring oscillator, where N is an even number. The first N stages of the ring oscillator are directly injected with the input signal f_{in} while the last stage of the ring oscillator has an additional modulus control (MC) switch to gate the feeding of f_{in} . When the modulus control (MC) switch is set to logic high, the input signal f_{in} is injected to all $N+1$

stages of the ring oscillator and an (N+1)-phase harmonic injection locked divider with an odd division ratio of N+1 is realized [4]. When the modulus control (MC) switch is set to logic low, the last stage the ring oscillator becomes an inverter and thus an N-phase harmonic injection locked divider with an even division ratio of N is realized. By simply changing the modulus control (MC) switch, the dual-modulus operation, i.e., divide-by-N/(N+1), is achieved. Furthermore, if we add modulus control (MC) switches in more stages of the ring oscillator, triple- (N-1/N/N+1) or quad-modulus (N-2/N-1/N/N+1) operation is readily obtained for multi-band multi-mode applications. This means that we can easily obtain multi-modulus for example divide-by-2/3, 4/5 and 8/9. The only difference is the change of the delay stages.

Conventionally, if we need to obtain a large division ratio for example divide-by-8/9, a divide-by-2/3 unit with two stage of divide-by-2 and several logic gates are needed as shown in Fig.5. The proposed topology has a much simpler circuit and lower power consumption than the conventional designs. For example, the conventional designs usually need more than 50 transistors to perform the divide-by-8/9 operations, but in the proposed design, only 19 transistors are needed.

To verify the proposed topology, several test chips, including the divide-by-2/3, divide-by-4/5 and divide-by-8/9 prescalers, using the proposed designs are fabricated using a standard 0.18 μm CMOS process. They are of identical configuration except the number of delay stages.

Fig. 5. The divide-by-8/9 prescaler and divide-by-2/3 unit in [1]

Fig. 6. The die photo of the proposed divide-by-4/5 prescaler

VI. MEASUREMENT RESULTS

Fabricated in a standard 0.18 μm CMOS process, all three dual-modulus prescalers have a small silicon footprint of less than $20\mu\text{m} \times 20\mu\text{m}$. The die micrograph of the 4/5 dual-modulus prescaler is shown in Fig. 6 and it is measured about $300\mu\text{m} \times 300\mu\text{m}$ including the testing buffers and pads.

All measurements were carried out on-wafer using a probe station. The input signal is provided from the Agilent 20GHz signal generator, while the output is captured by an oscilloscope.

For the divide-by-4/5 dual-modulus prescaler based on the proposed topology, the maximum operating frequency is measured at 6GHz while the minimum operating frequency is 1.8GHz with an injected input power of 5dBm. The 4/5 dual-modulus prescaler dissipates 0.22mW from a 1V supply when operating at 6GHz, which is an order of magnitude better than any previously published work. Its measured output transient waveform for a 6GHz

Fig. 7. output transient waveform of divide-by-4/5 with 6GHz input

input is shown in Fig. 7. When injecting a 5GHz signal, the measured phase noise is -92.9dBc at 10kHz offset. A 2/3 and an 8/9 dual-modulus prescaler based on the same topology were also implemented with their measured operating frequency range shown in Fig. 8. As shown in Fig. 9, their power consumptions increase linearly proportional to their operating frequencies. Table 1 summarizes the measured performance of three proposed dual-modulus prescalers, compared with previously published work in terms of operating frequency range, division ratio, and power consumption.

Fig. 8. The N stage signal mixing

VII. CONCLUSION

The programmable ILFD is proposed based on ring oscillators for the first time. By switching of different number of stages with injected signals, programmable division ratios are achieved. With the programmable ILFD, ultra-low power small size dual-modulus prescalers with wide-range operation are obtained. Several prototypes

Fig. 9. The power consumption vs. operating frequency

were fabricated using a standard 0.18 μm CMOS process. Measured operating frequencies from 1.8 GHz to 6 GHz are obtained for divide-by-4/5 with a maximum power consumption of 0.22 mW. The divide-by-2/3 and divide-by-8/9 operations using the same topology are also silicon-verified.

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Work	Vdd(V)	Process (μm)	Freq. (GHz)	Division Ratio	Power mW
[1]	1.8	0.25	2.8	8/9	3
[2]	2.2	0.25	5.5	220-224	59
[4]	1.8	0.25	2	128/129	0.48
[5]	1.8	0.18	10	8/9	11.7
This	1	0.18	1.8-6	4/5	0.22
This	1	0.18	1.8-5.5	8/9	0.29
This	1	0.18	2-5	2/3	0.15

Table 1 Performance summary and comparison

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