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Passive Circuit Designs toward Terahertz using Nanometer CMOS Technology

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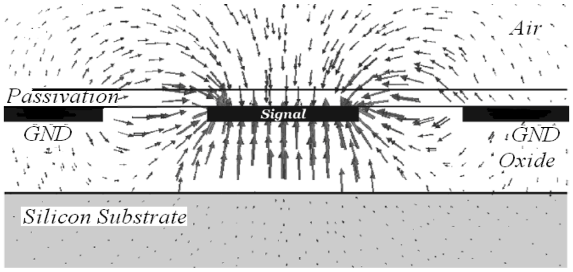
***Abstract*— This paper presents terahertz passive circuit design and investigation by using a 180 nanometer CMOS technology. A novel multimode bandpass filter and a power divider are designed by adopting a thin-film microstrip line, which uses silicon oxide layer of CMOS as the microstrip substrate. The circuit and full-wave electromagnetic results show that the proposed bandpass filter has a wide passband of 100~150GHz and a return loss of better than 14dB. The designed power divider can operate at 500GHz which is the first reported design using a 180nm CMOS process**.

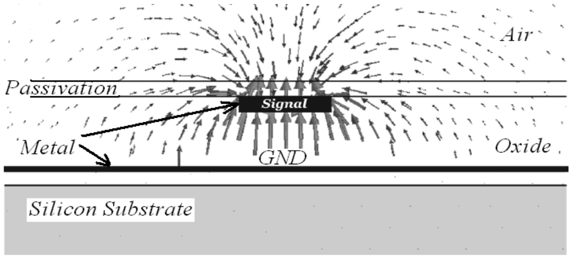
***Index Terms*— CMOS, Millimeter-wave Integrated Circuit, Nanometer, Terahertz, Passive Circuits**

I. INTRODUCTION

Terahertz electromagnetic radiation (from 100 GHz to 10 THz) that lies in the boundary region between light and radio waves has attracted much attention in recent years due to its advantages in sensing systems. Terahertz waves could also handle ultra-broadband signals, have very large absorption due to water or water vapor, and are transparent through many materials (e.g., plastic, paper, cloth, and oil) that are opaque in visible and IR light. Many materials have a so-called fingerprint spectrum in the spectrum range [1-4]. Therefore, terahertz waves are expected to be applied to ultrahigh data rate wireless communications, scanning systems for hazardous materials, and assay devices for medical examinations. They are also expected to be applied to the multi-residue analysis of agrichemicals, medical diagnostics, environmental assessment, process monitoring systems for industrial products, and biometric security. There is an atmosphere prevailing that terahertz technology represents the dawn of a new era [1].
Conventional terahertz integrated circuits (ICs) are implemented in III–V compound semiconductor technology [3-4] instead of standard CMOS because of its high electron mobility and semi-insulating substrate. With the continuous down-scale of channel length, the unity-gain frequency and maximum oscillation frequency of the latest CMOS devices have surpassed 100 GHz. CMOS circuits directly benefit from the higher speed of the scaled technology [5-10]. Additionally, improved circuit topologies and new design approaches to fully exploit the intrinsically faster devices have been introduced [11-13]. Now, CMOS technology has made it one of the most favorite technologies for millimeter wave design [5-13]. With further down-scaling and accuracy of fabrication, it is expected that the CMOS technology may become an alternative solution for circuits and systems implementation toward Terahertz operation. However, it is a challenge for CMOS design to combat high substrate loss. In order to reduce the substrate loss, [7] introduces a thin-film microstrip line (MSL) configuration as shown in Fig.1b, which has much better performance as compared to Coplanar waveguide (CPW) line on loss Si substrate (resistivity~10Ω·cm for commercial CMOS) as shown in Fig. 1a. For the MSL, metal1 was used for the ground planes and top metal was used for the signal line. Metal1 shields the unwanted effects of the conductive substrate. The loss of 0.25dB/mm for the MSL, and of 2.3dB/mm for the CPW at 40 GHz are experimentally demonstrated in [7]. As the electric field distribution of these two transmission structures shown in Fig.1, the loss reduction is from making the electromagnetic concentrate in the region of low loss silicon oxide substrate rather than loss silicon.



(a) Vector electric field distribution of CPW on CMOS



(b) Vector electric field distribution of MSL on CMOS
Fig. 1 The vector electric field distribution of MSL and CPW

In this paper, novel passive circuits, which can operate at terahertz frequency on a standard CMOS, are designed and investigated by using low loss MSL. Both circuit analysis and full-wave electromagnetic analysis are used to design a novel multimode bandpass filter, which can operate at 125GHz with a bandwidth of 50GHz, and a wideband power divider, which works in the frequency from 200GHz to 700GHz with return loss better than 15dB. This investigation shows that CMOS is a very good candidate for terahertz passive circuit and system design and implementation, and combination uses of circuit and full-wave analysis are an effective approach for CMOS passive circuit design beyond millimeter-wave frequency.

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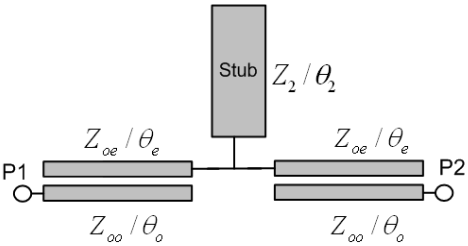
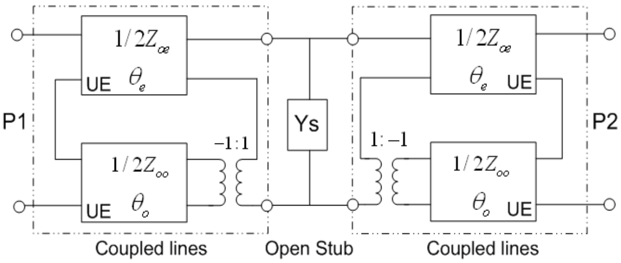
II. 125GHZ MULTIPLE MODE FILTER DESIGN



(a) Transmission line model of the proposed multimode filter



(b) The network model of (a)

Fig. 2 Proposed multimode filter topology and its network model

Bandpass filters with high-performance and compact size are highly demanded in most of the communication systems [14-16]. Fig. 2a shows the proposed filter configuration for CMOS implementation. An open stub with impedance of Z_2 and electric length of θ_2 connects with two section coupled transmission lines at the left-hand and right hand sides. The coupled transmission lines provide the even-mode impedance and electric length of Z_{oe} and θ_e and also the odd-mode impedance and the electric length of Z_{oo} and θ_o respectively. The structure in Fig. 2a can be represented by using the equivalent circuit network shown in Fig. 2b with unit element (UE) of the network [17]. As shown in Fig. 2b, the coupled transmission lines are represented by the UEs and the -1:1 transformer [17]. The shunt stub can be represented by the admittance of Y_s connected in shunt in the middle of the equivalent networks of the two sections of coupled transmission lines. The transmission characteristics of the network in Fig. 2b are calculated by doing the matrix conversion from ABCD matrix to the S-matrix. The ABCD matrix can be obtained by cascading the ABCD matrixes of the coupled transmission lines and the stub as follows:

$$\begin{bmatrix} A_t & B_t \\ C_t & D_t \end{bmatrix}_t = \begin{bmatrix} A_c & B_c \\ C_c & D_c \end{bmatrix}_c \times \begin{bmatrix} 1 & 0 \\ Y_s & 1 \end{bmatrix}_s \times \begin{bmatrix} A_c & B_c \\ C_c & D_c \end{bmatrix}_c \tag{1}$$

Where

$$A_c = \frac{Z_{oe}\cot\theta_e + Z_{oo}\cot\theta_o}{Z_{oe}\csc\theta_e - Z_{oo}\csc\theta_o} = D_c \tag{2}$$

$$B_c = \frac{j}{2}\frac{Z^2_{oe} + Z^2_{oo} - 2Z_{oe}Z_{oo}(\cot\theta_e\cot\theta_o + \csc\theta_e\csc\theta_o)}{Z_{oe}\csc\theta_e - Z_{oo}\csc\theta_o} \tag{3}$$

$$C_c = \frac{2j}{Z_{oe}\csc\theta_e - Z_{oo}\csc\theta_o} = D_c \tag{4}$$

$$Y_s = j/Z_2\tan\theta_2 \tag{5}$$

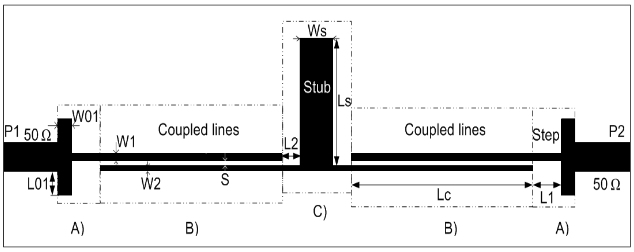


Fig. 3 Top metal configuration of the proposed thin-film MSL filter

The multimode bandpass filter is constructed on Chartered Semiconductor Manufacturing Ltd (CSM) 180nm CMOS process with six metal layers (from first metal layer (M1) to sixth Metal layer (M6) or top metal layer with a thickness of around 2μm. The thickness of other layers is around 0.57μm). The top metal is used for the signal trace of the MSL while the metal 1 or the bottom metal close to lossy silicon is used for the ground of thin-film MSL. The substrate from top metal to bottom metal is around 8μm. The layout of the top meal is shown in Fig. 3. The structure is symmetrical along the open stub in C) portion. The portion A) is mainly used to adjust the I/O matching. The portion C) is to generate the multiple operation modes and adjust the zero point in the stopband to control the stopband performance. The coupled lines in portion B) are to control the filter bandwidth as well as the modes. The dimensions of the filter are: *W1*=5.6μm, *W2*=5.6μm, *W01*=9.2μm, *L01*=23.6μm, *Lc*=363μm, *Ws*=99.4μm, *Ls*=98μm and *S*=2.5μm.

The analysis results through circuit (ADS2004 from Agilent)

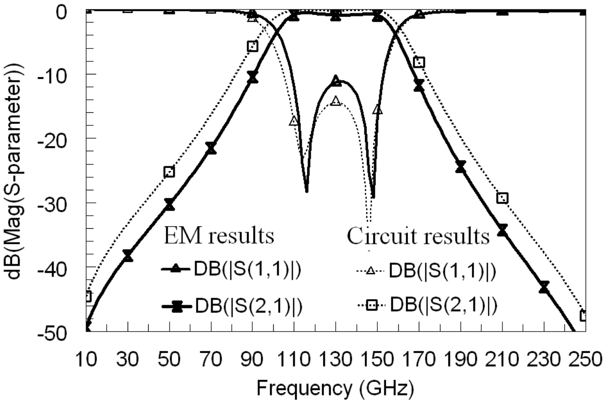


Fig. 4 Circuit and EM results of the proposed multimode filter

and full-wave EM simulation (HFSS9.2 from Ansoft Corporation) are compared in Fig. 4. Both results are well agreed in transmission and reflection. The designed filter is operating at 125GHz with bandwidth of 50GHz. Due to the use of thin-film MSL, which uses silicon oxide as the substrate and metal 1 as the signal ground, the insertion loss in the pass band is dramatically reduced due to thin-film MSL and multiple mode operation [16] of the bandpass filter. The size of the thin-film multimode filter is 1000µm times 200µm

III. 500GHZ THIN-FILM POWER DIVIDER

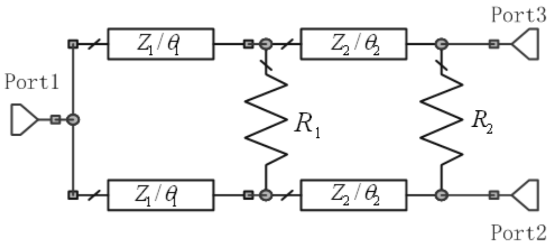


Fig. 5 Transmission line topology of the Wilkinson power divider

Wilkinson power divider [18-19] is a very important component of microwave amplifier and antenna distribution circuits. But it is rarely used in CMOS RF circuits due to the lossy silicon substrate and relative larger size below millimeter-wave frequency. However, at terahertz frequency range, it becomes advantages to implement the Wilkinson power divider circuits on CMOS with lower loss and compact size through using the thin-film MSL. The transmission line topology of the two-stage Wilkinson power divider is shown in Fig. 5. For this two-stage divider, under the constraint of Z_{1e}=Z_{1o}= Z_1, Z_{2e}=Z_{2o}= Z_2 and θ_1= θ_2=90 (Z_{io} and Z_{ie} are odd and even mode impedance of the transmission lines i=1,2 ; Z_1 and Z_2 are the characteristic impedance of the single transmission lines, and θ_1 and θ_2 are electric length of the transmission lines). The normalized electric parameters can be calculated by using following formula [20]:

$$Z_2 = \left[\left(2 + \frac{1}{4\tan^4 \Phi} \right)^{1/2} + \frac{1}{2\tan^2 \Phi} \right]^{1/2} \tag{6}$$

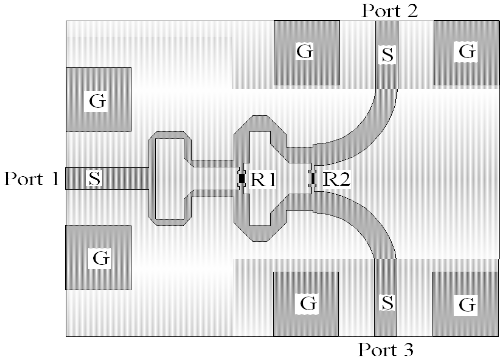
$$Z_1 = \frac{2}{Z_2} \tag{7}$$

$$R_1 = \frac{2}{(Z_1 + Z_2)^{1/2} (Z_1 - Z_2 \cot^2 \Phi)^{1/2}} \tag{8}$$

$$R_2 = \frac{2R_1(Z_1 + Z_2)}{R_1(Z_1 + Z_2) - Z_1} \tag{9}$$

$$\Phi = \frac{\pi}{4} \left[1 - \frac{1}{\sqrt{2}} \left(\frac{\frac{f_2}{f_1} - 1}{\frac{f_2}{f_1} + 1} \right) \right] \tag{10}$$

where bandwidth is equal f_2 minus f_1 (f_2 and f_1 are upper and low operating frequency respectively). The above parameters are optimized by using the circuit simulator with real time view of the circuit performance. A wideband power divider operating at 500GHz is designed. The electric parameters of the transmission line and resistors are: characteristic impedances Z_1=81.6Ω, Z_2=58.8Ω, electric length θ_1= θ_2=90 degrees at 500GHz and the resistance R_1=100 Ω, R_2=150 Ω. The electric parameters are used to determine the physical parameters of the thin-film MSL on CMOS (CSM 180nm CMOS process and thin-film MSL configuration are chosen for design and implementation). The calculated physical parameters corresponding to electric parameters of Z_1 and θ_1 are W1=5µm and L1=99.1µm respectively. The calculated physical parameters corresponding to electric parameters of Z_2 and θ_2 are W2=11µm and L2=94.8µm respectively. With known physical parameters, the distributed effects due to the layout of bending and “T-junction” etc (refer to the practical layout of the thin-film MSL power divider on CMOS in Fig. 6) are considered at Terahertz frequency range through using the circuit simulator. The circuit results are used as the reference for the full-wave EM optimization. The circuit simulation results and full-wave EM results are compared in Fig. 7. Excellent agreement between the circuit and EM results are achieved. The designed power divider operates from 260GHz to 660GHz. The return loss is better than 15dB and the isolation between two output ports is better than 15dB. Good balance between two output ports is achieved. The size of the thin-film power divider is only 300µm times 250µm.



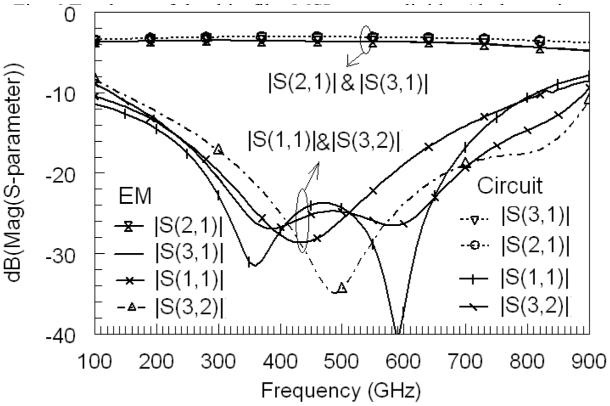


Fig. 7 Wideband magnitude characteristics of thin-film power divider

IV. CONCLUSION

The nanometer CMOS technology is adopted to design passive circuits, which can operate at terahertz frequency. A low loss MSL is adopted in these passive circuit design. Both circuit and full-wave electromagnetic simulations are used to design a novel 125GHz multimode bandpass filter and a 500GHz wideband power divider. This investigation shows that though the transistor has challenge to support terahertz active circuit operation for current technology, current nanometer CMOS technology is a very good for terahertz passive circuit implementation. The combination uses of circuit and full-wave analysis are an effective approach for the nanometer CMOS passive circuit design at millimeter-wave frequency or toward terahertz frequency. It is addressed that though the design is on 180nm commercial CMOS process, the same design approach can be used to implement these passive circuits on other CMOS processes such as130nm or 90nm.

REFERENCES

[1] H.-W. Hübers, "Terahertz Heterodyne Receivers," *IEEE Journal of Selected Topics in Quantum Electronics.*, vol. 14, no.2, pp. 378–391, March/April 2008.

[2] P. H. Siegel, R. P. Smith, M. C. Gaidis, and S. Martin, "2.5-THz GaAs monolithic membrane-diode mixer," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 596–604, May 1999

[3] H. M. Pickett, J. C. Hardy, and J. Farhoomand, "Characterization of a dual-mode horn for submillimeter wavelengths," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 936–937, Aug. 1984

[4] Y.-T. Li, J.-W. Shi, C.-L. Pan, C.-H. Chiu, W.-S. Liu, N.-W. Chen, C.-K. Sun, and J.-I. Chyi, "Sub-THz photonic-transmitters based on separated-transport-recombination photodiodes and a micromachined slot antenna," *IEEE Photon. Technol. Lett.*, vol. 19, no. 11, pp. 840–842, Jun. 1, 2007.

[5] J. Y. Hasani, M. Kamarei, and F. Ndagijimana, "Sub-nH Inductor Modeling and Design in 90-nm CMOS Technology for Millimeter-Wave Applications," *IEEE Trans. Circuits and systems-II.*, vol. 55, no. 6, pp. 517–521, June, 2008.

[6] M. Sasaki, "Design of a Millimeter-Wave CMOS Radiation Oscillator With an Above-Chip Patch Antenna," *IEEE Trans. Circuits and systems-II.*, vol. 53, no. 10, pp. 1128–1132, Oct, 2006.

[7] H. Shigematsu, T. Hirose, F. Brewer and M. Rodwell, "Millimeter-wave CMOS Circuit Design," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no.2, pp. 472–477, Feb. 2005

[8] K. Yamamoto and M. Fujishima, "70GHz CMOS harmonic injection locked divider," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2006, pp. 2472–2481.

[9] T.-N. Luo and Y.-J. E. Chen, "A 0.8-mW 55-GHz dual-injection-locked CMOS frequency divider," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 3, pp. 620–625, Mar. 2008

[10] L. M. Franca-Neto, R. E. Bishop, and B. A. Bloechel, "64 GHz and 100 GHz VCO's in 90 nm CMOS using optimum pumping method," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2004, pp.444–445

[11] Kaixue Ma, J.-G. Ma, L. Jia, B. Ong, M. A. Do, and K. S. Yeo, "800MHz~2.5GHz Miniaturized Multi-layer Symmetrical Stacked Baluns for Silicon Based RF ICs," *IEEE MTT-S Int. Microwave Symp. Dig.*, 2005, pp. 283-286

[12] R.-C. Liu, H.-Y. Chang, C.-H. Wang, and H. Wang, "A 63 GHz VCO using a standard 0.25μm CMOS process," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2004, pp. 446–447

[13] B. Razavi, "A 60-GHz CMOS receiver front-end," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan. 2006

[14] K. Ma, J.-G. Ma, and K. S. Yeo, and M. A. Do, "A compact size coupling controllable filter with separated electric and magnetic coupling paths" *IEEE Trans. Microwave Theory Tech.*, vol.54, no.3, pp.1113-1119, Mar., 2006

[15] K. Ma, K. S. Yeo, J.-G. Ma, M. A. Do, "An ultra-compact hairpin band pass filter with additional zero points", *IEEE Microwave and Wireless Components Lett.* vol.17, pp.262~264, April, 2007

[16] K. Ma, K. C. B. Leong, R. M. Jayasuriya and K. S. Yeo, "A Wideband and High Rejection Multimode Bandpass Filter Using Stub Perturbation", *IEEE Microwave and Wireless Components Lett.* vol.19, pp.24~26, Jan. 2009

[17] G. I. Zysman and A. K. Johnson, "Coupled Transmission line networks in an inhomogeneous dielectric medium," *IEEE Trans. Microwave Theory Tech.*, vol.17, no.10, pp.753-759, Oct., 1969

[18] J. Rogers and C. Plett, *Radio frequency integrated circuit design*, Artech House 2003

[19] E. J. Wilkinson, "An N-way hybrid power dividers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-8, pp. 116–118, 1960.

[20] L. Fan, and K. Chang, "Uniplanar Power Dividers using coupled CPW and asymmetrical CPS for MIC's and MMIC's," *IEEE Trans. Microwave Theory Tech.*, vol. 44, no.12, pp. 2411–2420, Dec. 1996