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16.6- and 28-GHz Fully Integrated CMOS RF Switches With Improved Body Floating

Qiang Li, *Member, IEEE*, Y. P. Zhang, Kiat Seng Yeo, *Member, IEEE*, and Wei Meng Lim

Abstract—This paper presents two fully integrated CMOS transmit/receive (T/R) switches with improved body-floating operations. The first design exploits an improved transistor layout with asymmetric drain–source region, which reduces the drain–source feed-through for body-floated RF switches. In the second design, a switched body-floating technique is proposed, which reconfigures the body-floating condition of a switch transistor in the ON and OFF states. Both designs are fabricated in a standard 0.13- μm triple-well CMOS process. With regard to 2-dB insertion loss, the switch with asymmetric drain–source achieves 28-GHz bandwidth, which is among the highest reported frequencies for CMOS T/R switches. The bandwidth of the switched body-floating design is 16.6 GHz. There is approximately 5 dB better isolation obtained in the switched body-floating design. With the resistive double-well body-floating technique, 26.5- and 25.5-dBm input 1-dB compression point ($P_{1\text{dB}}$) are obtained, respectively. Both designs consume only $150\ \mu\text{m} \times 100\ \mu\text{m}$ die area. The demonstrated T/R switches are suitable for high-frequency and wideband transceivers.

Index Terms—Asymmetric drain–source, CMOS integrated circuits, MOSFET switches, RF switches, switched body floating, transmit/receive (T/R) switches, triple well.

I. INTRODUCTION

SWITCHING functions are extensively employed in RF systems, especially with the development of the multimode and multiband transceivers. Several emerging applications, e.g., multiple-input multiple-output (MIMO), subsampling/decimating, antenna/phase arrays, etc., essentially require RF switches. RF switches are also used as passive mixers. A good example of an RF switch is the transmit/receive (T/R) antenna switch, which requires low insertion loss, high isolation, and good linearity. At high frequencies, due to the high-loss nature of the silicon substrate, it is very difficult to achieve the above performances concurrently in CMOS. For years, RF switches have been dominated by discrete components using p–i–n diodes and III–V MESFETs. Compared with other CMOS RF circuits that have been pushed beyond 100 GHz, the design of CMOS RF switches is only explored to a limited extent. To date, most of the reported CMOS T/R switches are below 6 GHz [1]–[7]

and the maximum reported operating frequency of a CMOS RF switch is around 15–20 GHz [8]–[10].

The performance of high-frequency T/R switches is mainly limited by the capacitive coupling from the silicon substrate and OFF transistors. To enhance the bandwidth of CMOS T/R switches beyond 10 GHz, the effect of capacitive coupling should be minimized. There are two approaches that were demonstrated. One approach employs an LC network to compensate the effect of coupling capacitance, which can be implemented in the form of an impedance transformation network (ITN) [8] or artificial transmission line [9]. This method can effectively compensate the parasitic capacitance in the input and output nodes. However, a large silicon area has to be consumed for on-chip inductors; and the effect of internal capacitive loss cannot be reduced. The other approach was proposed from the point of view of switch transistors in the cutoff region [10]. It is shown that, for high-frequency T/R switches, the parasitic capacitances of the OFF transistors significantly impact the overall performance, and there are always OFF transistors connected to an ON transistor. To improve the operation frequency of the T/R switch, the number of OFF transistors and the drain–source coupling capacitance of the OFF transistors should be minimized. In the demonstrated switch in [10], the shunt arms in a typical T/R switch are removed and a customized layout with decoupled drain–source is exploited for the switch transistors. This method enhances the bandwidth effectively without using on-chip inductors.

The body-floating technique has been used for high-linearity CMOS RF switches in the form of an LC -tuned body floating in a standard N -well CMOS [5] or wideband resistive body floating in a triple-well CMOS [7]. An improved double-well body-floating technique was also introduced in [10], where both the p-well and deep n-well are biased through large resistors to make them RF floating. However, when the customized layout is employed together with the body-floating technique, the floating body becomes a feed-through path between the drain and source, which has limited the bandwidth of the demonstrated T/R switch to 20 GHz.

Since body floating can hardly be avoided for switches requiring high linearity, it is important to find new approaches to further improve the performance of CMOS RF switches under the body-floating condition. This paper proposes two methods from two different points of view. One method is to minimize the drain–source coupling capacitance with the floating body, and the other one is to reconfigure the body-floating condition of the ON and OFF transistors. Both approaches are demonstrated in a 0.13- μm standard triple-well CMOS process. Section II explains the mechanism of the drain–source coupling under the body-floating condition. Section III presents an improved layout

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Q. Li was with the Centre for Integrated Circuits and Systems, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798. He is now with the Institute of Microelectronics, Singapore 117685 (e-mail: liqiang@pmail.ntu.edu.sg)

Y. P. Zhang, K. S. Yeo, and W. M. Lim are with the Division of Circuits and Systems, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798.

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Fig. 1. Simplified cross-sectional view of a typical nMOS transistor in a triple-well process. The parasitic capacitances and diodes limit the high-frequency performance of CMOS switches.

for body-floating switch transistors where the drain–source coupling can be minimized. In Section IV, a switched body-floating technique is proposed and discussed. Section V compares and discusses the experimental results. This paper presents conclusions in Section VI.

II. DRAIN–SOURCE COUPLING WITH FLOATING BODY

The capacitive feed-through between the drain and source is a dominant limit for high-frequency CMOS T/R switches. Fig. 1 shows a simplified cross-sectional view of an nMOS transistor in the triple-well process. When the transistor is used as a switch and is turned OFF, the feed-through between the drain and source is due to the parasitic capacitance C_{gs} , C_{gd} , C_{ds} , C_{sb} , and C_{db} . It is shown that in deep-submicrometer CMOS technologies, C_{ds} is dominant due to the metal interconnections, which can be significantly reduced by enlarging the distance between the drain and source [10]. In this case, the drain–source coupling is determined by C_{gs} , C_{gd} , C_{sb} , and C_{db} . When the body is biased to a dc voltage directly (RF grounded), C_{sb} and C_{db} will not contribute to the drain–source feed-through (though they create loss). The coupling capacitance between the drain and source can be written as

$$C_{DS,BG} = \frac{C_{gs} \cdot C_{gd}}{C_{gs} + C_{gd}}. \quad (1)$$

However, when the body-floating technique is employed, the body becomes a floating point; the coupling path through C_{sb} and C_{db} will contribute to the drain–source feed-through

$$C_{DS,BF} = \frac{C_{gs} \cdot C_{gd}}{C_{gs} + C_{gd}} + \frac{C_{sb} \cdot C_{db}}{C_{sb} + C_{db}}. \quad (2)$$

The second term in (2) clearly shows the effect of the body parasitics C_{sb} and C_{db} . This effect is further enhanced with the increased drain–source area when the distance between them is enlarged. Therefore, the body-floating technique actually improves the linearity at the cost of insertion loss and isolation degradations.

Note that the above analysis neither depends on the realization of body floating, nor on the triple-well process. The purpose of the custom layout proposed in [10] is to reduce the drain–source coupling of switch transistors in the cutoff region

Fig. 2. Customized layout with asymmetric drain and source for switch transistors.

so that insertion loss and isolation can be improved. However, the body floating degrades such improvement and eventually limits the bandwidth of CMOS T/R switches. To further improve the performance, the drain–source feed-through should be minimized under body-floating conditions.

III. CUSTOM LAYOUT WITH ASYMMETRIC DRAIN–SOURCE FOR SWITCH TRANSISTORS

Compared with (1), the second term in (2) indicates the additional coupling capacitance when the body is floating. To minimize this term, a straightforward approach is to reduce the values of C_{sb} and C_{db} , which requires small active areas of drain and source. However, the coupling due to metal interconnections will then increase significantly [10], which is very unfavorable for high-frequency circuits and will severely degrade the performance of switches. Therefore, a further customized layout with an asymmetric drain and source is proposed here.

Fig. 2 shows a layout sketch of the further customized switch transistors. Comparing with the layout proposed in [10], the distance between the drain and source is increased by only stretching one side. As a result, only the drain or the source areas are enlarged. The distance between them is kept at four times the p-cell default, which ensures the minimized drain–source coupling due to metal interconnections. Since one of C_{sb} and C_{db} is not changed in the custom layout, the second term in (2) is only increased by a small value. Referring to the capacitance values given in [10], the coupling capacitance under the body-floating condition can be estimated. The second term in (2) is 17.5 fF for the custom layout proposed in [10], which is reduced dramatically to 6.78 fF for the custom layout of Fig. 2. As each ON transistor is connected with at least one OFF transistor, the reduction of drain–source coupling will improve both insertion loss and isolation performance.

Fig. 3. Schematic of an SPDT T/R switch with double-well body floating. The dashed line denotes the deep n-well isolation.

Fig. 4. Die microphotograph of the fabricated switch shown in Fig. 3.

Fig. 3 shows the schematic of a single-pole double-throw (SPDT) T/R switch without shunt arms in which the double-well body-floating technique is employed. The dashed line denotes the deep n-well isolation. Since the custom layout proposed in Fig. 2 is asymmetric, it is necessary to consider the assignment of the drain-source. Intuitively, the side with less parasitics should be assigned to the node that is more critical. In Fig. 3, the common node (ANT) is considered more critical because there is always a signal (TX or RX) applied to the antenna port. Placing the small-area side to this node will prevent signals from coupling to the body and then elsewhere. This is also true when body floating is not used, where the large area leads to a severe loss of signals. Note that the resistive (ohmic) loss in the small-area side is also smaller, but the overall ohmic loss between the drain and source is equal to that of the custom layout proposed in [10].

The switch was fabricated in a 90-GHz 0.13- μm triple-well CMOS technology. Fig. 4 shows the die microphotograph of the fabricated T/R switch. The active area of the switch is only $150\ \mu\text{m} \times 100\ \mu\text{m}$. With test pads, the switch chip occupies $415\ \mu\text{m} \times 415\ \mu\text{m}$. The measurement was carried out on-wafer

Fig. 5. Measured and simulated insertion loss, isolation, and return loss for the fabricated switch shown in Fig. 3.

with ground-signal-ground (G-S-G) probes and the pad effect was deembedded using the Y-Z deembedding technique, where dedicated pads and metal connections used in the design were fabricated and measured. In the measurement, the control voltage is 2/0 V and the ANT/TX/RX nodes are biased at 0.5 V. The p-well and p-substrate are biased at 0.5 V and the deep n-well is biased at 2 V. This is the same condition used in [10].

The measured insertion loss and isolation of the fabricated switch are shown in Fig. 5. The dashed lines denote the simulated performances. The difference between the simulated and measured performance is most likely caused by the inaccuracy of the transistor model (BSIM) in the linear region. The deembedding process can also cause the discrepancies. With regard to 2-dB insertion loss, the bandwidth of the switch is over 28 GHz. The insertion loss is within 2.4 dB for the measured frequencies up to 35 GHz. It is shown that the insertion loss is improved significantly with the proposed asymmetric layout. The isolation is better than 15 dB for frequencies up to 35 GHz. Note that at frequencies below 20 GHz, the isolation is relatively inferior to the result obtained in [10]. This may be caused by the excessive drain-source coupling in the real chip. Meanwhile, the switch in [10] employs a differential architecture and, thus, some of the coupling components (even order) are canceled. Fig. 5 also gives the simulated and measured return loss from the antenna port, which is well below 10 dB over the measured bandwidth. This is because the switch is basically operated where the antenna port is always connected to a 50- Ω termination.

The linearity performance is measured by the input 1-dB compression points ($P_{1\text{dB}}$). At different frequencies, the $P_{1\text{dB}}$ result is shown in Fig. 6. Around 26.5 dBm, $P_{1\text{dB}}$ is achieved. Note that the $P_{1\text{dB}}$ curve is almost flat at high frequencies, which is probably caused by the combined effect of the body floating and return loss: the former tends to degrade the linearity at high frequencies [10], while the worse matching at higher frequencies will reduce the power fed into the switch and, thus, enhance the $P_{1\text{dB}}$ performance. Compared with the 30-dBm $P_{1\text{dB}}$ obtained in [10], the 3-dBm difference is due to the nature of differential architecture (twice of power can be handled). Another 0.5 dBm may be consumed on the tradeoff

Fig. 6. Input P_{1dB} for the fabricated switch shown in Fig. 3.

Fig. 7. Schematic of an SPDT T/R switch with switched body-floating scheme.

Fig. 8. Die microphotograph of the fabricated switch with switched body-floating technique, as shown in Fig. 7.

among linearity and other performances. The results shown in Figs. 5 and 6 indicate that the proposed layout with asymmetric drain-source for switch transistors effectively improves the performance of the CMOS T/R switch.

Fig. 9. Measured and simulated insertion loss, isolation, and return loss for the fabricated switch with switched body-floating technique, as shown in Fig. 7.

Fig. 10. Input P_{1dB} for the fabricated switch with switched body-floating technique, as shown in Fig. 7.

IV. SWITCHED BODY FLOATING

Besides the straightforward approach to minimizing drain-source coupling with the floating body, this problem can also be disentangled by improving the body-floating technique itself. Comparing with (1), the additional (second) term in (2) appears only when the body is floating. This term can be removed when the body is RF grounded (directly connected to a dc voltage), i.e., body floating is not favorable for OFF transistors. On the other hand, to have a good performance at high frequency, body floating is favorable for ON transistors. Therefore, the requirement of body floating actually differs for transistors in different states. This observation leads to an improved body-floating scheme, where the body can be made floating when a transistor is turned ON and grounded when it is turned OFF.

A possible realization of the scheme is shown in Fig. 7. The body floating is controlled by an additional switch connected in parallel with the biasing resistor, which provides a controllable impedance between the body and its dc-biasing voltage. When the switch transistor is turned ON, the body switch is turned OFF, the body of the ON transistor becomes RF floating; and vice

TABLE I
SUMMARY OF PERFORMANCE AND COMPARISON WITH REPORTED HIGH-FREQUENCY CMOS T/R SWITCHES

Performance		This Work		[8] *	[9]	[10] †
		Asymmetric D/S	Switched B/F			
CMOS Technology		0.13 μm	0.13 μm	0.13 μm	0.18 μm	0.13 μm
Insertion Loss (dB)	10 GHz	0.8	1.3	1.1	0.9	1.7
	15 GHz	1.0	1.9	1.8	1.0	1.7
	20 GHz	1.3	2.0	–	2.5	2.0
	28 GHz	2.0	2.6	–	5.2	–
Isolation (dB)	10 GHz	20	23	24	32	32
	15 GHz	18	22	23	28	32
	20 GHz	16	21	–	26	21
	28 GHz	15	21	–	27	–
2-dB Bandwidth (GHz)		28	16.6	17–20 ‡	19	20
$P_{1\text{dB}}$ (dBm)		26.5	25.5	21.5	25	30
Area (mm^2)		0.015	0.015	0.2	0.06	0.027
Control/Bias Voltages (V)		2/0.5/0	2/0.5/0	3.0/1.8/1.0	3.6/1.8/0/-1.8	2/0.5/0

* Best available performance in case of multiple designs.

† Performances in differential-mode.

‡ Estimated value.

versa. Under this configuration, the body of the OFF transistors are RF grounded and the second term in (2) no longer exists. As a result, the drain–source coupling through body is significantly reduced.

Nevertheless, there is a negative effect brought by this switched body-floating technique. Since the OFF transistor is body grounded, the parasitics to the body, C_{sb} or C_{db} , lead to extra loss to the ground. Therefore, the insertion loss is degraded and is naturally inferior to that of the switch with its body always floating.

To reduce the above negative effect, the parasitics at the common node (ANT) should be kept as small as possible. This is because the common node is connected to both the ON transistor and OFF transistor concurrently, and the grounded parasitics in the OFF transistor create extra loss for the ON transistor. Also consider the parasitics due to metal interconnections, the custom layout of Fig. 2 is employed with the small-area side assigned to the common node.

The switch was fabricated in the same 0.13- μm triple-well CMOS process, as stated in Section III. Fig. 8 shows a die microphotograph of the fabricated T/R switch, which consumes the same area as the switch discussed in Section III. The measurement and biasing conditions are also kept the same. The measured and simulated insertion loss, isolation, and return loss are shown in Fig. 9. Again, there are discrepancies between them, which is likely due to the inaccuracy in transistor models and the deembedding process. Note that, at very low frequencies, the insertion loss of this switch is very close to the pre-

vious one shown in Fig. 5. The insertion loss drops to 2 dB at 16.6 GHz. At frequencies up to 25 GHz, the insertion loss is within 2.3 dB. The isolation is better than 21.5 dB for frequencies up to 35 GHz. The increased insertion loss, as compared to Fig. 5, results from the loss due to the grounded OFF transistor, as previously discussed. On the other hand, the isolation is improved by 3–6 dB compared to Fig. 5, which clearly shows the effect of the switched body floating. This is a consequence of the fundamental tradeoff between insertion loss and isolation.

The linearity performance in terms of $P_{1\text{dB}}$ is shown in Fig. 10. Around 25.5-dBm $P_{1\text{dB}}$ is obtained. Compared to Fig. 10, this result is 1 dBm lower, but the trend is very similar. The linearity degradation may result from the effect of the grounded OFF transistor [10]. In addition, the parasitics of the body switch can also degrade the body-floating condition and, thus, degrade the linearity.

V. PERFORMANCE COMPARISON AND DISCUSSIONS

The performances of the proposed T/R switches are summarized in Table I. It is shown that the proposed asymmetric layout is more efficient in terms of insertion loss, while the switched body-floating technique is more isolation driven. This table also compares the performances with other reported high-frequency CMOS T/R switches with more than 10-GHz bandwidth. With the proposed techniques, the bandwidth of the CMOS T/R switch is further improved without using LC networks.

Note that the mechanism of resistive body floating in the triple-well process is the same as the gate floating. Therefore,

the floating gate also contributes to the drain–source coupling capacitances, as shown in (1) and (2). From the point of view of the OFF transistors, the feed-through due to gate floating should also be reduced for CMOS switches targeting on even higher frequency. Eventually, a fundamental limit to the performance of the CMOS T/R switch is the parasitic capacitance. The biasing condition is also very important since it determines the ON resistance of the switch.

VI. CONCLUSION

The capacitive feed-through between the drain and source of the OFF transistor limits the bandwidth of CMOS RF switches, and this effect gets worse under body-floating conditions. This paper has proposed two approaches to minimize this effect and improve the bandwidth of CMOS switches. A custom layout with an asymmetric drain and source has been proposed for the switch transistors, which reduces the drain–source coupling from both floating-body and metal interconnections. The fabricated switch with this technique achieved a high 2-dB bandwidth of 28 GHz in a standard 0.13- μm CMOS technology. Instead of minimizing the capacitance values, the other proposed approach reconfigures the body-floating condition of the switch transistors, where only the body of the ON transistor is floating. This is implemented by using an additional body switch to control the biasing of the main switch transistor. The fabricated switch with switched body floating achieves a 2-dB bandwidth of 16.6 GHz. The isolation is improved at the cost of degraded insertion loss. With the proposed techniques, the bandwidth of CMOS switches is improved without using LC networks. As a result, both designs occupy only a $150\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ active area. Further performance improvement of CMOS RF switches can be expected with advanced silicon technologies and sophisticated biasing and controlling schemes.

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Qiang Li (S'04–M'07) was born in Xuchang, China, in 1979. He received the B.E. degree in electrical engineering from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2001, and the Ph.D. degree in electrical and electronics engineering from the Nanyang Technological University (NTU), Singapore, in 2007.

From 2001 to 2002, he was an RTP Analog/Mixed-Signal Integrated Circuit Designer with the Center for Wireless Communications (later known as the Institute for Communications Research and currently the Institute for Infocomm Research, A*STAR), Singapore. In 2006, he joined the Institute of Microelectronics, Singapore, where he is a Senior Research Engineer involved with analog and mixed-signal integrated circuits. His research interests include analog/RF circuits for wireless communications, data converters, and mixed-signal circuits for biomedical applications.

Y. P. Zhang received the B.E. degree from the Taiyuan Polytechnic Institute, Taiyuan, China, in 1982, the M.E. degree from the Shanxi Mining Institute, Taiyuan University of Technology, Shanxi, China, in 1987, and the Ph.D. degree from the Chinese University of Hong Kong, Hong Kong, in 1995, all in electronic engineering.

From 1982 to 1984, he was with the Shanxi Electronic Industry Bureau. From 1990 to 1992, he was with the University of Liverpool, Liverpool, U.K. From 1996 to 1997, he was with the City University of Hong Kong. From 1987 to 1990, he was with the Shanxi Mining Institute. From 1997 to 1998, he was with the University of Hong Kong. In 1996, he became a Full Professor with the Taiyuan University of Technology. He is currently an Associate Professor and the Deputy Supervisor of the Integrated Circuits and Systems Laboratories, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. He has authored or coauthored numerous publications for seven IEEE societies. He has delivered scores of invited papers/keynote address at international scientific conferences. He has broad research interests in radio science and technology. He is listed in *Marquis Who's Who*, *Who's Who in Science and Engineering*, and *Cambridge IBC 2000 Outstanding Scientists of the 21st Century*. He serves on the Editorial Board of the *International Journal of RF and Microwave Computer-Aided Engineering* and was a Guest Editor of this journal for the "Special Issue on RF and Microwave Subsystem Modules for Wireless Communications." He also serves as an Associate Editor of the *International Journal of Microwave Science and Technology*.

Dr. Zhang serves on the Editorial Boards of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS. He has organized/chaired dozens of technical sessions of international symposia. He was the recipient of the 1990 Sino-British Technical Collaboration Award for his contribution to the advancement of subsurface radio science and technology. He was the recipient of the 2000 Best Paper Award presented at the Second International Symposium on Communication Systems, Networks and Digital Signal Processing, Bournemouth, U.K., and the 2007 Best Paper Prize presented at the Third IEEE International Workshop on Antenna Technology, Cambridge, U.K. He was also the recipient of the 2005 William Mong Visiting Fellowship presented by the University of Hong Kong.

Kiat Seng Yeo (M'00) received the B.E. degree in electronics (Hons.) and Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore in 1993 and 1996, respectively.

In 1996, he begun his academic career as a Lecturer, became an Assistant Professor in 1999, and then an Associate Professor in 2002. from 2001 to 2005, he was Sub-Dean (Student Affairs), during which time he held several concurrent appointments as Program Manager of the System-on-Chip flagship project, Coordinator of the Integrated Circuit Design

Research Group, and Principal Investigator of the Integrated Circuit Technology Research Group, NTU. He is on the Advisory Committee of the Centre for Science Research and Talent Development, Hwa Chong Junior College. In July 2005, he became Head of Circuits and Systems for a three-year period. He is also a consultant/advisor to statutory boards and multinational corporations in the areas of semiconductor devices, electronics, and integrated circuit design. He authored *Low-Voltage, Low-Power VLSI Subsystems* (McGraw-Hill, Int. ed., 2005), *Low-Voltage Low-Power Digital BiCMOS Circuits: Circuit Design, Comparative Study and Sensitivity Analysis* (Prentice-Hall, 2000, Int. ed.), and *CMOS/BiCMOS ULSI: Low-Voltage, Low-Power* (Prentice-Hall, NJ, 2002, Int. ed.). The latter was translated into a Chinese language version. He holds more than six patents and has additional patents pending. He has authored or coauthored over 200 papers on CMOS/BiCMOS technology and integrated circuit

design appearing in leading technical journals and conferences worldwide. He is a Technical Reviewer for several international journals. He was listed in Marquis' *Who's Who in the World* and Marquis' *Who's Who in Science and Engineering*.

Prof. Yeo was the technical chair of the 8th and 9th International Symposium on Integrated Circuits, Devices, and Systems (ISIC'99 and ISIC'01, respectively). He also served on the Program Committee of the International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA), Taiwan, R.O.C., and the International Symposium on Low-Power and High-Speed Chips (COOL Chips), in 1999 and 2002, respectively.

Wei Meng Lim received the B.E (Hons.) and M.E degrees from Nanyang Technology University (NTU), Singapore, in 2002 and 2004, respectively.

Upon graduation, he joined NTU as a Research Staff member. His research interests include RF circuit design, RF device characterization, and modeling.