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COMPUTER-AIDED DESIGN OF A MASS PRODUCTION CIRCUIT

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ABSTRACT

Tolerance of the circuit components can sometimes bring about costly consequences in mass production. To tackle this problem, recent efforts have been dedicated to develop tolerant circuit design in order to boost manufacturing yield [1]. To redesign a practical circuit successfully, a combination of many techniques is needed. This paper summarizes the techniques used in the redesigning of a practical mass production circuit that consider all the practical requirements. Experiments show that computer aided design along with tolerance design techniques are valuable tools in mass production.

1 INTRODUCTION

Sound identification circuit is used in color television set for switching off sound when amplitude of sound signal is rather slim or noise condemnation is fairly severe. Numerous malfunctioning circuits were found during mass production. Redesigning of such circuits is mandatory to achieve satisfactory yield. There three factors to consider in the redesigning process: first, simplification of the testing method which determines the length of time required; second, minimization of necessary modifications which dictates the amount of cost; and last but not least to strive for 100% yield.

This paper describes the procedure to achieve above goals. Before detailing the circuit redesigning process, a brief introduction to the yield evaluation and the centers of gravity (CoG) method [1] that are used in the yield optimization process is given in the following sections.

1.1 Centers of Gravity (CoG) Method

Iterative local search methods are the most commonly used optimization techniques in design centering. Among the iterative local search approaches used in tolerance design, the centers of gravity (CoG) method [1] stands out as the most popular and robust technique. Hence, in this paper, we choose to use CoG for circuit optimization. In this approach, Monte Carlo sampling is first performed within the tolerance region; the center of gravity of the parameter vectors associated to pass circuits is then calculated. Production yield is evaluated as the percentage of pass circuits in all the tested samples. The nominal design center, i.e. the parameter vector p^T , is then moved towards the center of pass

circuits. This process is repeated until the desired yield is attained or when the incremental yield improvement becomes very small.

2 FUNCTION OF THE CIRCUIT

Sound identification circuit, used in color televisions, functions like a switch. It controls when to amplify the sound and when to switch it off. When the incoming signal falls within specific range of amplitude and frequency, the output of the circuit is low. When the input signal's frequency and amplitude fall outside the specific range which indicates that there is no sound signal or that the sound signal is weak or noisy, the output of the circuit is high. The low/high output voltage level is used to switch on/off the sound.

2.1 The Circuit Model and its Nominal Performance

The model of the circuit, provided by an industrial partner, is shown in Fig. 1. The parameters of the circuit are omitted in this paper as required by our industrial partner. The circuit consists of three different amplification stages. The first stage amplifier amplifies specific frequency's signal which is defined by the frequency selector circuit L_1 and C_1 . Following the first amplification stage is a high pass filter, which is made up of capacitor C_2 and resistor R_4/R_5 . The second stage is a rectifier. Its time constant is determined by C_4 and R_8 . The output stage converts analog signal into high/low level. Transistor T_3 operates in cut off mode when there is a sound signal at input, and operates in saturation mode when there is no sound signal at input.

The input signal is amplified by the first stage amplifier if its frequency falls within the specific frequency range. The amplified signal is then integrated by the rectifier. The voltage of the capacitor C_4 gradually increases to certain voltage, which switches off the output transistor and the output of the circuit falls to a low level. This means sound signal is detected. When the signal presented at the input falls outside the frequency range, the first amplifier doesn't amplify the signal, and therefore the voltage at the capacitor C_4 is low. The output transistor works in saturation mode and the output voltage is at high level. When the incoming signal smaller than 0.4V, the signal after amplification is still

quite weak, the voltage of the capacitor C_4 is not high enough to switch the output transistor T_3 to cut-off mode and hence the output voltage is also high.

The nominal design performance is shown in Fig. 2 and Fig. 3. The input signal, in Fig. 2, is a sinusoidal signal with $0.4V$ amplitude and $505kHz$ frequency. Fig. 3 shows the corresponding output signal, which gradually decreases to a low level in $500\mu s$ time.

To test the performance of the nominal design, time domain simulation as shown in Fig. 2 and Fig. 3 are repeated with input signal, with different amplitudes and a constant frequency at $505kHz$. The input amplitude versus end point voltage at $500\mu s$ of the output in time domain is shown in Fig. 4. Similar simulations, with different frequency values and a constant amplitude equals to $0.4V$, are performed. The input frequency versus the end point voltage of the output at $500\mu s$ is shown in Fig. 5. Several additional simulations are performed to give detailed information between frequency $480kHz$ and $505kHz$ in Fig. 5.

2.2 Nominal Performance and its Problem

During the production of the circuit, a fairly large portion of the circuits failed to function properly. When there is no sound signal at input, some circuits' output voltages are low. This suggests that these circuits have wrongly identified the presence of a sound signal at the input. To illustrate this problem, we perform a 30 samples Monte Carlo simulation. The input signal is set to zero, i.e., no input sound signal. The time domain responses of the 30 sample circuits are plotted in Fig. 6. This figure shows that some curves gradually decrease to mid level and some decrease to low level. This phenomenon clearly shows that a portion of the circuits failed to detect the absence of sound signal at the input. Thus, redesigning the circuit is required.

3 CIRCUIT OPTIMIZATION PROCEDURE

3.1 The Problem in Optimizing the Circuit

In redesigning the circuit, repeated pass or fail testing of a sample circuit is needed. Sadly, evaluation of circuit performance is very time consuming process if we simply resort to the method described in evaluating nominal design, i.e., performing repetitive time domain analyses with dissimilar inputs and examine the end point voltage of the output.

One way to resolve this problem is to simplify the testing procedure by using relevant performance metrics that are faster to simulate. It is well known that time domain analysis is slow, whilst DC analysis is much faster.

Furthermore, the failure caused by absence of input signal, i.e., $V_{in} = 0$, that might be caused by the wrong working mode of the output transistor. The working mode of the transistor when $V_{in} = 0$ can be examined by DC analysis.

When there is no input, the output transistor should work in saturation mode. To verify if the output transistor always work in saturation mode when $V_{in} = 0$, a DC Monte Carlo analysis is carried out. The scatter plot of V_{ce} versus V_{out} is illustrated in the Fig. 7. From Fig. 7, it can be deduced that some of the sample circuits do not work in saturation mode. Therefore, the bias of output transistor is one of the reasons that cause the malfunction. We can use DC analysis and either $V_{ce} < -0.2V$ or $V_{out} > 4.8V$ as the testing condition to access whether a circuit is a pass circuit or a fail circuit. In the following study of the redesigning issue, DC analysis with $V_{out} > 4.8V$ is used as the testing criteria.

3.2 Trial and Error Study in Optimizing the Circuit Using CoG

As the simulation time is greatly reduced, several trials of optimizations are executed.

In the first trial, all the components are considered as designable parameters that could be modified during the optimization process, the tolerances of all the components are considered, 250 Monte Carlo sample points are used in each iteration. The yield is shown in Fig 8 (a).

Note that the maximum yield has not been improved significantly. In the second trial, three critical component's values (R_7 , R_8 , and R_9) which directly determine the working mode of the output transistor are considered as designable components. In order to see a clear trend of improving yield, we deliberately reduce the value of R_9 . The yield is plotted in Fig 8 (b). Although CoG does improve the yield, the result is still not satisfactory.

3.3 The Final Solution

In order to achieve the final goal, i.e. 100% yield with minimal modifications, we reduce the inter-component influence even further. We fixed all the other components at their nominal values, leaving only one designable variable. In other words, only one component's value could be modified and only one tolerance is considered. To accelerate the process of finding the global optimum, auto-focus technique [2] is used. The tolerance of R_9 is enlarged 5 times and then reduced to its original value in the next step. The yield is easily increased to 100% in just two iterations. The yield is shown in Fig. 8 (c).

The resistor value is increased by the optimization process. The amplification factor β of the output transistor T_3 may influence the output voltage significantly. So the β of T_3 is set to its worse case, and then a DC analysis is performed. The output voltage is lowered by setting β to its worse case. To make the circuit more robust, the resistor value of R_9 is further increased to an industry available value.

100% yield achieved using above procedure does not consider the tolerances of other components. To see whether increasing nominal value of R_9 is a good design, all the components' tolerances have to be considered and a Monte Carlo simulation using DC analysis is conducted. All the samples' outputs are high which means that 100% yield is achieved using DC analysis.

3.4 Verification of the redesigned circuit's performance

The circuit is now redesigned to attain 100% yield using the simplified testing criteria. To verify the performance of the circuit using the original criteria, a transient analysis Monte Carlo simulation with $V_{in} = 0$, is performed. The results are plotted in Fig. 9. All the output voltages are high. The nominal performance is also examined to meet the frequency and amplitude specifications, see Fig. 10 and Fig. 11, which give similar performances as shown in Fig. 4 and Fig. 5, and are verified to be acceptable by our industry partner.

4 CONCLUSION

Redesign the sound identification circuit is accomplished, i.e., 100% yield is achieved, by applying CoG method and auto-focus technique. The final solution is simple -- a single component's value must be altered. In the redesigning process, sensitivity analysis facilitates the simplification for pass or fail testing. Robustness of the circuit is considered by worst-case study and the component value to be modified is available in industry. It shows that tolerance design is very useful in mass production.

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Fig 1: The model of the sound identification circuit.

Fig. 2: Input signal to the sound identification circuit.

Fig. 3: Output response of the sound identification circuit.

Fig. 4: Steady state output voltage as a function of the amplitude of input signal (original circuit.)

Fig. 5: Steady state output voltage as a function of the frequency of input signal (original circuit.)

Fig 9: Responses of 30 sample circuits with input=0.

Fig. 6: Responses of 30 circuits of original design, input=0.

Fig. 10: Steady state output voltage as a function of the amplitude of input signal (redesigned circuit.)

Fig. 7: Vce versus Vout of the output transistor.

Fig. 11: Steady state output voltage as a function of the frequency of input signal (redesigned circuit.)

Fig. 8: Yield trajectory (1st 2nd 3rd attempt).