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The multiple temperature heater platforms for solder Electromigration test conducted at room temperature

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Abstract

To accommodate the increasing input-out (I/O) counts in future integrated circuits, the size of the solder bumps has to shrink and current density through each solder bump is increasing. With the ever-increasing current density through the solder bumps, electromigration (EM) remains as a main concern for the reliability of future solder bumps. This phenomenon is responsible for the structural damage of solder bumps in the form of void formation caused by ionic diffusion driven by high electron wind force.

Conventional solder bump EM test is performed in high temperature oven with high stress current. Besides the high cost oven, the total test time can be very long as the EM test has to be performed at several different temperatures and EM failure for solder bumps is usually much longer than their interconnect counterpart. In this work, we propose a multiple temperature heater platform for solder EM test conducted at room temperature. This platform eliminates the use of high cost oven. In addition, the solder joints can be tested at different temperatures simultaneously, shorting the total required EM test time. This proposal is verified by ANSYS[®] finite element simulations through the corresponding electrical-thermal analysis.

Introduction

For flip-chip packages, the solder interconnects serve as electrical and thermal paths as well as structural supports, which render its importance in the IC reliability where its degradation can seriously affect the functionality of the entire IC package.

On the other hand, the size of solder joints/bumps in IC packages is decreasing owing to the increase in the number of I/O contact pads on the chip in order to enhance the performance and functionality of electrical devices. This continuous down scaling of the size of the solder joint increases the current density through the joint, making electromigration (EM) a serious threat to the reliability of solder joints [1].

Electromigration of solder bumps is a failure mechanism that leads to increased resistance with accompanying events such as the formation of intermetallic compounds (IMC), voids and cracks that can disrupt the solder joint and silicon/package metallization leading into the bump. The driving forces for this EM failure are current density and elevated temperature. Typical solder EM test is performed in an oven at a constant high temperature with a constant current source. The highest temperature allowed in solder bump EM test is limited by the melting point of the solder alloy system, and as such, the device temperature should be kept to be at least 25 °C below the melting point.

The applied test current to the solder bump is also restricted. This is due to the geometry of the solder bump, and

there exists a current crowding region near the intersection of the chip interconnect and the solder bump where the current density changes abruptly in the solder bump. A non-uniform current density within the bump, particularly at the UBM interface, creates several complications affecting the time to failure for the bumps [2]. The current crowding can increase the temperature of the region significantly due to Joule heating. This Joule heating problem is more severe with a smaller dimension of the solder joint because the conductive heat transfer through the solder joint is lesser owing to the small surface area, making the heat dissipation less efficient.

Simulation of current density distribution in the solder bump of a flip chip structure showed that the current density in the current crowd region is much higher than the averaged current density inside the solder bump [1]. This current non-uniformity affects the spatial and temporal distributions of the intermetallic and void formation. The solder bump temperature can be very much larger than the ambient oven temperature under the Joule heating effect, leading to the thermo-migration failure in the solder bump [3] or local melt of the solder bump [4].

With the limitation in test temperature and current, the time taken for solder EM test can be very long. On the other hand, in order to obtain the activation energy E_a of the solder EM from the Black's equation [5], the solder bump EM test needs to be performed at three different temperatures. As a single solder EM test will take a long time, the determination of the E_a at three test temperatures will require a very long duration unless three ovens are used simultaneously. Besides, package level EM test in ovens requires special test boards and test sockets that are reliably at the high test temperatures. The cost of these ovens, boards and sockets are very high.

In this work, we propose a novel multiple-temperature heater platform for solder EM test conducted at room temperature, hence the use of high cost oven is eliminated. In addition, the solder bumps can be tested at different temperatures simultaneously, shorting the total EM test time. A heater is realized by implementing poly-Si stripes embedded in the Si die as heat sources. Due to the high resistivity of the Poly-Si stripes, moderate current is able to achieve a die temperature above 150 °C in ambient test environment. The temperature difference between solder bump and the heater is very small by assuming a one-dimensional heat conduction mechanism.[6] This will be verified in our 3-D solder bump simulations. This paper describes the details of the test platform as well as the simulation results by finite element analysis (FEA).

Model description

Eutectic SnPb solder is chosen for illustration in this work although the same methodology can be applied to other types of solder joints. The proposed test platform comprises of five

components: ceramic substrate, heater, solder balls, poly-Si stripes inside the heater, and Si chip. The schematic drawing of the model is shown in Fig. 1. It has a 5×5 solder ball array at 0.45 mm pitch. The number of the solder bumps in simulation is determined as a compromise between the simulation time and overall model accuracy. The component size is listed in Table 1. The structural parameter of the solder joint is shown in Table 2.

Fig. 1. Schematic drawing of the solder bump electromigration test platform.

Finite element model is constructed using ANSYS Workbench® and the simulation is carried out in the ANSYS Classic® environment. The geometry of the entire platform is drawn using the Design Modeler® in ANSYS Workbench® as shown in Fig. 2. The model is then meshed in workbench simulation environment with 4 node tetrahedral elements (solid69). The model after meshing is passed to ANSYS Classic® through ANSYS input files. There are 97391 nodes and 539441 elements in the model. The meshed model is shown in Fig. 3. The meshing density in solder bump is much higher than that in the substrate so the accuracy will not be sacrificed in the solder bumps. Si chip and underfill are removed for clearer illustration in Fig. 3. An individual meshed solder joint is shown in Fig. 4.

Table 1. Component dimensions

Component	Length (mm)	Width (mm)	Thickness (mm)
Si chip	1.6	1.6	0.3
Heater	1.6	1.6	0.3
Ceramic substrate	2	2	0.3
Poly Si	1.6	0.05	0.05

Table 2. Structural dimensions of the solder bump

Solder height	0.11 mm
Pad diameter	0.1 mm
Solder width	0.15 mm
Solder volume	1.5958×10 ⁻³ mm ³

Fig. 2. Geometry created by Design Modeler® for the solder bump electromigration test platform.

Fig. 3. Finite element model for the solder bump electromigration test platform.

Fig. 4. Finite element model for an individual solder bump.

Poly-Si stripes are embedded in the heater as heat generating sources and their layout will affect the temperature distribution of the whole EM test system. In this work, ten poly-Si stripes are placed horizontally in the heater as shown in Fig. 5. The three axial directions x, y, z are along the poly-Si length, width and thickness directions, respectively. During EM test, moderate current will be applied to the poly-Si stripes and the generated heat will be transferred to the solder bumps on top. Therefore, by controlling the amount of current applied to poly-Si stripes, the solder bumps can be heated to the desired EM test temperature. Also, the number of the poly-Si stripes powered will affect the temperature distribution of the heater and the solder bumps on top. The temperature distributions will be more uniform if more poly-Si stripes are powered simultaneously. It is noteworthy that the layout of the poly-Si can always be modified to meet the specific geometry of the solder bump test system in actual implementation in the future.

Fig. 5. The layout of poly silicon stripes.

Simulation results

ANSYS element *Solid69* is chosen for the coupled field electrical-thermal analysis. The electrical and thermal properties of the materials used in simulation are shown in Table 3. In the simulation, all materials are assumed to be homogenous and isotropic. The interfaces between different materials are assumed to be perfectly bonded.

Since simulation results are affected by the boundary conditions, it is critical to apply accurate boundary conditions to reflect the actual experimental test conditions. In the simulation, the substrate bottom is fixed at an ambient temperature of 25°C. The rest of the substrate surfaces are subject to natural convection with a convection coefficient of 10 W/mm²·K [7]. In order to obtain different temperature distribution over the solder bumps, current is applied only at two poly-Si stripes in the center of the heater. The steady state analysis show that with input poly-Si current of 250 mA, the solder bumps can be heated up to 170°C, which is suitable for eutectic SnPb EM test.

Table 3. Material properties used in the simulations

Component	Thermal conductivity (W/m·K)	Specific heat J/kg·K	Density Kg/m ³	Resistivity (μΩ·cm)
Copper	698	385	8960	1.7
Aluminum	232	900	8700	2.7
Ceramic	3	1112	3100	–
Underfill	0.2	2000	1630	–
Eutectic SnPb	50	190	8420	14.6
Silicon	61.9	702	2329	–
Poly-Si	61.9	702	2329	5100

The temperature distribution of the solder bumps on top of the heater is shown in Fig. 6. It can be seen that the solder bumps at the edge of the die are at a lower temperature than those at the center. This is because current is applied only to the two poly-Si stripes at the center of the chip in simulation. As shown in Fig. 6, the temperature distribution is more uniform along the poly-Si direction (x direction). The temperature distribution along y direction is non-uniform. Therefore, these solders can be tested simultaneously at different temperatures along the y direction. By performing the steady state analysis with different input current, the relationship between maximum solder bump temperature and input current is shown in Fig. 7. The maximum temperature in the solder bump is proportional to the square of input current, arising from the nature of the Joule heating effect. Figure 7 can be used to estimate the amount of input current needed to achieve a desired temperature in actual experiment.

In actual implementation, the temperature of the solder bump can be estimated through the temperature coefficient of resistivity (TCR) method with Cu thin films embedded near the solder bump [8]. For Cu metallization, TCR and R are linear below 200 °C, which can provide high accuracy for the temperature estimation.

Fig. 6. Temperature distribution of the solder bumps with an input current of 250mA. (Unit: degree)

Fig. 7. Maximum solder bump temperature change with the input current.

Figure 8 shows the temperature distribution across the heater surface for different amounts of input current applied to the poly-Si stripes. The temperature profile direction is along y axial direction. As shown in Fig. 8, the temperature at the center of the heater is the highest since only two poly-Si stripes at the center of the heater are powered. With decreasing poly-Si current, the temperature on top surface of the heater also decreases and the temperature distribution is more uniform.

Transient analysis is also performed to estimate the amount of time for the system to reach the steady state once the current is applied. This duration is also called thermal response time. Transient analysis is performed with the time duration of 10s and the sub-step is set at 0.1s. The simulated maximum solder bump temperature changing with time is shown in Fig. 9. It can be seen that the temperature increases dramatically initially and stabilizes to the steady state temperature in 5 seconds. The simulated thermal response time may be dependent on the finite element model and more verification is needed in our future work.

Fig. 8. Temperature distribution profile across the heater surface for different input current to the poly-Si stripes.

Fig. 9. Maximum solder bump temperature change with time simulated by transient thermal-electrical analysis.

Fig. 10. Temperature distribution profile across the heater surface for the case of different number of poly-Si stripes are powered.

Fig. 10 shows the temperature distribution profile across the heater surface for different number of poly-Si strips being powered along y axial direction. As shown in Fig. 10, with more number of poly-Si being powered, the temperature distribution is more uniform along y direction. In other words, the uniformity of the temperature distribution can be controlled by the number of poly-Si stripes powered during actual test.

Discussions and future works

It is well-known that the trace routing in the chip side to the solder bump introduces significant current crowding. The temperature gradient associated with the current crowding effect can be very large, leading to enhanced thermo-migration effects. It was reported that a temperature gradient of $0.15\text{ }^{\circ}\text{C}/\mu\text{m}$ is sufficient to cause thermo-migration in eutectic SnPb solder joints [9]. Therefore, it is necessary to examine the temperature gradient introduced by the heater in this design.

Fig. 11 shows the current density distribution for the solder bump with an input current density of $0.29\text{ MA}/\text{cm}^2$ in the Al

trace without applying any poly-Si current. It is obvious that the maximum current density site is located at the intersection of the chip interconnect and the solder bump. The Al trace has to be thick enough so that EM failure only occurs in the solder joint. Figure 12 shows the temperature gradient distribution for the same current applied in Fig. 11. The maximum temperature gradient site is located at the same location as the maximum current density site. This is because the temperature gradient is mainly contributed by the current crowding effect.

It is noteworthy that the maximum temperature gradient is $0.01\text{ }^{\circ}\text{C}/\mu\text{m}$ in Fig. 12, far below the value ($0.15\text{ }^{\circ}\text{C}/\mu\text{m}$) for thermo-migration to appear. With the heater current of 250 mA to the two poly-Si stripes in the center, the temperature gradients in the solder bump at the center and edge of the die are at a level of 0.145 and $0.1\text{ }^{\circ}\text{C}/\mu\text{m}$, respectively. Under such a high temperature gradient, the voiding from EM test may be contributed by thermo-migration, complicating the analysis.

In order to reduce the temperature gradient introduced by the poly-Si heater, the EM test platform can be modified slightly. As shown schematically in Fig. 1, poly-Si stripes can also be implemented in the Si Chip on top of the solder bumps. In this case, the poly-Si stripes at both sides of solder bumps contribute to the temperature gradient and the two temperature gradients can cancel each other in the solder bump, leading to reduced temperature gradient in the solder bumps. The verifications will be done in our future works.

Fig. 11. Current density distribution in the solder bump. (Unit: $\text{pA}/\mu\text{m}^2$)

Fig. 12. Temperature gradient distributions in the solder bump. (Unit: $^{\circ}\text{C}/\mu\text{m}$)

Conclusions

In this work, we propose a multiple temperature heater platform for solder EM test conducted at room temperature. This platform eliminates the use of high cost oven. In addition, the solder joints can be tested at different temperatures simultaneously, shorting the total required EM test time. This proposal has been verified by ANSYS[®] finite element simulations through the corresponding electrical-thermal analysis.

The proposed solder EM test platform has three advantages. Firstly, solder bump can reach a high temperature by controlling the heater input current. Hence, the test current can be reduced under such high temperature without compromise on the EM failure time. Secondly, solder bumps can be tested on EM at different temperatures simultaneously. This is achieved by controlling the layout of the poly-Si stripes in the heater so that the top surface of the heater is at different temperatures with the edge of the die at a lower temperature than that at the center. Therefore solder bump at center of the heater will be tested at higher temperature than that at the edge. Lastly, the EM test can be carried out at room temperature, eliminating the use of high-cost oven.

To reduce the temperature gradient in the solder bump contributed by the heater, poly-Si stripes can be implemented in the chip on top of the solder bumps. The temperature gradients produced from both sides of poly-Si stripes can cancel each other, leading to reduced temperature gradient. This will be done in our future works.

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