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A Scalable RFCMOS Noise Model

Ah Fatt Tong, Wei Meng Lim, Kiat Seng Yeo, Choon Beng Sia, and Wen Cong Zhou

Abstract—This paper presents the high-frequency (HF) noise modeling of an RF MOSFET for a 90-nm technology node. A brief discussion on the noise measurement theory is presented to illustrate the limitation of the noise measurement system. The extracted noise sources were studied for their geometry and biasing dependences and by implementing additional noise sources into the small-signal RFCMOS model, accurate HF noise simulation for the transistor can be achieved. Verilog-A is used for the coding of the additional noise sources into the RFCMOS model and the added noise source will compensate the underestimation of the channel thermal noise from the BSIM3v3 core model. Simulated noise circles and the measured noise figures are plotted at other source impedances to show that all the noise parameters are simulated accurately. The biasing and geometry dependences of the measured and simulated noise parameters are presented to demonstrate the scalability of the developed HF noise model. The scalability feature in HF noise model can be implemented into the process design kit (PDK) so that more powerful PDK can be developed for the circuit designers to optimize and simulate their circuit design that requires stringent noise specifications. The accurate noise simulation can ensure better chance of success and reduce the number of tape-out and design cycle time.

Index Terms—BSIM3v3, high-frequency (HF) noise model, HF noise modeling, RF MOSFET, RFCMOS, Verilog-A.

I. INTRODUCTION

A SCALABLE RFCMOS model is typically formed by using a macromodeling approach whereby sub-circuit components are added into the BSIM core model as a structure parasitic that only appears at the RF frequency region. By forming geometrical equations for each of these sub-circuit components, the developed RFCMOS model can predict its dc, S -parameters, and flicker noise for a range of device geometry, biasing, and frequency. The geometry scalability of the RFCMOS model has allowed circuit designers to have more flexibility in choosing the device sizes that they need in the circuit design and by incorporating such scalability feature into the process design kit (PDK), it can improve the

design optimization process, and shorten the design cycle time. However, the model simulation capability for the transistor's high-frequency (HF) noise performance is still limited by the BSIM core model that underestimate the HF noise for short channel devices. The transistor's HF noise has been widely studied and many methods were proposed to improve its model simulation. In order to obtain accurate HF noise simulation, noise sources were proposed to be added into the RF model to compensate the underestimation from the BSIM core model. By monitoring the trend of the noise sources and implementing them using Verilog-A, accurate and scalable HF noise modeling can be achieved. Furthermore, the scalable HF noise model allows more powerful PDK to be developed so that the optimum device size based on its dc, S -parameters, and noise performances can be selected to use in a critical RF block such as the low-noise amplifier (LNA).

Presently, the selection of the transistor for the LNA design is normally based on the measured noise parameters provided by the foundry. However, the foundry is not able to provide the measured noise parameters for all different geometry and biasing combinations. Therefore, in cases where there is no measured noise data provided for a certain geometry and biasing point, the noise performance of such circuit design is usually unknown and this will raise the risk of not meeting the noise specification required by the RF chip and increase the required number of tape-out and design cycle time. Hence, it is critical to develop an accurate and scalable HF noise model such that a more accurate prediction of the RF circuit's performance can be simulated before sending them for fabrication.

Although HF noise modeling has been widely studied and researched, in most of the published papers, they mainly demonstrated HF noise model fitting at a fixed device size and a few biasing points [1]–[6]. The objective of this paper is to demonstrate scalable HF noise modeling for RFCMOS for a range of geometry sizes, biasing, and frequency points. The extracted noise sources were studied for its geometry, biasing, and frequency dependences; thus, by coding additional noise sources into the model file using Verilog-A, a scalable HF noise model can be generated. Section II shows the measurement setup and test structures used for the HF noise measurement. By using the MATLAB program, the pads and interconnects noise are embedded to obtain the true device noise parameters. The effect of ground metal shielding on the pads and interconnects affect the noise parameters slightly due to better shielding from the substrate's noise that causes degradation to the noise performance of the transistor. A brief review on the measurement theory is presented to study the measurement setup limitations that may explain the irregular fluctuating of the measured NF_{min} parameter versus frequency for small device sizes and low biasing points. Section III shows the transistor's equivalent circuit model used for its noise source extraction, and the geometry

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Fig. 1. ATN NP5 microwave noise parameter system.

and biasing dependences of the extracted noise sources are presented. The behavior of the extracted noise sources for different transistor geometry and biasing points can be explained by using the classical RF noise model, and this shows that the extracted noise sources results are reliable. Finally in Section IV, the additional noise sources implemented into the RF model is presented and these noise sources are implemented using Verilog-A to introduce their geometry and biasing effects and improve the fitting of the HF noise model. The measured and simulated noise parameters are shown to be scalable for a range of geometry, biasing, and frequency points. In addition, the accuracy of the developed scalable HF noise model is demonstrated by plotting the measured noise figures at other source impedance states with the simulated noise circles.

II. HF NOISE MEASUREMENT AND PARASITIC DEEMBEDDING

A. Test Setup and Parasitic Deembedding

Fig. 1 shows the measurement system of ATN NP5 used for HF noise and S -parameters measurement. The frequency module of 2–26.5 GHz was used. In this study, the devices-under-test (DUTs) are thin gate NMOS transistors that have a fixed channel length (L_g) of 70 nm, unit width (W_f) of 1, 2.5, and 5 μm and finger number (N_f) of 4, 16, 32, and 64. The RF transistor and its standard OPEN and SHORT deembedding structures were measured at various bias combinations of the gate to source (V_{gs}) and drain to source (V_{ds}) potentials for a range of frequency points. By using the reported technique in [7] and [8], the pads and interconnects parasitic that contributed to the measured HF noise and S -parameters can be removed to obtain the intrinsic transistor characteristics.

Fig. 2 shows the four noise parameters before and after deembedding of the pads and interconnects parasitic. It is shown that

Fig. 2. Noise parameters: (a) $NF_{\min}$ and r_n and (b) $\text{real}(\Gamma_{\text{opt}})$ and $\text{imag}(\Gamma_{\text{opt}})$ before (solid line) and after (symbols) deembedding of the pads and interconnects parasitic for transistor with N_f of 32, W_f of 5 μm , and L_g of 70 nm at $V_{gs} = 0.95$ and $V_{ds} = 1.2$ V.

the effect of the pads and interconnects affect the noise parameters slightly. This is because in the test structures, the design of the pads and interconnects are shielded with ground metal and it has been published in the literature that such a layout design is capable of shielding the wafer surface from the substrate's noise that can degrade the measured noise figure of the DUT [9].

Fig. 3 shows the simplified layout of the RF NMOS transistor. The transistor has a multifinger configuration with double contacted gate poly structure. Dummy gate poly is added to improve the gate structure formation and metals 1 and 2 are used for the connection of the gate terminal. The source diffusions are connected using the metal 1 layer and shorted to the body terminal or P-well while the drain diffusions are pulled out using the metal 3 layer.

Fig. 3. Simplified RF NMOS layout.

B. ATN NP5 Measurement Theory

Basically, the transistor's noise figure (F) is dependent on the four noise parameters and the source reflection coefficient (Γ_s), shown in (1) as follows:

$$F = F_{\min} + \frac{4 \cdot r_n \cdot |\Gamma_s - \Gamma_{\text{opt}}|^2}{(1 - |\Gamma_s|^2) \cdot |1 + \Gamma_{\text{opt}}|^2}. \quad (1)$$

The variable $F_{\min}$ is the linear term of minimum noise figure when the complex source reflection coefficient (Γ_s) is matched to the optimum complex source reflection coefficient (Γ_{opt}) and r_n is the normalized noise resistance, which is a measure of how sensitive the transistor's noise figure to the source mismatch from Γ_{opt} . It is obvious that for low-noise transistor performance smaller $F_{\min}$ and r_n is desirable. From (1), the noise parameters that need to be extracted are $F_{\min}$, r_n , and the real and imaginary term of Γ_{opt} . In principle, since four variables are required to be extracted, only four measurements at different Γ_s are required, but in practice, normally 16 measurements are done to increase the accuracy of the noise parameters extraction.

During noise measurement, the measured noise figure includes both the measurement system and the DUT. In order to obtain the noise parameters of the DUT, the noise contribution from the measurement system (F_{sys}) has to be determined during the calibration stage so that it can be removed automatically by the measurement software. During noise measurement, the total noise figure (F_{total}) at different source impedance states is measured and by using the Friis cascade equation [10] in (2), the DUT noise figure (F_{dut}) can be calculated. Note that G_{dut} is the available gain of the DUT

$$F_{\text{dut}} = F_{\text{total}} - \frac{F_{\text{sys}} - 1}{G_{\text{dut}}}. \quad (2)$$

As the ATN measurement system uses the Friis equation to extract the noise figure of the DUT, the measurement accuracy will be greatly dependent on the measured G_{dut} . For example, if F_{sys} is large and G_{dut} is small, the second term in (2) will be large and F_{dut} will be the subtraction of two large numbers; hence, this will lead F_{dut} to be very sensitive to measurement errors. Furthermore, the accuracy of measured F_{dut} will, in turn, affect the extraction of the $F_{\min}$ parameter in (1). Therefore, it is expected that for measurement of small device sizes with low G_{dut} values, their $F_{\min}$ is typically less than 1 dB. Thus, the extraction of $F_{\min}$ will be a challenge under such conditions.

Fig. 4. Noise parameters: (a) $NF_{\min}$ and r_n and (b) $\text{real}(\Gamma_{\text{opt}})$ and $\text{imag}(\Gamma_{\text{opt}})$ before (solid line) and after (symbols) deembedding for transistor with N_f of 32, W_f of 1 μm , and L_g of 70 nm at $V_{\text{gs}} = 0.95$ and $V_{\text{ds}} = 1.2$ V.

Fig. 4 shows the extracted noise parameters for a transistor with N_f of 32, W_f of 1 μm , and L_g of 70 nm. The extraction of the noise parameters were done at the same biasing condition as in Fig. 2. It is shown that the extracted $NF_{\min}$ become fluctuating and does not have a clear upward trend with respect to the frequency. However, the extraction of the parameter r_n and Γ_{opt} are not affected in the measurement. It is suspected that such extracted behavior of the $NF_{\min}$ parameter is due to the measurement limitation of the ATN system, as discussed in (2). Hence, due to the measurement system limitation, the extraction of $NF_{\min}$ for small device sizes, the low biasing points will have such an irregular trend of $NF_{\min}$ versus frequency.

Fig. 5 shows the measured and simulated dc characteristics for the transistor with N_f of 32, W_f of 1 μm , and L_g of 70 nm. The measured dc results show that the device used for the noise measurement is operating correctly. Another possible explanation for the fluctuation in the extracted $NF_{\min}$ is that the source impedance state used for the noise measurement falls either in

Fig. 5. DC characteristics: (a) g_m versus V_{gs} and (b) I_{ds} versus V_{ds} with measured (symbols) and simulated (solid line) data for transistor with N_f of 32, W_f of $1\ \mu\text{m}$, and L_g of 70 nm.

Fig. 6. Proposed RFCMOS model with extrinsic parasitic resistance noise, intrinsic induced gate noise ($i_{g_g}^2$) and channel thermal noise ($i_{d_d}^2$).

the “conditionally stable” or “unstable” region. This will also cause errors in the measured noise figures for each of the source impedance states during the noise measurement. As NF_{min} is extracted from these measured noise figures, the fitted NF_{min}

Fig. 7. Extracted noise sources: (a) $i_{d_d}^2$, (b) $i_{g_g}^2$, and (c) $i_{g_g} i_{d_d}^*$ versus frequency for transistors with N_f of 4, 16, 32, and 64 at fixed W_f of $5\ \mu\text{m}$ and L_g of 70 nm (extracted at $V_{gs} = 0.55\ \text{V}$ and $V_{ds} = 1.2\ \text{V}$). $\diamond$ Finger 4. $\times$ Finger 16. $\square$ Finger 32. $\triangle$ Finger 64.

curve may contain such errors and cause it to fluctuate, as shown in Fig. 4(a).

Fig. 8. Extracted noise sources: (a) $\overline{i_d^2}$, (b) $\overline{i_g^2}$, and (c) $\overline{i_g i_d^*}$ versus W_f for transistors with N_f of 4, 16, 32, and 64 at fixed L_g of 70 nm (extracted at $V_{gs} = 0.55$ V, $V_{ds} = 1.2$ V and frequency = 5 GHz). $\diamond$ Finger 4. $\times$ Finger 16. $\square$ Finger 32. $\triangle$ Finger 64.

III. NOISE SOURCE EXTRACTION

Fig. 6 shows an RFCMOS model that has all the extrinsic parasitic components and their corresponding resistance noise, the intrinsic induced gate ($\overline{i_g^2}$), and channel thermal ($\overline{i_d^2}$) noise sources. By using the reported noise source extraction technique

Fig. 9. Extracted noise sources: (a) $\overline{i_d^2}$, (b) $\overline{i_g^2}$, and (c) $\overline{i_g i_d^*}$ versus V_{gs} for transistors with N_f of 4, 16, 32, and 64 at fixed W_f of 5 μm and L_g of 70 nm (extracted at $V_{ds} = 1.2$ V and frequency = 5 GHz). $\diamond$ Finger 4. $\times$ Finger 16. $\square$ Finger 32. $\triangle$ Finger 64.

in [11], the intrinsic noise source $\overline{i_g^2}$ and $\overline{i_d^2}$ and their cross-correlation term ($\overline{i_g i_d^*}$) can be extracted from the measured S -parameters and noise measurements. In this extraction technique, the measured noise parameters were deembedded from its pads and interconnect noise and by using the correlation matrix in [12] and [13], the extrinsic parasitic resistance noise sources can

Fig. 10. RF equivalent-circuit model with added enhanced noise current $\overline{i_{de}^2}$ and induced gate noise current $\overline{i_g^2}$.

Fig. 11. Equivalent noise circuit: (a) $\overline{i_{de}^2}$ and (b) $\overline{i_g^2}$ that generate additional noise current [2].

be deembedded and obtain the intrinsic noise portion, as indicated in Fig. 6. $\overline{i_g^2}$, $\overline{i_d^2}$ and $\overline{i_g i_d^*}$ can be calculated using the equations given in [11]. As the extraction technique uses the extrinsic resistances for the noise deembedding, the accuracy of the extracted $\overline{i_g^2}$, $\overline{i_d^2}$, and $\overline{i_g i_d^*}$ will strongly depend on the accuracy of the extrinsic resistances values. Hence, it is crucial that the small-signal RF transistor model must be modeled accurately before the noise source extraction can be done.

In the classical RF noise model from Van Der Ziel [14], [15], the expression for $\overline{i_d^2}$ and $\overline{i_g^2}$ are given as follows in (3) and (4), respectively:

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f \quad (3)$$

$$\overline{i_g^2} = 4kT\delta \left(\frac{\omega^2 C_{gs}^2}{5g_{d0}} \right) \Delta f \quad (4)$$

$$\overline{i_g i_d^*} = c \cdot \sqrt{\overline{i_g^2} \overline{i_d^2}}. \quad (5)$$

In (3), the parameter g_{d0} is the drain-source conductance at zero V_{ds} . γ is the noise factor and has a value of unity at zero V_{ds} . In long channel devices, γ decreases to a value of 2/3 in the saturation region. Note that for short channel devices that operate in the saturation region, γ can be considerably higher

Fig. 12. Measured (symbol) and simulated (solid and dash line) noise parameters versus frequency for transistor with N_f of 32, W_f of 5 μm , and L_g of 70 nm (extracted at $V_{gs} = 1.2$ V and $V_{ds} = 1.2$ V).

than the long channel value. In (4), the parameter δ is the gate noise coefficient and it is given a value of 4/3 in [14]. The factor

Fig. 13. Measured (symbol) and simulated (solid line) noise parameters versus frequency for transistor with N_f of 32, W_f of 5 μm , and L_g of 70 nm (extracted $V_{ds} = 0.5$ V @ $V_{gs} = 0.55, 0.95$, and 1.2 V).

c in (5) represents the correlation between the noise $\overline{i_d^2}$ and $\overline{i_g^2}$. By studying the geometry dependence of g_{do} and C_{gs} in (3) and (4), it is found that $\overline{i_d^2}$, $\overline{i_g^2}$, and $\overline{i_g i_d^*}$ is proportional to $(N_f W_f / L_g)$, $N_f W_f L_g^3$, and $N_f W_f L_g$, respectively. Furthermore, in terms of frequency (f) dependences, it is clear that $\overline{i_d^2}$ is frequency independent, while $\overline{i_g^2}$ and $\overline{i_g i_d^*}$ are proportional to f^2 and f , respectively. The frequency and geometry dependences plots for the noise sources are shown in Figs. 7 and 8. The plots in Figs. 7 and 8 clearly validate the above discussion on the frequency and geometry dependences of the noise sources.

Fig. 14. Measured (symbol) and simulated (solid line) noise parameters versus frequency for transistor with N_f of 32, W_f of 5 μm , and L_g of 70 nm (extracted $V_{ds} = 1.2$ V @ $V_{gs} = 0.55, 0.95$, and 1.2 V).

The biasing dependence of the extracted noise sources $\overline{i_d^2}$, $\overline{i_g^2}$, and $\overline{i_g i_d^*}$ is shown in Fig. 9. It is shown that $\overline{i_d^2}$ increases when V_{gs} increases in Fig. 9(a). This is mainly due to the higher output conductance when V_{gs} increases at a fixed V_{ds} biasing point [1]. As $\overline{i_g^2}$ is mainly the coupled thermal noise from the channel through the gate capacitance to the gate structure, it is strongly dependent on the gate capacitance and is less sensitive to the biasing applied in the channel. Hence, in Fig. 9(b), it shows that $\overline{i_g^2}$ has little changes when V_{gs} increases. Note that the correlation noise $\overline{i_g i_d^*}$ follows the V_{gs} dependence of $\overline{i_d^2}$.

Fig. 15. Simulated noise circles and measured noise figures at different source impedance states for transistor with N_f of 32, W_f of $5 \mu\text{m}$, and L_g of 70 nm . (a) $V_{ds} = 1.2 \text{ V}$, $V_{gs} = 0.55 \text{ V}$. (b) $V_{ds} = V_{gs} = 1.2$ (extracted at frequency = 5 GHz).

IV. HF NOISE MODELING

In most compact models, their HF noise model equations are implemented into their core models and circuit simulators are designed to recognize these model equations when it perform simulations using these models. When the implemented noise model equations underestimate the noise performance of the transistor [4], it is usually very difficult for modeling engineers to go into the core models to change the model's equations, and such changes may require similar modifications to be done on the device simulators, which only the software vendor can carry out. Hence, in order to compensate the underestimation of the compact noise models, it is proposed to add in additional noise sources into the RF model using the sub-circuit approach [2]. In this paper, the noise implementation is done using a BSIM3v3 compact model.

A. Noise Source Implementation

Fig. 10 shows the RF equivalent-circuit model with added enhanced noise current $\overline{i_{de}^2}$ and induced gate noise current $\overline{i_g^2}$.

Fig. 16. Simulated noise circles and measured noise figures at different source impedance states for transistor: (a) $N_f = 4$, $W_f = 1 \mu\text{m}$, (b) $N_f = 64$, $W_f = 1 \mu\text{m}$.

Note that the correlation noise current $\overline{i_{g d}^*}$ is not added into the RF model because most circuit simulators are unable to process the correlation noise sources.

In [2], the following equations are derived to extract the component values of R_{de} , R_{ind} , and C_{ind} of the equivalent noise circuits, as shown in Fig. 11:

$$R_{de} = \frac{4kT}{\overline{i_d^2} - \overline{i_{dBSIM}^2}} \quad (6)$$

$$C_{ind} = 100 \cdot \frac{P_{ind} \cdot f_{max}}{8kT\pi} \quad (7)$$

$$R_{ind} = \frac{P_{ind}}{16kT\pi^2 C_{ind}^2} \quad (8)$$

$$P_{ind} = \frac{\overline{i_g^2}}{f^2}. \quad (9)$$

Note that $\overline{i_{dBSIM}^2}$ is the simulated channel thermal noise current of the BSIM3v3 core model and f_{max} is the maximum frequency for the noise model to be valid.

Although the equivalent-circuit model in Fig. 10 is different from the proposed equivalent-circuit model in [2], a similar technique to implement the noise sources can be applied.

Fig. 16. (Continued.) Simulated noise circles and measured noise figures at different source impedance states for transistor: (e) $N_f = 4$, $W_f = 5 \mu\text{m}$, and (f) $N_f = 64$, $W_f = 5 \mu\text{m}$ at fixed L_g of 70 nm (extracted at $V_{gs} = V_{ds} = 1.2$ V and frequency = 5 GHz).

The same modeling approach for the scalable HF noise model can be applied to the RF circuit design tools such as Cadence, Advanced Design System (ADS), and Microwave Office (MWO). In their circuit simulators, the CCCS component can be described with geometry and biasing equations and they are added into the RF MOS model to generate the required additional noise current during the HF noise simulation. Therefore, accurate and scalable HF noise simulation can be achieved and give better prediction for noise performance of the designed RF circuit blocks.

The implemented noise sources together with the RF model are simulated and compared with the measured noise parameters in Fig. 12. In this experiment, the Cadence Spectre simulator is used for the simulation of the HF noise parameters.

Fig. 12 shows a comparison between the measured and simulated noise parameters versus frequency for a transistor with N_f of 32, W_f of $5\ \mu\text{m}$, and L_g of 70 nm. It is observed that the simulated (dashed line) noise parameters for the RF model with no additional noise sources added underestimate the following noise parameters: $\text{NF}_{\min}$, r_n , and $\text{imag}(\Gamma_{\text{opt}})$. By performing the noise source implementation [2] as shown in this section, the simulated (solid line) noise parameters fit closely to the measured results throughout the whole frequency range. By using Verilog-A, the V_{gs} and V_{ds} biasing dependences can be coded into the CCCS component so that the added noise source will vary when the biasing is changed. The biasing dependences of the noise parameters are shown in Figs. 13 and 14. It is shown

Fig. 17. Measured (symbol) and simulated (dashed line) noise parameters versus biasing for transistors with W_f (1, 2.5, and 5 μm) at fixed N_f of 32 (extracted at $V_{ds} = 1.2$ V and frequency = 5 GHz). W_f $\blacktriangle$ 1 μm , $\blacksquare$ 2.5 μm , $\bullet$ 5 μm .

that the simulated noise parameters can vary with biasing and are able to predict the measured results well.

In order to demonstrate the accuracy of the generated HF noise model, the simulated noise circles (dotted line) and the measured noise figures (symbol) at the other source impedance states are plotted in Fig. 15. It is observed that the simulated noise circles can closely predict the measured noise figures at various source impedance states. Thus, it demonstrates the accuracy of the simulated noise parameters.

Due to the possibility of measurement system limitation, as discussed in Section II, it is very difficult to measure very good NF_{min} data for small width devices at the various biasing conditions. However, it is shown in Fig. 4 that the measured parameters r_n and Γ_{opt} are not affected in the measurement. Therefore, in order to show the geometry scalability of the developed HF noise model, the simulated noise circles for the small devices are plotted with their measured noise figures at other source impedance states for comparison. As r_n and Γ_{opt} are not affected by the measurement system, its geometry (N_f and W_f) and biasing dependences are plotted to show the scalability of the developed HF noise model.

Fig. 16 shows the simulated noise circles and measured noise figures at other source impedance states for various transistors' geometry N_f and W_f . It has shown that the simulated noise circles can predict accurately for small (N_f of 4 with W_f of 1, 2.5, and 5 μm) and large (N_f of 64 with W_f of 1, 2.5, and

Fig. 18. Measured (symbol) and simulated (dash line) noise parameters versus transistors' geometry with N_f (4, 16, 32, and 64) and W_f (1, 2.5, and 5 μm) (extracted at $V_{gs} = V_{ds} = 1.2$ V and frequency = 5 GHz). W_f $\blacktriangle$ 1 μm , $\blacksquare$ 2.5 μm , $\bullet$ 5 μm .

5 μm) transistors. This further demonstrates that all the noise parameters NF_{min} , r_n , and Γ_{opt} are simulated accurately for the above geometry ranges.

In Figs. 17 and 18, the measured and simulated noise parameters r_n and Γ_{opt} are plotted versus biasing and transistor's geometry, respectively. Both figures show that the simulated results can predict the measured values for the above range of biasing, N_f and W_f . Therefore, from the plots presented in Figs. 13–18, it has demonstrated that a scalable HF noise model was achieved in this work for various biasing and transistor's geometry.

V. CONCLUSION

In most of the literature reports, the HF noise model is normally demonstrated for one or few device sizes and some biasing points for a range of frequency, but in order for the HF noise model to be applicable to the industry, it has to be able to simulate for a range of geometry, biasing, and frequency points. Hence, in this paper, the scalability of the HF noise model is shown with good accuracy up to 26 GHz for all four of the noise parameters at a different geometry combination of N_f and W_f and at a range of biasing points.

Furthermore, to show the accuracy of the developed scalable HF noise model, its simulated noise circles are plotted against the measured noise figures at other source impedance states and

it has demonstrated that good fitting was achieved between the measured and simulated results. The effect of the metal ground shielding on the pads and interconnects shows that it is able to shield the transistor from the substrate noise sources. The fluctuating of the measured $NF_{\min}$ versus frequency trend for the small devices is explained with the measurement theory and setup. Although the $NF_{\min}$ parameter is fluctuating with frequency, the other three noise parameters (r_n , $\text{real}(\Gamma_{\text{opt}})$ and $\text{imag}(\Gamma_{\text{opt}})$) can be used to demonstrate the HF noise model fitting between the simulated and the measured results.

Finally, the scalability of the HF noise model can help the circuit designers to optimize their design and run accurate simulations to ensure its circuit performances are within the chip specifications before sending them for fabrication. This can greatly enhance the chance of first time success in tape-out and reduce the design cycle time for those RF chips that has critical noise specifications.

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