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A High-Speed Twin-Capacitor BiNMOS (TC-BiNMOS) Logic Circuit for Single Battery Operation

Kiat-Seng Yeo, Heng-Kah Lee, *Student Member, IEEE*, and Manh-Anh Do

Abstract—This paper presents a novel BiNMOS logic gate specially designed for single battery operation (1.2–1.5 V). Through the use of two capacitors, in the pre-charging and bootstrapping cycles, the circuit achieves a high-speed and full-swing operation. Analytical expressions for the circuit were derived, and the main design considerations were addressed. Based on a 0.5 μm BiCMOS technology, HSPICE simulation results have proven the superiority of the new circuit over the CMOS, BFBiNMOS and BSBiNMOS circuits in terms of speed and power consumption. The circuit also occupies the smallest area amongst the BiNMOS families. A 75-stage ring oscillator of the new circuit was fabricated using a 0.8 μm BiCMOS process, and the measured gate delay/stage is merely 1.32 ns at a supply voltage of 1.5 V and a load capacitance of 1 pF.

Index Terms—Circuit analysis and testing, fabrication, low-voltage digital BiNMOS design, simulation.

I. INTRODUCTION

OVER the years, the demand for high performance digital applications has increased significantly to meet the needs for present and future large-scale computations. Meanwhile, for every generation, the power consumption increases tremendously with the integration density and operating frequency. Hence, efficient power management in digital circuit design is essential. An effective measure to cut down the power consumption and to extend the battery life of portable devices is to reduce the supply voltage [1]. However, this results in a drastic increase in the delay especially when the supply voltage is scaled down to 1.5 V [2].

It is a well-known fact that BiCMOS technology has been used to implement high-performance logic circuits [3]. Nevertheless, when the supply voltage goes below 3 V, its leverage over the CMOS, in particular the speed and output voltage swing, starts to diminish. So far, a few BiCMOS designs have improved the performance of the BiCMOS circuit for low-voltage operation [3]–[9]. However, there are still many shortcomings associated with these circuits. For instance, several BiCMOS circuits use shunting elements across the base–emitter or the collector–emitter junctions of the output bipolar transistor to realize full-swing operation, but at the expense of a poor rise response [4]. While the circuit reported

in [5] requires a complementary BiCMOS process, the BS-BiCMOS [6] suffers from high crossover capacitance/fanout [7]. Others involve additional circuits like pre-charge level generator, and charge pump circuit to supply secondary voltage that is higher than the primary supply voltage [8], [9].

II. CIRCUIT DESCRIPTION AND OPERATION

Fig. 1 shows the proposed twin-capacitor BiNMOS (TC-BiNMOS) inverter. It can be fabricated using a standard noncomplementary BiCMOS process. During the pull down or pre-charge cycle, when the input rises from low to high, MN3 turns on to discharge the output node. Once the output voltage is low, MP1 conducts and starts to charge up $C_{\text{boot}2}$ to V_{DD} . Concurrently, $C_{\text{boot}1}$ is pre-charged to $(V_{DD} - V_{T(\text{MN}1)})$ through MN1 and MN2. For a 0.8 μm BiCMOS technology and a supply voltage of less than 1.5 V, the voltage at node b is less than $V_{BE(\text{on})}$, therefore $Q1$ remains off. During the pull-up cycle, when the input goes low, MP2 conducts and connects $C_{\text{boot}1}$ and $C_{\text{boot}2}$ in series. The initial charge stored separately in these capacitors will be redistributed, and hence the resultant voltage at the base of $Q1$ will go beyond V_{DD} . Once $Q1$ turns on, it starts to charge up the output node. The positive feedback loop formed by $Q1$, $C_{\text{boot}1}$, MP2 and $C_{\text{boot}2}$ speeds up the charging process. Transistor MPU is necessary to ensure that the output voltage remains at the correct logic when $Q1$ cuts off. The simulated waveforms at a supply voltage of 1.5 V and a load of 1 pF are shown in Fig. 2.

Two pre-charging mechanisms occur simultaneously during the pre-charge cycle. The first one pre-charges the voltage at node b to near $V_{BE(\text{on})}$ and hence shortens the turn-on time of $Q1$. The second one pre-charges the voltage at node a to V_{DD} and, when coupled with the first, enables the base voltage of $Q1$ to be boosted to a voltage higher than V_{DD} when MP2 turns on. Consequently, as illustrated in Fig. 2, the output voltage achieves a full swing in a very short time. Fig. 3(a)–(c) shows the equivalent circuit models during the pre-charge, at the beginning of and during the bootstrapping cycles respectively, where

$$V_{EQ} = (C_{\text{boot}1} (V_{DD} - V_{T(\text{MN}1)}) + C_{\text{boot}2} V_{DD}) \times \frac{C_{\text{boot}1} + C_{\text{boot}2}}{C_{\text{boot}1} C_{\text{boot}2}}. \quad (1)$$

In the pre-charge cycle, let the initial charges stored in $C_{\text{boot}1}$

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Fig. 1. The proposed twin-capacitor BiMOS (TC-BiMOS) inverter.

Fig. 2. The key voltage waveforms of the TC-BiMOS inverter.

and C_{boot2} respectively be

$$Q_1 = C_{boot1} (V_{DD} - V_{T(MN1)}) \quad (2)$$

$$Q_2 = C_{boot2} V_{DD}. \quad (3)$$

At the beginning of the bootstrapping cycle, when MP2 conducts, the equivalent capacitance at node b is

$$C_{EQ} = \frac{C_{boot1} C_{boot2}}{C_{boot1} + C_{boot2}} \quad (4)$$

and the voltage at node b due to the charge redistribution is given by

$$V_b = V_{EQ} \times \frac{C_{EQ}}{C_{EQ} + C_X} \quad (5)$$

where C_X represents the parasitic capacitance at node b that includes the output load capacitance (C_L/β), source capacitance of MN1, and base-emitter and base-collector capacitances of Q1.

Fig. 3. Simplified equivalent circuits to explain the functions of C_{boot1} and C_{boot2} during : (a) Pre-charge (b) Beginning of the bootstrapping (c) Bootstrapping cycles.

Fig. 4. The effect of the pre-charge voltage on the propagation delay and power dissipation.

During the bootstrapping cycle, as illustrated in Fig. 3(c), when the output voltage rises from low to high, the voltage at node a will rise even higher. This effect will, in turn, boost up the voltage at node b to a level that is high enough to overcome the V_{BE} barrier of $Q1$ and hence allows the output voltage to achieve a full swing.

III. DESIGN CONSIDERATION

A. Pre-Charge Voltage at Node a

The pre-charge voltage at node a depends on the charging time t_c of C_{boot2} . Assuming the circuit operates at a frequency f , which corresponds to a period T , with a fall time of t_f , and

Fig. 5. The amplitude of the output voltage swing against C_{boot1} for different C_{boot2} .

Fig. 6. The propagation delay and power dissipation against C_{boot2} for different C_{boot1} .

TABLE I
THE RELATIONSHIP BETWEEN POWER DISSIPATION, PROPAGATION DELAY AND C_{boot1} , FOR $C_{boot2} = 150$ fF

C_{boot1} (fF)	Power Dissipation (μW)	Delay (ps)
150	139.20	525.3
300	141.00	518.45
500	143.9	515.75

that C_{boot2} starts to charge up once the output voltage drops to 0 V, then the allowable charging time is

$$t_{c, \max} = \frac{1}{2} T - t_f. \quad (6)$$

The charging current that flows into C_{boot2} is

$$I = C_{boot2} \frac{dV_a}{dt}. \quad (7)$$

Based on (7), the entire operation of charging the node a from 0 to $0.9 V_{DD}$ can be divided into two regions.

Fig. 7. Various two-input NAND gates (a) CMOS, (b) BFBiNMOS, (c) BSBiNMOS and (d) TC-BiNMOS circuits.

Region 1: $0 \leq V_a \leq (1 - K)(V_{DD} - |V_{T(MP1)}|)$: MP1 operates in saturation mode, since it is a short-channel device, its current can be expressed as [10], [11]

$$I_{D1} = K v_{sat} C_{OX} W (V_{DD} - |V_{T(MP1)}|) \quad (8)$$

where

K short-channel effect factor;

v_{sat} carrier saturation velocity;

C_{OX} gate oxide capacitance;

W channel width of MP1.

Substituting (8) into (7), the charging time is found to be

$$t_{c1} = \frac{(1 - K) C_{boot2}}{K v_{sat} C_{OX} W}. \quad (9)$$

Region 2: $(1 - K)(V_{DD} - |V_{T(MP1)}|) < V_a \leq 0.9V_{DD}$: MP1 now operates in the linear region, and its drain current is given by [10], [11]

$$I_{D2} = \frac{\mu_{eff} C_{OX} W}{L_{eff}} \times \frac{1}{1 + \frac{V_{DD} - V_a}{E_C L_{eff}}} \cdot \left(\frac{1}{2} V_{DD} - |V_{T(MP1)}| + \frac{1}{2} V_a \right) (V_{DD} - V_a) \quad (10)$$

where

μ_{eff} effective hole mobility;

L_{eff} effective channel length;

E_C critical electric field.

By solving (7) and (10), the charging time in this region is obtained

$$t_{c2} = \frac{C_{boot2}}{\mu_{eff} C_{OX} E_C W} \times \frac{1}{V_{DD} - |V_{T(MP1)}|} \cdot \left[E_C L_{eff} \ln \frac{V_{DD}}{K V_{DD} + (1 - K) |V_{T(MP1)}|} + (2V_{DD} + E_C L_{eff} - 2 |V_{T(MP1)}|) \cdot \ln \frac{19V_{DD} - 20 |V_{T(MP1)}|}{(20 - 10K)V_{DD} - (30 - 10K) |V_{T(MP1)}|} \right]. \quad (11)$$

So, the total pre-charge time is

$$t_c = \frac{C_{boot2}}{C_{OX} W} \left\{ \frac{1 - K}{K v_{sat}} + \frac{1}{\mu_{eff} E_C} \times \frac{1}{V_{DD} - |V_{T(MP1)}|} \cdot \left[E_C L_{eff} \ln \frac{V_{DD}}{K V_{DD} + (1 - K) |V_{T(MP1)}|} + (2V_{DD} + E_C L_{eff} - 2 |V_{T(MP1)}|) \cdot \ln \frac{19V_{DD} - 20 |V_{T(MP1)}|}{(20 - 10K)V_{DD} - (30 - 10K) |V_{T(MP1)}|} \right] \right\}. \quad (12)$$

Fig. 8. The effect of the load capacitance on (a) propagation delay and (b) power dissipation for various two-input NAND gates.

From (12), it is obvious that the pre-charge time is proportional to C_{boot2} , and inversely proportional to W . In order to fully charge-up node a to V_{DD} within the allowable charging time, C_{boot2} should have a small capacitance, and MP1 should have a large W . However, the area of and the power dissipated by MP1 are proportional to W . Similarly, a small C_{boot2} would have charge leaking problem during the switching period, and as a result the circuit might not achieve a full swing.

B. Pre-Charge Voltage at Node b

The pre-charge voltage at node b affects the circuit performance especially the power consumption and speed. The dependence of the pre-charge voltage on the supply voltage and the threshold voltage of MN1 is

$$V_{pre} = V_{DD} - V_{T(MN1)}. \quad (13)$$

The static power consumed by the circuit is related to the static current flowing through $Q1$ during the pull-down cycle. The initial value of this current can be expressed as

$$I_{ST} = I_S \left(\exp \left[\frac{V_{pre}}{V_{TH}} \right] - 1 \right) \quad (14)$$

where

- I_S saturation current;
- $V_{T(MN1)}$ threshold voltage of MN1;
- V_{TH} thermal voltage.

From (14), it is clear that high values of V_{pre} are undesirable, as they cause excessive static power dissipation. However, if this pre-charge voltage is too low, the output voltage might take

Fig. 9. The dependence of the power dissipation and propagation delay on the supply voltage for different two-input NAND gates.

TABLE II
DEVICE COUNT AND AREA RATIO OF VARIOUS TWO-INPUT NAND GATES

	Device Count			Area Ratio (w.r.t. CMOS)
	MOS	Capacitor(MOS)	BJT	
CMOS	4	-	-	1
BSBiNMOS	13	1	1	2.3
BFBiNMOS	15	1	1	2.6
TC-BiNMOS	10	2	1	2.2

Fig. 10. The photomicrograph of the new 75-stage ring oscillator.

a long time (or even fail) to achieve a full swing. Hence, an optimum pre-charge voltage is needed. Fig. 4 shows the effect of the pre-charge voltage at node b on the power consumption and propagation delay. The power consumption rises sharply when the pre-charge voltage exceeds 0.8 V due to the excessive static current flowing through $Q1$. This is a static power dominant situation that is undesired. Below the turn-on voltage of $Q1$ [i.e., $V_{BE(on)} < 0.7$ V], the static power of the circuit is negligibly small as compared to its dynamic power dissipation. Hence, the optimum pre-charge voltage should be kept about 0.7 V and the supply voltage of the new circuit should not exceed $V_{T(MN1)} + V_{BE(on)}$.

C. Sizes of C_{boot1} and C_{boot2}

Since there are two capacitors in the circuit, their sizes become an important factor to determine the overall chip area, the average power consumption, and also the delay time. It has been shown that by implementing these capacitors using the MOS gate oxide capacitance, the area can be reduced significantly

Fig. 11. The output voltage waveform of the new 75-stage ring oscillator.

[12]. Fig. 5 shows the achievable output voltage swing for different combinations of C_{boot1} and C_{boot2} . The output voltage could not reach full swing when both capacitors are less than 100 fF. The effect of C_{boot2} on the power dissipation and propagation delay is shown in Fig. 6. The speed and power consumption of the circuit increase with the size of C_{boot2} . Based on the results shown in Figs. 5 and 6, a 150-fF capacitance was chosen for C_{boot2} to ensure a full output voltage swing and the best compromise in speed, power and chip area of the new circuit. With C_{boot2} fixed at 150 fF, C_{boot1} is varied according to Table I. The results show that both the propagation delay and power dissipation are weak functions of C_{boot1} . Therefore, from Figs. 5, 6, and Table I, the optimum value for C_{boot1} is 150 fF.

D. Scaling of Supply Voltage/Technology

Any scaling down of the device feature size to improve the performance of the circuit must be accompanied by appropriate scaling down of the supply voltage due to reliability issues and power consumption limitations. Indeed, our circuit simulations have indicated that the amount of charge stored in the bootstrapping capacitor decreases with the supply voltage. Hence, the threshold voltage of the MOS devices should switch from 0.85 to 0.55 V, and the gate oxide thickness should reduce from 120 to 90 Å for the 1.5 V/0.8 μm and 1.2 V/0.5 μm technologies, respectively, to avoid any circuit performance degradation that may arise due to a reduced stored charge in the bootstrapping capacitors.

IV. PERFORMANCE EVALUATION

The performances of all the circuits, namely, BSBiNMOS [6], BFBiNMOS [7], CMOS and TC-BiNMOS were verified by HSPICE simulation based on a 0.5- μm BiCMOS technology. A two-input NAND configuration was chosen to evaluate and

compare the performance of the circuit as shown in Fig. 7. All circuits have the same input capacitance of 80 fF per input pin. The simulation was carried out using a 50 MHz square wave input with rise and fall time of 0.2 ns. The reported propagation delay time is that of the third gate in a chain of four NAND gates.

A. Propagation Delay

Fig. 8(a) shows the effect of the load capacitance on the propagation delay. The TC-BiNMOS outperforms all other circuits and its crossover capacitance is as low as 0.15 pF. At a load capacitance of 1 pF, its propagation delay reduction is 40% over the CMOS circuit. Its delay to load sensitivity is only 820 ps/pF, while the CMOS is 1520 ps/pF. As for the BFBiNMOS and BSBiNMOS, both circuits are slower than the proposed circuit, the former's crossover capacitance is 0.2 pF while the later is 0.3 pF.

B. Power Consumption

The power dissipation against the load capacitance is shown in Fig. 8(b). The BFBiNMOS consumes more power under all load conditions. The BSBiNMOS and the TC-BiNMOS dissipate almost equal amount of power, and only slightly more power than their CMOS counterpart. Fig. 9 illustrates the effect of scaling the supply voltage on the propagation delay and power dissipation. The high speed and relatively low power consumption characteristics of the proposed circuit outdo the suitability of the other circuits for single battery operation.

C. Area

Table II lists the device counts and area ratios with respect to the CMOS, for various two-input NAND configurations. The TC-BiNMOS requires a smaller number of devices and occupies the smallest area amongst the various BiNMOS families.

D. Experimental Results

A 75-stage ring oscillator with the new circuit was designed and fabricated using the AMS 0.8 μm double poly-silicon double metal BiCMOS process. Its photomicrograph and output voltage waveform are shown in Figs. 10 and 11, respectively. The ring oscillator oscillates at a frequency of 5.0 MHz for a supply voltage of 1.5 V and a load capacitance of 1 pF. This is equivalent to a gate delay/stage of 1.32 ns.

V. CONCLUSION

A new BiNMOS logic gate (TC-BiNMOS) which uses two bootstrapping capacitors and a standard noncomplementary BiCMOS process is presented. The circuit is specially designed for 1.2–1.5 V supply voltage. Some important design issues such as the pre-charge voltage and the size of bootstrapping capacitors, which affect the circuit performance, were discussed. HSPICE simulations have shown that the proposed circuit offers 40% delay reduction and about 50% delay to load capacitance sensitivity reduction over the CMOS circuit. The new circuit occupies the smallest area amongst the various BiNMOS families and it consumes only slightly more power than its CMOS counterpart. The crossover capacitance of the new circuit is as low as 0.15 pF and a 75-stage ring oscillator was fabricated using a 0.8- μm BiCMOS process. The measured gate/stage is 1.32 ns at a supply voltage of 1.5 V and a load capacitance of 1 pF.

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