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Impacts of Bends and Ground Return Vias On Interconnects For High Speed GHz Designs

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***Abstract*—In the past only critical clock circuits are running at high speed but this is no longer true in today high-speed digital design world. Most of the digital traces on board are running at speed in excess of 200 MHz and drivers output with rise time less than 1 ns. Due to constraints of board size and highly complex designs, trace bends and inter-layer transitions through vias are unavoidable. This paper carries out a comprehensive study on the impacts of bends and ground return vias optimisation on signal integrity performance using a full-wave electromagnetic simulator. (CST Microwave Studio). This study will provide high-speed digital designers an in-depth assessment of these effects in high-speed GHz applications so that some design guides to avoid these effects can be established.**

I. INTRODUCTION

PCB traces are used as interconnects between devices and circuits. In most previous digital designs with clock frequency below 40 MHz, the significant of interconnects are small compared to the devices driving capabilities. However, in the last decade, there was a tremendous surge in the needs for higher speed interface and faster operating devices. Today operating clock frequency has exceeded 1 GHz with rise time reduced to sub nano second and typical bus interfaces are in excess of 200 MHz. As design complexity increases coupled with miniaturisation needs, multi-layer PCB are rapidly adopted to meet the compact and dense routing challenge. The effects of interconnects not only affects the critical clock signals but also the rest of the digital buses and interfaces which becomes the limiting factor in the design and proper trace routing has to be consider seriously.

II. PERFORMANCE INDICATORS FOR INTERCONNECT ANALYSIS

In this paper, the effects of commonly used trace bends, ground return via and its optimisation for digital application are studied. Though conventional 4 ground vias requirement provides optimum signal integrity, the number of additional ground vias for dense board can poise some practical limitation. A simpler one ground return via is studied for practicality purposes. With the via diameter fixed as 0.2 mm optimum choice for typical high speed digital design and PCB thickness simulated at 1.5 mm which is commonly used.

To study these effects of trace structure on high speed interconnects, the scattering parameters S11 (reflection loss), S21 (insertion loss) are chosen to assess the trace performance. S11 indicates the amount of reflected signal due to impedance mismatch introduced by the discontinuity of structure and S21 shows the amount of signal attenuation when the signal going through the trace structure. Besides the frequency domain scattering parameters, the TDR results are simulated with 10-90% rise time of 43.8 ps and 1 V signal magnitude.

A. *Effect of Trace Bend on Signal Performance*

In high speed designs, impedance control of board, buses and peripheral interfaces are critical. Impedance change caused by trace bends will result in signal reflections and degrades the signal performance. However such bends are inevitable in PCB routing due to physical board limitation.

A typical bend or corner is often seen as a capacitive discontinuity. This section provides a thorough simulation, analysis cum measurement to fully characterise the impact of various typical bend structures on signal integrity performance for gigahertz operation. Simulations are carried out on 4 commonly used techniques to implement trace bend in PCB design. They are 90° bend, 45° bend with chamfer, double round bend and single round bend, as illustrated in Fig. 1. The performance characteristics of these bend test structures are simulated, compared and analysed.

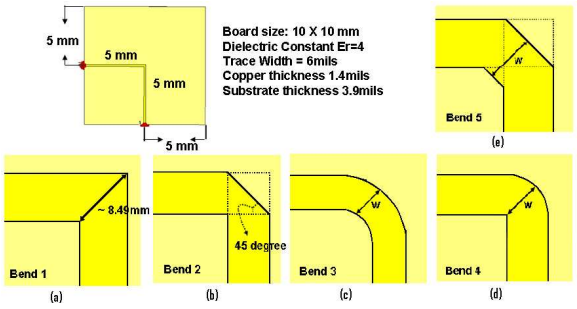


Fig. 1 Trace overall test structure Configuration (a) Right angle bend, (b)45° chamfer, (c)double rounded bend (d)Single rounded bend and (e)45° bend

Fig.2 shows the simulated TDR responses for the 5 different bend structures. As expected, the 90 degree bend provides the worst impedance discontinuity and should be avoided. The double rounded bend gives the best performance. The 45 degree bend is a much better choice offering performance closer to that of the double round bend. The 45 degree bend offers up to 70% reduction in impedance discontinuities over the 90degree bent.

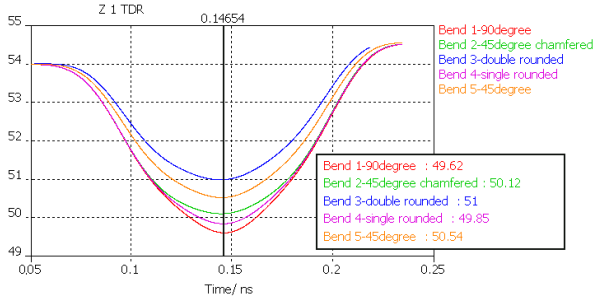


Fig. 2 Effects on TDR response of bend structures

Fig 3 and 4 illustrate the S11 and S21 respectively for each of the 4 bend structures. For very high speed digital application with tighter tolerance, the following results do show a clear different between the various structures. While the double round bend is best but not very practical in digital routing. The simple 45degree bent structure is still the optimum choice in terms of S21 and S11 which provides a close to 20% improvement over the 90degree bent.

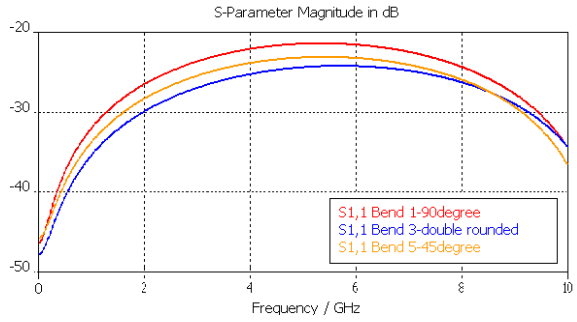


Fig. 3 S11 Reflection loss response for various bent structures

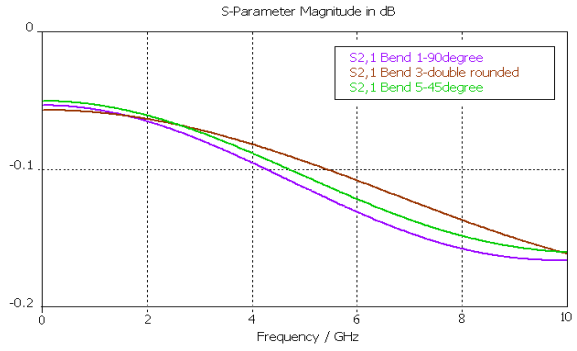


Fig. 4 S21 Insertion loss response for various bend structures

B. *Effect of Ground vias on Signal Performance*

When a signal propagates down the interconnect from the source and a reference, it has to return back to the source via the same reference. While emphasis in the past has been place significantly on the forward trace routing, the return through the plane is often neglected. In many existing digital designs, signal path are layout from source to destination along the way, vias are used randomly to allow for physical trace layout possible in multi-layer PCB structures. Not many designs consider the return ground vias in which its effect may not be significant in the past. However in gigahertz high speed digital design, this becomes crucial and cannot be ignored. Return path has to be designed into the layout with as much consideration as the signal path.

As it has been shown that at high frequency operation, the return current follows closely to the signal path with least loop impedance. Hence for PCB interconnects, the path of least impedance is in fact directly next to the signal path. For two conductor transmission line, microstrip and strip line where signal is driven with a common reference between them, the return path is easy to determine.

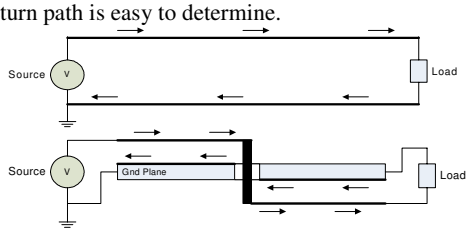


Fig. 5 Two conductors & microstrip interconnects over common return plane

What if the signal transit through a multi-layer PCB switching over different grounds? The reference plane is no longer common and this gives rise to serious discontinuities problem in the return path and would leads to degradation of signal performance. The return will go through the nearest surrounding ground via to move from gnd2 to gnd1.

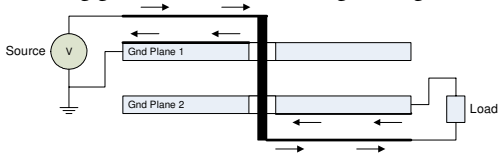


Fig. 6 Interconnects over different return plane

It has been shown[2] and in our simulations that with a 4 ground vias structure in fig7, by varying the distance of the ground vias to the signal via and ground opening in the inner layers, we can control the capacitance and provide optimum impedance control with excellent S11 and S21 performance.

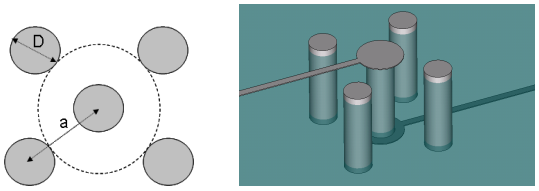


Fig. 7 Four ground via Configuration and Design Structure

However, typical digital design boards can easily have up to 2000 signal vias. If the 4 ground vias approach is adopted, this could increase the number of vias by 4 times to 10000. This can cause tremendously routing constraint and often not practical at all in a limited physical PCB space in today compact digital design. Hence a more practical and suitable technique is to use the single ground via return. This is a typical adopted technique but the author attempts to shed more lights on its effects on SI performance in high-speed application through the simulation and measurement.

The effects of the presence of even one single ground return via can significantly affects the behaviour of the return current flow as shown in fig.8 below.

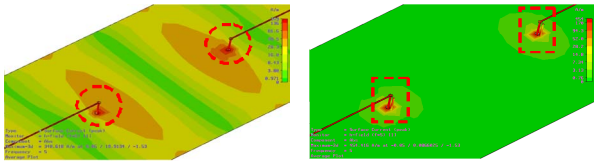
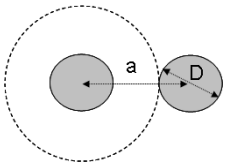


Fig. 8 One Gnd return via Design

Using the design parameter as in Fig.9 and a typical high-speed signal via of 0.2mm, it is shown that the impedance can be optimised for minimum discontinuity and good S11 and S21 performance.



Design parameters

Dielectric constant	: 4
Interconnect	: Cu
Gnd and trace thickness	: 0.015mm
Substrate 1, 2 & 3 height	: 0.2/3/0.2mm
Via radius D	: 0.2mm
Signal-Gndvia distance a	: 0.6-3mm

Fig. 9 One Gnd return via Design

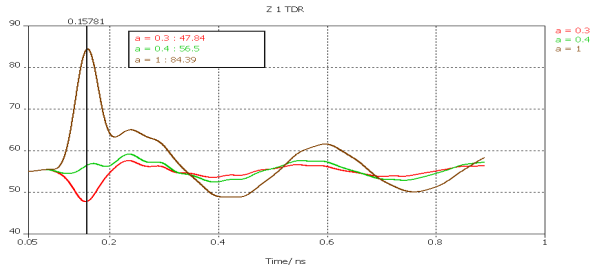


Fig. 10 TDR Response of One Gnd return via design

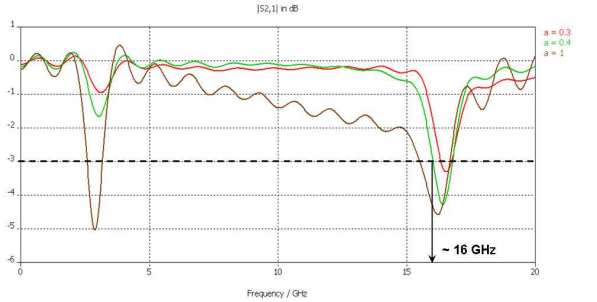


Fig. 11 S21 Response of One Gnd return via design

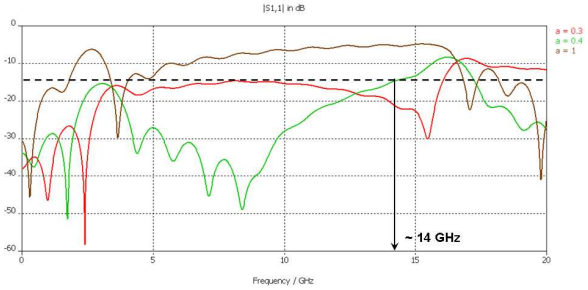


Fig. 12 S11 Response of One Gnd return via design

Fig10-12 shows the simulated TDR, S11 and S21 response of the single ground via configuration. By varying the distance from the signal via, it is show that the optimum distance of ~0.4mm separation between the signal and ground via will achieve the best performance. At -20dB cut-off, S11 is capable of operating up to 7.5GHz while S21 is less than -2dB.

C. Case Study on Trace structure on SI Performance

In today gigabits transfer rate of common digital designs, every slightest impedance variation will cause degradation to the signal integrity and overall performance. In most typical digital board, direct continuous routing from one point to another is a luxury and often not possible. Minor bends are needed to avoid obstructions. The use of other layers to complete the routing is also in-avertable. Hence the use of via is needed and the ground return path switches reference plane bound to occurs.

To illustrate the effects of traces bent and ground return vias present in high speed application, a microstrip is routed with 2 closely space bends followed by two large bends with and without layer transition between layer 1 and 6 using vias. The common design parameters: Frequency range: 0-20 GHz, FR4 permittivity $\varepsilon_{r} = 4$, trace width = 6mil, trace thickness of 1/5oz and each trace segments ~1" & 5mm for small bend.

Ref: Both bents using 90degrees bent structure
Case1: Both bents using double rounded structure
Case2: Both bents using 45degree bend structure
Case3: One 45° bent with layer transition w/o ground via
Case4: One 45° bent with layer transition with 1 ground via

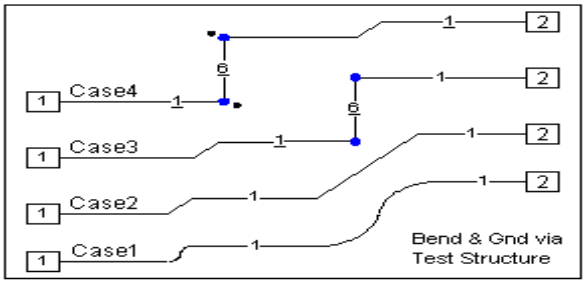


Fig. 13 S21 Response of One Gnd return via design

As results shows that both case1 and case2 have similar and equally good response. Fig14 shows the comparison between case2 and the reference straight and 90degree which clearly

indicates that though both have similar TDR response (<1ohm) when compare to using right angle bend, but 90degree bend S21 response is worst off in the high frequency region.

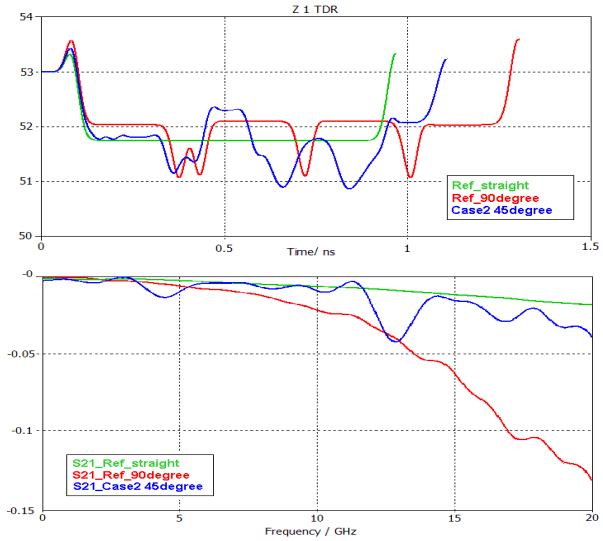


Fig. 14 Simulated TDR and S21 response for Case2 and Ref comparison

When trace structure transit between layers without appropriate ground return via, the response is far worst as shown in the serious ringing in the TDR up to 30% and the degradation in the high frequency S parameter response with a bandwidth of less than 3GHz shown in Fig 15.

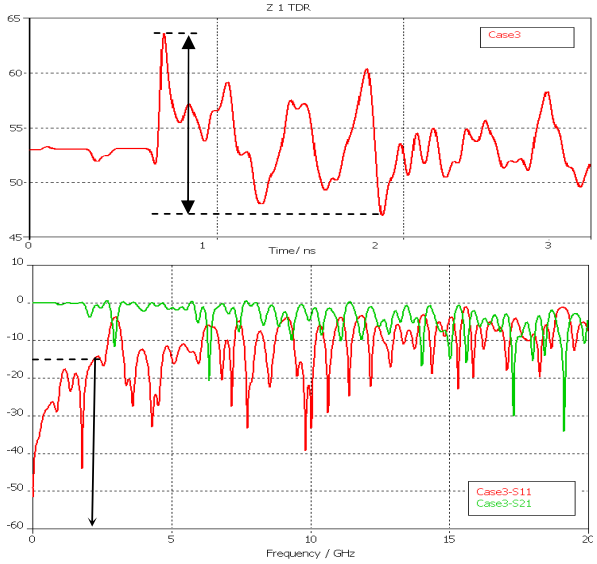


Fig. 15 Simulated Case3 TDR, S11 and S21 response w/o Gnd return via

For proper impedance control when signal transit between layers, suitable ground return via has to be design into the layout to ensure smooth transition and optimised signal performance as shown in Fig 16 whose TDR is within 5% and S21 response in excess of 10GHz.

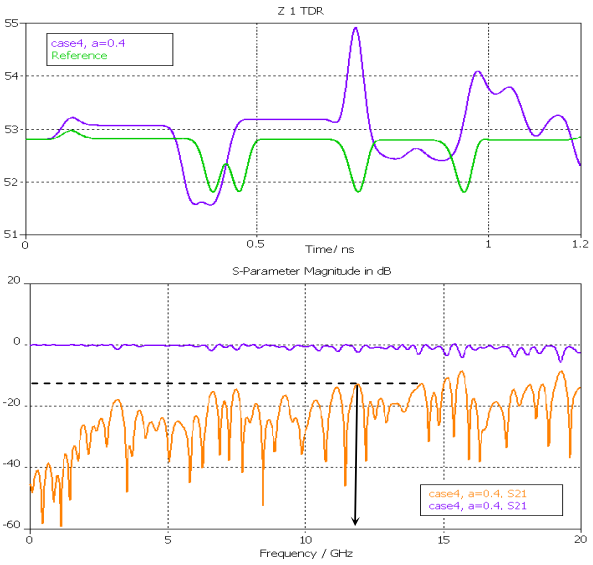


Fig. 16 Simulated TDR and S21 response for Case4 and Ref comparison

The simulated results obtained clearly shows the important of even the basic trace layout such as bends and layer transition have on the SI effects and with a single optimised return ground via will helps significantly in the improvement of the signal performance. The authors are currently working on the actual prototypes measurements so as to correlate to the simulated results. Details may be published in future works.

III. Conclusions

Both the two crucial trace structure bents and ground vias, their effects on signal performance in high speed digital application are evaluated. To ensure optimum design margin, though effect not very significant, the simple and yet efficient 45 degree bent should be used when possible instead of 90 degree bent. As for signal return path which is critical to design, at least one single ground return via with an optimized distance of 0.35mm should be utilized for high speed application to avoided signal aberration due to impedance discontinuity when signal transit between grounds layers in the multi-layer PCB. A practical case study on the importance of trace bend and ground return via was presented.

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