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A Subthreshold Low-Noise Amplifier Optimized for Ultra-Low-Power Applications in the ISM Band

Aaron V. Do, *Member, IEEE*, Chirn Chye Boon, Manh Anh Do, *Senior Member, IEEE*,
Kiat Seng Yeo, *Member, IEEE*, and Alper Cabuk, *Member, IEEE*

Abstract—The IEEE 802.15.4 standard relaxes the requirements on the receiver front-end making subthreshold operation a viable solution. The specification is discussed and guidelines are presented for a small area ultra-low-power design. A subthreshold biased low-noise amplifier (LNA) has been designed and fabricated for the 2.4-GHz IEEE 802.15.4 standard using a standard low-cost 0.18-μm RF CMOS process. The single-stage LNA saves on chip area by using only one inductor. The measured gain is more than 20 dB with an S_{11} of -19 dB while using 630 μA of dc current. The measured noise figure is 5.2 dB.

Index Terms—Front-end, low-noise amplifier (LNA), low power, subthreshold.

I. INTRODUCTION

THE IEEE 802.15.4 standard was introduced to meet the growing demand for low-cost low-power short-range wireless communications devices. The specifications relax the requirements on the RF front-end and allow for less power-hungry designs [1]. The IEEE 802.15.4 standard covers three frequency bands, i.e., 868 MHz, 915 MHz, and 2.4 GHz. This study will use the 2.4-GHz industrial, scientific, and medical (ISM) band.

This paper presents the design of a low-noise amplifier (LNA) for the IEEE 802.15.4 standard, which fully exploits the relaxed front-end requirements to minimize the power consumption and chip area. To that end, the input transistor of the LNA is biased in the subthreshold region, which offers superior gain per current consumption. We will justify the use of subthreshold biasing through MOSFET characteristic equations and simulations. The MOS transistor's noise characteristics are not adequately modeled in the weak-inversion/subthreshold region at high frequencies, therefore, the analysis of noise performance will not be included [2]. We will also avoid the use of off-chip components. Finally, we remove two typically used on-chip inductors, which require a large chip area while providing only marginal benefits. This is in line with the need for a low-cost RF front-end.

The LNA was designed using the Chartered Semiconductor Manufacturing (CSM) 0.18-μm RF CMOS Process Design Kit (PDK). Section II will cover the LNA specifications based on IEEE 802.15.4 standard specifications. Section III will present the LNA design. Section IV will present the simulated and measured results. This paper then concludes in Section V.

TABLE I
IEEE 802.15.4 RECEIVER REQUIREMENTS

Receiver's Specification	Requirement
Noise Figure	20.5 dB
IIP$_3$	-32 dBm
P$_{1dB}$	-20 dBm

II. IEEE 802.15.4 SPECIFICATIONS

A. Overall System

Table I shows the receiver specifications important to the LNA design [3]. The requirements can be calculated from the IEEE 802.15.4 standard's physical layer (PHY) specifications [1], [4]. Based on the overall requirements of the receiver and past experience in IF block design, we can formulate the requirements for the LNA.

The LNA was designed for a system assuming that a low-IF or zero-IF architecture is used. Such a system can achieve high integration by eliminating the need for off-chip image-reject filtering after the LNA. Therefore, the LNA will be followed directly by an image reject mixer as is used in the Hartley or Weaver receivers [5].

B. Noise Figure (NF)

The required NF assuming a 5-dB loss preceding the LNA is 20.5 dB [1]. This 5-dB margin will account for issues such as board losses and band-select filter insertion losses. The NF can be expressed as a magnitude to yield the noise factor F, which is defined as the ratio of the total output noise to the output noise arising due to the source resistance only. By convention, F is defined at 290 K as follows:

$$F = \frac{\mathrm{Source}N_{\mathrm{in}} + \mathrm{DUT}N_{\mathrm{in}}}{\mathrm{Source}N_{\mathrm{in}}} \tag{1}$$

where $\mathrm{Source}N_{\mathrm{in}}$ is the input noise due to the source, and $\mathrm{DUT}N_{\mathrm{in}}$ is the input-referred noise (IRN) due to the device-under-test (DUT). We define the input terminal as the node connecting the DUT to the source resistance. We can derive the IRN of the IF stages (taken at the output of the down-conversion mixer) IFN_{Mixout} as

$$IFN_{\mathrm{Mixout}} = \mathrm{Source}N_{\mathrm{in}} \cdot G_{\mathrm{LNAMix}}^2 \cdot (F_{\mathrm{system}} - F_{\mathrm{LNAMix}}) \tag{2}$$

where G_{LNAMix} is the voltage gain of the LNA and mixer, F_{system} is the required system noise factor, and F_{LNAMix} is

the noise factor of the LNA and mixer. IFN_{Mixout} is the most important factor in determining the power consumption of the analog IF blocks such as the channel select filter (CSF) and the variable gain amplifier (VGA). This is because input referred noise varies inversely with transconductance [7]. In general we can improve the transconductance by increasing the power consumption. While research has typically focused on minimizing the LNA power consumption and NF, the analog section still takes up significant power consumption to minimize its noise contribution [8], [9]. The complex baseband filter designed in [9] requires 4.7 mA to maintain its IRN of 30 nV/$\sqrt{\text{Hz}}$. According to (2), in terms of overall receiver power consumption, it is more beneficial to optimize LNA gain than the LNA NF.

From (2), if $F_{\text{system}} \gg F_{\text{LNAMix}}$, we can then neglect the contribution of F_{LNAMix}. For this purpose, let us assume that F_{LNAMix} becomes insignificant if it is less than 10% of F_{system}. Converting 20.5 dB to magnitude, we find F_{system} to be 112.2. Therefore, we can tolerate an F_{LNAMix} of 11.2 or 10.5 dB, which is not difficult to achieve even with low power consumption. On the other hand, IFN_{Mixout} is directly proportional to G_{LNAMix}^2. Therefore, for the IEEE 802.15.4 standard, high LNA gain is much more important than a low NF.

C. Linearity

When strong out-of-channel interference passes through a nonlinear system, the power of the interferer can be frequency translated into the desired channel. It can then be treated as noise and will degrade the system's throughput. The linearity of the LNA is usually measured by its input-referred third-order intercept point (IIP_3). The IIP_3 trades directly with the LNA gain, but in a low-power design, gain is scarce. Therefore, we must maximize the gain to dc current ratio. This is elaborated upon in Section III-D.

In fact, the LNA IIP_3 has little impact on the overall IIP_3 of the system, as is obvious from the equations derived in [9]. This result is intuitive because, as the signal progresses to the later stages of the receiver, it passes through more amplifying blocks and its amplitude becomes larger. For example, if the mixer has an IIP_3 of 0 dBm and is preceded by an LNA gain of 20 dB, the overall IIP_3 of the combined LNA and mixer will be lower than -20 dBm. Since the LNA is the first amplification block in the receiver chain, it is not difficult to meet IIP_3 requirements. For our system, the 1-dB compression $\left(P_{1\,\text{dB}} \right)$ point imposes a much stricter linearity requirement on the LNA than the IIP_3. Even so, the required $P_{1\,\text{dB}}$ of the LNA is still achievable.

III. LNA Design

A. Main Changes

Fig. 1(a) shows the standard inductively degenerated LNA [5] and Fig. 1(b) shows the proposed LNA. The three main changes are the removal of L_s, replacing L_d with a resistor, and biasing M_1 in the weak inversion region. M_2 is biased in the saturation region to take advantage of the low parasitic output capacitance associated with the smaller device size. We will justify each of these changes. Using the aforementioned design methods, the LNA meets the IEEE 802.15.4 standard's requirements.
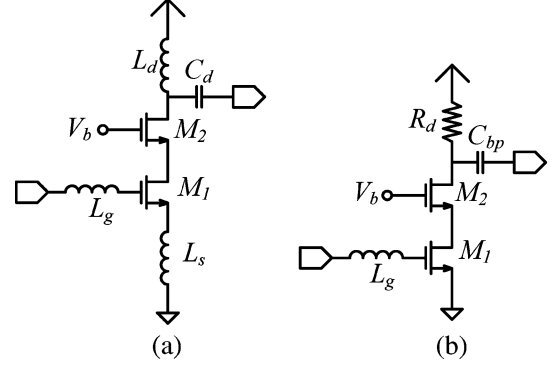

Fig. 1. (a) Typical inductively degenerated LNA. (b) Proposed LNA. In the proposed LNA, we have removed L_s and replaced L_d with R_d. M_1 is biased in the subthreshold region.

B. Input Matching

In Fig. 1(a), L_s adds a real part to the input impedance, while $(L_g + L_s)$ resonates with C_{gs} (gate–source capacitance) of M_1 to provide impedance matching at the operating frequency. Ideally, L_s adds no noise to the system, making this input matching method highly attractive. If the impedance at resonance is R_{in}, then the input current I_{in} is

$$I_{\text{in}} = \frac{V_{\text{in}}}{R_{\text{in}}} \tag{3}$$

where V_{in} is the input voltage. Thus, the voltage across C_{gs} is

$$V_{C_{\text{gs}}} = \frac{I_{\text{in}}}{\omega_0 C_{\text{gs}}} = \frac{V_{\text{in}}}{R_{\text{in}} \omega_0 C_{\text{gs}}} \tag{4}$$

and the transconductance from the input to the drain of M_1 is

$$G_m = \frac{g_m}{R_{\text{in}} \omega_0 C_{\text{gs}}} = g_m Q_{\text{in}}. \tag{5}$$

For the proposed LNA, the source is matched to the parasitic series resistance of L_g. If this resistance is insufficient, an extra resistor can be added in series with L_g. The justification for this is that the IEEE 802.15.4 standard does not require a low LNA NF, as demonstrated in Section II-B. Furthermore, in typical designs, the low-Q inductor, i.e., L_g, is often so large that its parasitic resistance not only significantly affects the input matching, but its noise contribution masks the noise contribution of M_1 even when using inductive degeneration.

In the proposed topology, following the same reasoning, it is easy to see that G_m is calculated by (5). In other words, the 50-Ω series resistor introduces no additional loss into the system. The proposed input matching network saves one inductor in the LNA design. In the CSM 0.18-μm RF CMOS process, a single-turn top metal inductor with a 100-μm-core diameter requires a total area of approximately $\pi(110\,\mu\text{m})^2$ including a peripheral area, which must be left unoccupied to prevent magnetic coupling into nearby metal lines. Each additional turn adds 12 μm to the radius.

C. LNA Load

In traditional board level design, the LNA output is expected to match to a 50-Ω load. This practice has continued in several integrated circuit designs through the use of an *LC* matching

network like the one used in Fig. 1(a). Using this network, we can approximate the voltage gain G_{LNA} by (see Appendix)

$$G_{\text{LNA}} = \frac{1}{2} G_m \sqrt{R_{\text{out}} R_{\text{load}}} \qquad (6)$$

where R_{out} is the parallel parasitic resistance of L_d combined with the output resistance of M_2. We have assumed that the capacitor C_d has sufficiently high Q, and that its parasitic resistance can be neglected. If R_{load} can be made equal to R_{out}, the voltage gain will be maximized, and the matching network is unnecessary. The inductor L_d still performs the useful function of resonating with the parasitic load capacitance of M_2 and the down-conversion mixer. In order to make R_{load} equal or greater than R_{out}, we can minimize the device sizes of the passive mixer. This is in line with the low-power theme since the reduced loading on the local oscillator (LO) signal will further reduce the required power consumption.

In the proposed design, we have replaced L_d with a load resistor R_d. This is possible because the dc current through the LNA is only 630 μA. For a 1-kΩ resistor, this results in a voltage drop of 0.63 V, which provides for sufficient voltage swing at the output. Use of a load resistor significantly reduces the chip area needed by a load inductor. Furthermore, the load has no resonant frequency, making the gain broadband and less sensitive to process variation. This increases the chance of a first-pass circuit design success. Unfortunately, these benefits come at the cost of reduced gain due to signal loss through the parasitic load capacitance, and a 3-dB loss in the maximum voltage swing.

D. Weak Inversion Biasing

From the discussion in Section II, we can relax the LNA noise requirements and, therefore, lower power consumption. We must now find a way to meet the high voltage gain requirements with reduced power consumption.

Weak inversion biasing is usually restricted to low-frequency circuit designs because of the poor g_m associated with the low current drive. It is well known that lowering the gate overdrive improves the g_m to dc current ratio, but to meet the required g_m, large input transistors are usually needed, which have correspondingly large gate capacitances. It is clear from (5) that, to maximize G_m, we need to minimize the gate capacitance. Using the standard saturation region dc current equations for long channel devices, we can approximate

$$g_m \approx \sqrt{K \frac{W}{L} I_{\text{DS}}} \qquad (7)$$

$$\frac{g_m}{I_{\text{DS}}} \approx \frac{2}{(V_{\text{GS}} - V_T)} \qquad (8)$$

where K is a technology dependant constant, and V_T is the threshold voltage. To ensure saturation region operation, we should set $(V_{\text{GS}} - V_T)$ to at least nV_t [10], where V_t is the thermal voltage ($V_t = kT/q \approx 26$ mV), and n is the subthreshold slope, which, for the CSM 0.18-μm RF CMOS
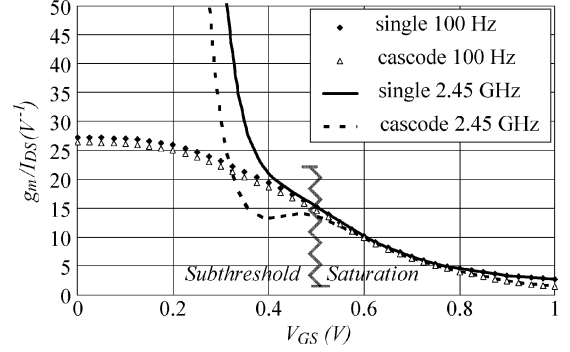

Fig. 2. g_m/I_{DS} of a MOS transistor and cascode structure at 100 Hz and 2.45 GHz.

process, is roughly equal to 1.5. The corresponding subthreshold equations can be derived based on the BSIM3v3 model [11]

$$I_{\text{DS}} = I_{SO} \cdot \left(1 - \exp\left(-\frac{V_{\text{DS}}}{V_t}\right)\right) \exp\left(\frac{V_{\text{GS}} - V_T - V_{\text{off}}}{nV_t}\right). \qquad (9)$$

I_{SO} is proportional to W/L, and V_{off} is an offset voltage. If V_{DS} is more than V_t, then the first term in brackets is close to unity and we can safely ignore the contribution of V_{DS}. Therefore,

$$g_m \approx \frac{I_{\text{DS}}}{nV_t} \qquad (10)$$

$$\frac{g_m}{I_{\text{DS}}} \approx \frac{1}{nV_t}. \qquad (11)$$

Equations (8) and (11) illustrate that g_m/I_{DS} improves until the device enters subthreshold operation then reaches its maximum value, while (7) and (10) show that g_m increases with increasing I_{DS}. We can also see that (8) and (11) disagree at the border between saturation and subthreshold operation ($V_{\text{GS}} = V_T + nV_t \approx 0.519$ V). Equation (8) shows g_m/I_{DS} is roughly equal to 51.3 V^{-1}, whereas (11) shows g_m/I_{DS} is roughly equal to 25.6 V^{-1}. In practice, the gradient of (8) will gradually level off and g_m/I_{DS} will tend to (11).

While these trends hold at low frequencies, they are somewhat distorted at higher frequencies due to parasitic effects. At 2.45 GHz, the amount of leakage current through the gate–drain capacitance of M_1 can exceed the channel current if the transistor is biased in the deep subthreshold region. Fig. 2 shows simulations of g_m/I_{DS} at 100 Hz and 2.45 GHz, and Fig. 3 shows the corresponding phase difference between the input voltage and output current. The simulations are run for both single device and cascode structures. From Fig. 2, g_m/I_{DS} reaches a maximum value of around 26 V^{-1} at low frequency, which agrees with (11). With improving technology, the same device dc current, and hence, subthreshold g_m, can be yielded with a smaller gatewidth. Since C_{gd} is proportional to channel width, improving technology can make subthreshold biasing a more attractive solution. As C_{gd} reduces, the ratio of leakage current to channel current will correspondingly reduce.
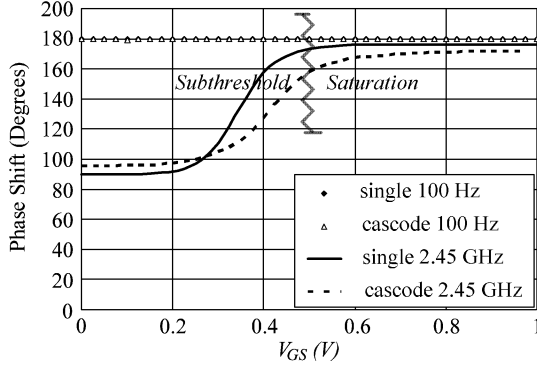
Fig. 3. Output current phase shift of a MOS transistor and cascode structure at 100 Hz and 2.45 GHz.
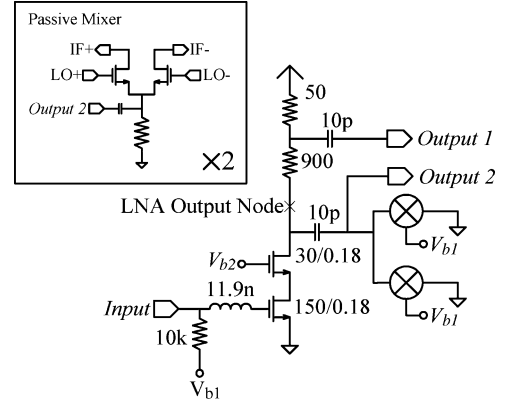

Fig. 4. Fabricated LNA including a dummy quadrature mixer to account for the load impedance. The inset shows a passive mixer, where, in this case, $LO+$ and $LO-$ connect to V_{b1}, and $IF+$ and $IF-$ are grounded.

From Fig. 3, when V_{GS} is less than 0.35 V for a single transistor or 0.44 V for a cascade structure, the leakage current exceeds the channel current. In our design, V_{GS} is biased by a current mirror at around 0.47 V.

In designing the LNA, we must realize that the ultimate goal is high voltage gain measured from the input to output. In low-current designs, the output resistance is improved since

$$Z_{\text{out}} \approx \frac{1}{\lambda I_{\text{DS}} + j\omega_0 C_{\text{gd},M2}} \qquad (12)$$

where λ is a constant, which depends on the channel-length modulation of the device, and we have assumed the cascade stage is biased in the saturation region. Smaller device size also results in lower output capacitance. Hence, for our design, we can accept low g_m for the advantage of high g_m/I_{DS} and high Z_{out}. Our resulting voltage gain is enough to meet the receiver requirements. The reader should remember that the LNA will be loaded by an impedance equal to the following stage's input impedance, which will appear in parallel with Z_{out} (see Section III-C). Therefore, lowering I_{DS} past a certain point will result in insufficient voltage gain.

IV. SIMULATED AND MEASURED RESULTS

A. Design for Measurement

The LNA was designed and fabricated using CSM's 0.18-μm RF CMOS process. For measurement purposes, the standard practice is to design a buffer to match the output port to the 50-Ω load of the measuring equipment. Unfortunately, it is difficult to accurately model both the gain and noise contribution of such a buffer, and it will inevitably distort the frequency response characteristics of the LNA.

In order to avoid the need for a buffer, we replaced R_d with the simple resistive divider attenuator shown in Fig. 4. This attenuator was used for measuring voltage gain. NF was measured separately. Since on-chip matching of resistors is extremely accurate (within 0.1%) [12], the voltage gain can be accurately deembedded with knowledge of the resistor ratios and the measured S_{22}. The 900-Ω resistor is formed by three 300-Ω resistors in series and the 50-Ω resistor is formed by six 300-Ω resistors in parallel. The nine resistors were placed in three rows and three columns with the three series resistors forming the second

row. This common-centroid arrangement minimizes the effects of process variation.

From Fig. 4, V_{b1} and V_{b2} are controlled by a cascode current mirror. The current to the LNA and the current mirror come from separate supply voltages, allowing us to accurately measure the LNA current consumption. V_{b1} and V_{b2} are ac grounded. Not only does this remove noise arising from the current mirror, but it also prevents feedback through the gate–drain capacitance of the cascade transistor from lowering the output impedance and, hence, the voltage gain. V_{b2} is set to around 1.2 V to allow the supply voltage to vary from 1.5 to 1.8 V without significantly affecting the voltage gain. The 10-pF capacitor is a bypass capacitor.

The fabricated design includes a quadrature passive mixer to properly account for LNA loading. The passive mixer has recently gained a lot of attention and has been used in several studies [8], [13], [14] for its low power and low flicker noise, making it appealing for direct conversion and low-IF receivers. In this design, the quadrature passive mixer is properly biased, but the LO signal is shorted to ground. The single balanced mixer schematic is shown in the inset of Fig. 4. In a typical passive mixer, a large capacitor is added between $IF+$ and $IF-$ to ac ground any RF signals [13]. With no LO signal to make the outputs differential, we instead chose to ground the mixer outputs. Two such single balanced mixers were used to load the LNA to account for both the in-phase and quadrature (I and Q) paths. In a fully differential system, two LNAs are used and each is loaded by a pair of single balanced mixers with cross coupled outputs of the corresponding I and Q mixers. In our design, small switch sizes are used to increase the load impedance seen by the LNA and the LO. However, the switches are directly in the signal path, and the mixer noise performance degrades as the device width reduces and resistance increases. This is compensated by the high LNA gain. Another drawback to small switch sizes is device mismatch due to process variation. Mismatch between the I and Q paths leads to loss in image rejection. For the IEEE 802.15.4 standard, however, the image rejection requirement is equal to the signal-to-noise (SNR) requirement [8], which is only 0.5 dB [1]. The mixer input impedance was derived in [13], where the switch capacitance was not included.

The derivation in [14] shows that small device size and low duty cycle are favorable for high input impedance. Simulations on the passive mixer show that the input impedance is $1042 \angle -66.25$ ($2588~\Omega$ in parallel with 57 fF).

B. Voltage Gain and NF Measurement

For accurate measurement, the voltage gain and NF were measured from separate output pads. From Fig. 4, the voltage gain was measured from Output 1, and the NF was measured from Output 2. The actual LNA output node is also marked in Fig. 4. When one output pad is under test, the other is considered an open circuit and ideally has no effect on the circuit. In practice, the pad introduces a small capacitance to ground. The true resistance of the 50-Ω resistor in Fig. 4 can be approximated as

$$R_{\text{out}} = 50 \cdot \frac{1 + S_{22}}{1 - S_{22}}. \tag{13}$$

From the output port, the resistance looking into the 900-Ω resistor appears as a much larger value since it appears in series with the output impedance of the cascade transistor combined with the input impedance of the mixer. Therefore, its contribution to S_{22} is negligible. The overall voltage gain is

$$G_{\text{LNA}} = \left(1 + \frac{900 \cdot (R_{\text{out}} + 50)}{R_{\text{out}} \cdot 50}\right) S_{21}. \tag{14}$$

Measuring the NF from the attenuator output is complicated due to the deembedding. Furthermore, the circuit noise level is already very low so passing it through an attenuator can only degrade the measurement accuracy. For these reasons, the NF was measured from Output 2. Before measuring the NF, the system is calibrated to deembed any noise resulting from cables, the probe to wafer connection, and the load. Since the load noise is deembedded, loading of the LNA with a small resistance (50 Ω) will not affect the measured NF as long as the dc characteristics of the LNA remain the same. The same cannot be said of voltage gain.

C. Measurement Results

The S-parameters of the fabricated LNA were measured with a -15-dBm input power, which is higher than the required $P_{1~\text{dB}}$. This was necessary in order to properly calibrate the test equipment. Fig. 5 shows the measured S_{11} and deembedded voltage gain. From Fig. 5, the optimum operating frequency is 2.52 GHz, but the circuit has better than 15-dB input matching over the desired ISM bandwidth. Fig. 6 shows the measured versus simulated NF of the LNA. The data was averaged over the four corners of the wafer. The gain variation for the wafer was 0.25 dB and the NF variation was 0.11 dB at 2.4 GHz when the current was maintained at 630 μA. The measured NF exceeded the simulated NF by 1 dB. This large difference is attributed to the poor noise modeling in the subthreshold region. The simulated $P_{1~\text{dB}}$ is -15 dBm and the IIP_3 is -10 dBm.

As shown in Fig. 5, the LNA was purposely designed with a positive frequency offset in order to account for un-modeled parasitic capacitances and inductances. The measured S_{11} is thus shifted to the left. Fig. 7 shows a micrograph of the chip. The LNA area is approximately 500 μm $\times$ 360 μm. From the micrograph, it is obvious that the inductor including the peripheral
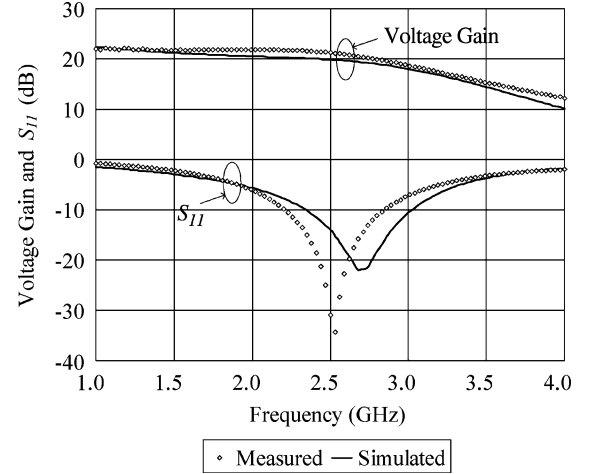
Fig. 5. Measured and simulated S_{11} and voltage gain (in decibels) versus operating frequency.
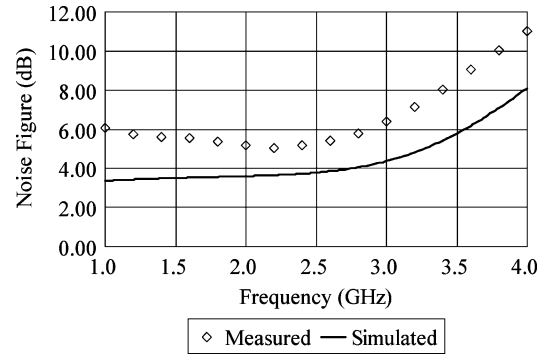
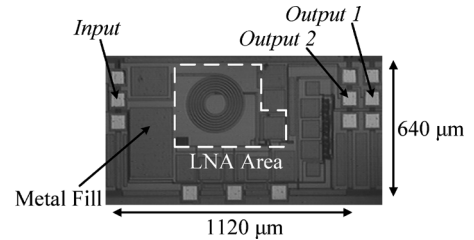Fig. 6. Simulated and measured NF versus frequency.

Fig. 7. Micrograph of the fabricated LNA.

area, which cannot be used takes up most of the LNA area (approximately 90%). This stresses the importance of minimizing the number of on-chip inductors.

D. Discussion

In order to properly analyze the LNA's performance, we compare our design to several recently published studies in Table II. Designs in [15] and [16] are subthreshold designs. In [16], the output is matched to a 50-Ω load, which, as shown in Section III, results in suboptimal voltage gain. The LNA in [8] achieves significantly higher gain than this study, while using double the current consumption. The high gain is a result of the two-stage current reuse topology employed. Multistaging increases gain exponentially while increasing current consumption linearly. The design requires stacking four transistors and three inductors. Such high gain adds strain to the linearity requirements of the

TABLE II
COMPARISON OF PROPOSED LNA AND CURRENT LITERATURE

Specification	This Work	[8][a]	[9]	[15]	[16]	[16]
DC Current (μA)	630	1200	4400	230	670	260
Voltage Gain (dB)	21.4	33	18	13.6	9.1	4.5
S_{11} (dB)	-19	-	-	-5	-13	-13
P_{1dB} (dBm)	-15	-	-13	-0.2	-25	-19.5
IIP_3 (dBm)	-11	-8.7	-3	7.2	-11	-10.5
NF (dB)	5.2	5.7	3.5	4.6	4.7	6.3
Frequency (GHz)	2.4	2.4	2.4	1	3	3
Inductor Count	1	3	3	3	4	4
Technology	0.18μm	0.18μm	0.35μm	0.18μm	0.13μm	0.13μm

[a] NF is for the entire receiver. The theoretical minimum NF for a common gate amplifier with matched input (used in [8]) is 2.2 dB [17].
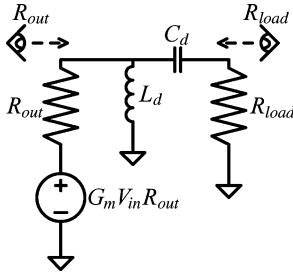

Fig. 8. Small-signal equivalent output matching network of Fig. 1(a).

following stages. The design in [9] achieves the lowest NF, but this comes at the cost of the highest current consumption. Such low NF is not necessary for our application. It should also be noted that [9] uses 0.35-μm technology. All of the LNAs are fully integrated, but this study requires only one inductor, while the other designs require at least three. The number of inductors is one of the main factors in determining the overall silicon area and resulting cost of an RF integrated circuit (RFIC).

V. CONCLUSION

A fully integrated LNA was designed based on the IEEE 802.15.4 standard. In Section II, we showed that the LNA NF is not a critical performance parameter for the IEEE 802.15.4 standard. The required performance was shown and justified, and an architecture was proposed that best suits the requirements. The design method was explained, the LNA was fabricated, and its performance was measured. The measured dc current consumption is among the lowest in current literature, while the gain is over 20 dB. The fabricated LNA uses only one inductor to minimize the area, thereby improving the cost effectiveness of the design.

APPENDIX

Fig. 8 shows the small-signal output matching network of Fig. 1(a). R_{out} approximates the output resistance of the cascade transistor combined with the parallel parasitic impedance of L_d. C_d is of sufficiently high Q that its parasitic resistance can be ignored. The matching network is, therefore, considered

ideal, and the signal power going into the network from the left is equal to the power across the load R_{load}. At resonance, we can write

$$\frac{1}{2}G_m^2 V_{\text{in}}^2 R_{\text{out}} = \frac{V_{\text{out}}^2}{R_{\text{load}}}. \tag{15}$$

Therefore, the voltage gain at the resonant frequency can be calculated as

$$\left|\frac{V_{\text{out}}}{V_{\text{in}}}\right| = \frac{1}{2}G_m\sqrt{R_{\text{out}}R_{\text{load}}}. \tag{16}$$

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Aaron V. Do (S'05–M'06) was born in Wellington, New Zealand, in 1982. He received the B.Sc. degree in electrical engineering from The University of Texas at Austin, in 2004, the M.Eng. degree in electrical and electronic engineering (with a specialization in LNA and passive mixer design for direct conversion receivers) from Nanyang Technological University, Nanyang, Singapore, in 2006, and is currently working toward the Ph.D. degree (part time) at Nanyang Technological University.

He is currently a Research Associate with Nanyang Technological University. His research is focused on ultra-low power RF front-end circuit and system design.

Chirn Chye Boon received the B.E. degree (Hons.) in electronics and Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

In 2005, he joined NTU as a Research Fellow and became an Assistant Professor later that same year. Prior to that, he was a Senior Engineer with Advanced RFIC. He specializes in direct conversion RF transceiver front-end design, phase-locked-loop frequency synthesizers, clock and data recovery circuits, and frequency dividers.

Prof. Boon is a reviewer for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS, the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.

Manh Anh Do (M'05–SM'05) received the B.Sc. degree in physics from University of Saigon, Saigon, Vietnam, in 1969, and the B.E. degree (Hons.) in electronics and Ph.D. degree in electrical engineering from the University of Canterbury, Canterbury, New Zealand, in 1973 and 1977, respectively.

From 1977 to 1989, he held various positions including Research and Development Engineer and Production Manager with Radio Engineering Ltd., Research Scientist with the Fisheries Research Centre, Wellington, New Zealand, and Senior Lec-
turer with the National University of Singapore. In 1989, he joined the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), as a Senior Lecturer, became an Associate Professor in 1996, and a Professor in 2001. He has been a consultant for numerous projects in the Singapore electronic industry, and was the principal consultant for the design, testing, and implementation of the $200 million Electronic Road Pricing (ERP) island-wide project in Singapore (1990–2001). From 1995 and 2005, he was Head of the Division of Circuits and Systems, School of Electrical and Electronic Engineering, NTU. He is currently the Director of Centre for Integrated Circuits and Systems (CICS), NTU. He has authored or coauthored over 200 papers in the areas of electronic and communication circuits and systems. His current research concerns digital and mobile communications, RF integrated-circuit (IC) design, mixed-signal circuits, and intelligent transport systems. Prior to that, he specialized in sonar designing, biomedical engineering, and signal processing.

Dr. Do is a Fellow of the Institution of Engineering and Technology (IET), U.K., a Chartered Engineer in the U.K., and a Professional Engineer (Singapore). He was a council member of the IET from 2001 to 2004. Since April 2005, he has been an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.

Kiat Seng Yeo (M'00) received the B.E. degree in electronics (Hons.) and Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore in 1993 and 1996, respectively.

In 1996, he began his academic career as a Lecturer, became an Assistant Professor in 1999, and then an Associate Professor in 2002. from 2001 to 2005, he was Sub-Dean (Student Affairs), during which time he held several concurrent appointments as Program Manager of the System-on-Chip flagship project, Coordinator of the Integrated Circuit Design Research Group, and Principal Investigator of the Integrated Circuit Technology Research Group, NTU. He is on the Advisory Committee of the Centre for Science Research and Talent Development, Hwa Chong Junior College. In July 2005, he became Head of Circuits and Systems for a three-year period. He is also a consultant/advisor to statutory boards and multinational corporations in the areas of semiconductor devices, electronics, and integrated circuit design. He authored *Low-Voltage, Low-Power VLSI Subsystems* (McGraw-Hill, Int. ed., 2005), *Low-Voltage Low-Power Digital BiCMOS Circuits: Circuit Design, Comparative Study and Sensitivity Analysis* (Prentice-Hall, 2000, Int. ed.), and *CMOS/BiCMOS ULSI: Low-Voltage, Low-Power* (Prentice-Hall, NJ, 2002, Int. ed.). The latter was translated into a Chinese language version. He holds more than six patents and has additional patents pending. He has authored or coauthored over 200 papers on CMOS/BiCMOS technology and integrated circuit design appearing in leading technical journals and conferences worldwide. He is a Technical Reviewer for several international journals. He was listed in Marquis' *Who's Who in the World* and Marquis' *Who's Who in Science and Engineering*.

Prof. Yeo was the technical chair of the 8th and 9th International Symposium on Integrated Circuits, Devices, and Systems (ISIC'99 and ISIC'01, respectively). He also served on the Program Committee of the International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA), Taiwan, R.O.C., and the International Symposium on Low-Power and High-Speed Chips (COOL Chips), Tokyo, Japan, in 1999 and 2002, respectively.

Alper Cabuk (M'07) received the B.Sc. degree in electrical engineering from Middle East Technical University (METU), Ankara, Turkey, in 1999, and the M.Eng. and Ph.D. degrees in electrical and electronic engineering from Nanyang Technological University (NTU), Singapore, in 2002 and 2006.

From 1998 to 1999, he was with the Information Technologies Institute (Bilten), Ankara, Turkey. He is currently a Research Fellow with NTU. His research interests include CMOS RF integrated circuit design, low-voltage low-power analog/baseband circuit design, and clock and data recovery circuits for SONET systems.