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Abstract—This Letter evaluates the bit-error rate (BER) performance of a coherent binary phase-shift keying interconnect system operating on an intra-chip wireless channel at 15 GHz. Results show that the system performance degrades with the separation distance and the data rate. A high data rate at 2 Gb/s with a low BER $< 10^{-5}$ over the entire chip of size 20×20 mm can be achieved with the transmitted power of 10 dBm.

Index Terms—bit-error rate (BER), binary phase-shift keying (BPSK), chip-scale wireless communications systems.

I. INTRODUCTION

TRADITIONAL wire interconnect systems may soon encounter their fundamental material limits. To surpass these fundamental limits, wireless interconnect systems have been proposed, which realize intra-chip interconnection at the speed of light via electromagnetic waves using on-chip antennas, receivers, and transmitters. Wireless interconnect systems can be used for both clock and data signals. They have been demonstrated recently for clock distribution at 7.4 GHz and 15 GHz in 0.25-μm and 0.18-μm CMOS technologies, respectively [1]. They have also received attention for data communication [2]. Unlike wireless clock, wireless data require a modulation scheme. Thus, the assessment of the performance of the known modulation schemes on intra-chip wireless channels appears desirable. In this Letter, the performance of a coherent BPSK interconnect system operating on an intra-chip wireless channel at 15 GHz is evaluated. Because of the simplicity of this wireless interconnect system, it can be considered as a reference system, allowing for a certain generality of the results.

II. ANALYSIS

The wireless interconnect system is shown in Fig. 1. Note that the transmitter comprises a binary phase-shift keying (BPSK) modulator, a power amplifier (PA), and a transmit antenna (TA), while the receiver comprises a receive antenna (RA), a low noise amplifier (LNA), and a BPSK demodulator. Also note that the wireless interconnect system features a unique intra-chip wireless channel. The intra-chip wireless channel can be regarded
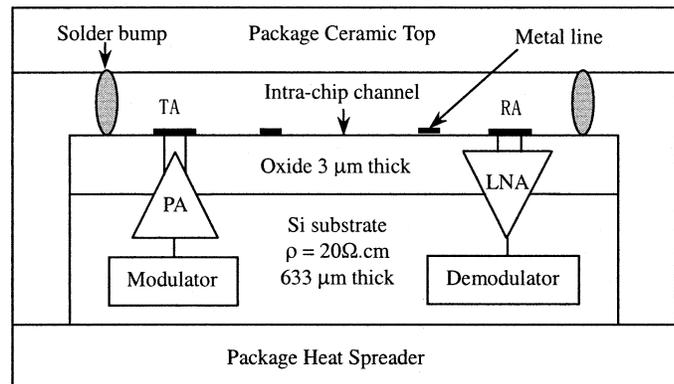
Fig. 1.   A coherent BPSK intra-chip wireless interconnect system.

as an imperfect dielectric waveguide, which supports the transmission of multi hybrid electromagnetic modes at 15 GHz [3]. The imperfectness of the dielectric waveguide is the result of the intra-chip wireless channel not being designed primarily as a wave guiding structure. This is particularly true in a packaged chip environment where exist a large number of metal lines and solder bumps. They will cause mode conversion and increase transmission loss. Similar to radio signal propagation via multipaths in an indoor wireless channel, radio signal transmission through multimodes in the intra-chip wireless channel exhibits fluctuations. Since electric dipole antennas are used, the horizontally polarized hybrid electromagnetic mode HEM_{11} dominates in the transmission, as a result, signal fluctuations over the intra-chip wireless channel follow a Rician distribution, the intra-chip wireless channel can thus be treated as a Rician fading channel [4]. The treatment of the intra-chip wireless channel as the Rician fading channel agrees with the on-chip measurements of the radio signal transmission at 15 GHz. The measurements reveal that the signal fade depth never exceeds 10 dB [1]. In addition, the time delay spread of the intra-chip wireless channel is calculated to be negligible as compared with the data rate considered here [2]. Hence, over such a nondispersive Rician fading channel the system performance depends on the signal-to-noise ratio. The signal-to-noise ratio has been estimated for intra-chip wireless clock signal distribution [5]. It is found that the signal is corrupted by the thermal noise and the switching noise. The thermal noise dominates the switching noise at the frequency of interest for wireless clock. It is believed that the thermal noise also dominates the switching noise for intra-chip wireless data communication. This is because most of the switching noise coupled to the antenna is common mode in nature [6]. The dipole balanced and the LNA differential structures reject

most of the common mode noise [5]–[7]. Hence, the BER performance of the BPSK wireless interconnect system can be evaluated as

$$\text{BER} = P_e = \int_0^\infty P_e(X) p(X) dX \tag{1}$$

where $P_e(X)$ is the probability of error for the BPSK modulation at a specific value of signal-to-noise ratio X, $X = \alpha^2 E_{rb}/(N_o + S_o)$, and $p(X)$ is the probability density function of X due to the fading channel. E_{rb}, N_o, and S_o are constants that represent the average energy per bit, the thermal noise power density, and the switching noise power density in a nonfading AWGN channel. The random variable α^2 is used to represent instantaneous power values of the fading channel, with respect to the nonfading $E_{rb}/(N_o + S_o)$ [8]. Using the complementary error function, $P_e(X)$ for the BPSK modulation is given below:

$$P_e(X) = \frac{1}{2}\text{erfc}(\sqrt{X}). \tag{2}$$

For the intra-chip wireless channel, the fading amplitude α has a Rician distribution, so the fading power α^2 and consequently X can be expressed as

$$p(X) = \frac{1+K}{\Gamma} \exp\left[-\frac{X(1+K)+K\Gamma}{\Gamma} I_0\left(\sqrt{\frac{4(1+K)KX}{\Gamma}}\right)\right] \tag{3}$$

where $\Gamma = \bar{\alpha}^2 E_{rb}/(N_o + S_o)$. is the average value of the signal-to-noise ratio, K is the specular-to-random ratio of the Rician distribution, and $I_o(y)$ is the zero-order modified Bessel function of the first kind. Substituting (2) and (3) in (1) and solving the integration we get the BER performance of the BPSK wireless interconnect system. The average energy per bit E_{rb} is given by

$$E_{rb} = E_{tb} + G_{tr} + G_r \tag{4}$$

where E_{tb} is the transmitted energy per bit in dBm, G_{tr} is the average value of the transmission gain between the transmit and receive antennas in decibels, and G_r is the gain of the receiver in dB. The average value of the transmission gain G_{tr} can be obtained from an on-chip measurement or from a full wave electromagnetic analysis [1], [7]. Fig. 2 shows the average value of G_{tr} versus frequency and distance for dipole antennas of length 2 mm. As can be seen from the figure, the average value of G_{tr} increases with frequency and decreases with distance. It should be mentioned that G_{tr} in the figure does not include the reduction due to the chip metal lines in between the transmit and receive antennas. This reduction can be up to 10 dB at 15 GHz. The thermal noise power spectral density N_o is given by

$$N_o = kT_oF = kT_o\left(\frac{T_{ant}}{T_o} + F_r\right) \tag{5}$$

where k is the Boltzman constant, T_o is the reference temperature (typically taken as 290 K), T_{ant} is the antenna temperature (taken as 330 K), and F_r is the receiver noise figure. The
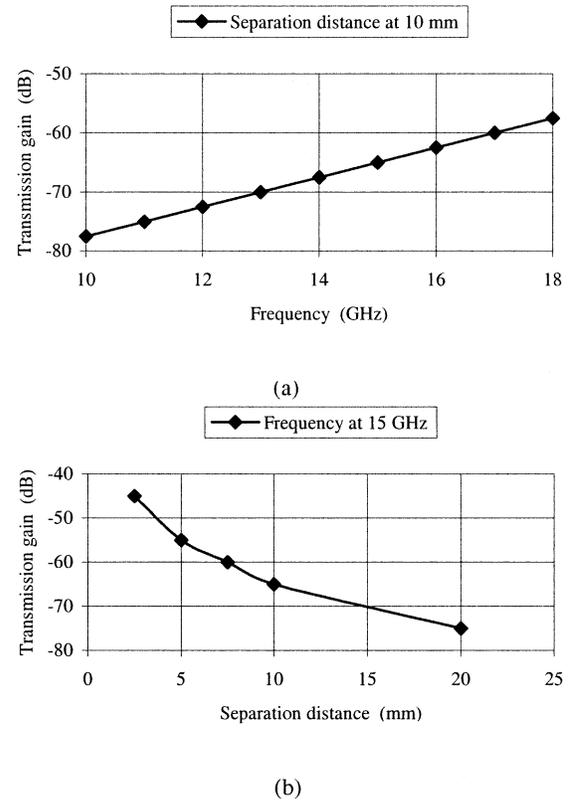

(a)

(b)

Fig. 2.   Average values of the transmission gain versus frequency and distance.

receiver for wireless data must be broadband and should be designed to compensate the signal loss over the transmission. It is assumed that G_r and F_r are 20 and 10 dB at 15 GHz, respectively. This assumption is supported by a recent study of CMOS implementation of a broadband software radio [9]. The switching noise power spectral density S_o is given by

$$S_o = \frac{\sum \frac{\chi_i A_i^2}{2}}{B_w} \tag{6}$$

where χ_i is the coupling factor, A_i is the amplitude of the switching noise harmonics within the system bandwidth B_w. For a BPSK system, B_w is equal to the data rate. The voltage supply and clock rate of a typical 0.18-μm CMOS technology are 1.8 V and 2.0 GHz, respectively. Most digital logic circuits operate on square wave whose harmonics are odd-order. Thus, for the case of the clock frequency at 2 GHz, only the seventh harmonic is within the system bandwidth, while for the case of higher clock frequencies, the lower order harmonic is used. The amplitude of the seventh harmonic A_7 is equal to 0.33 V. The coupling factor χ_7 is estimated to be 2.6×10^{-10} from the measured switching noise being 10 dB lower than the thermal noise [5]. Fig. 3 shows the BER performance of the intra-chip wireless interconnect system for the case of the transmitted power at 0 dBm and the ratio K of 10 dB. As shown, the BER performance degrades with the separation distance and the data rate. It degrades from 1.43×10^{-5} at 2.5 mm to 2.1×10^{-4} at 20 mm. It also degrades from 4.13×10^{-5} at 2 Gb/s to 7.97×10^{-5} at 5 Gb/s. Thus, to achieve a high data rate at 2 Gb/s with a low $\text{BER} < 10^{-5}$ over the entire chip of size 20×20 mm,
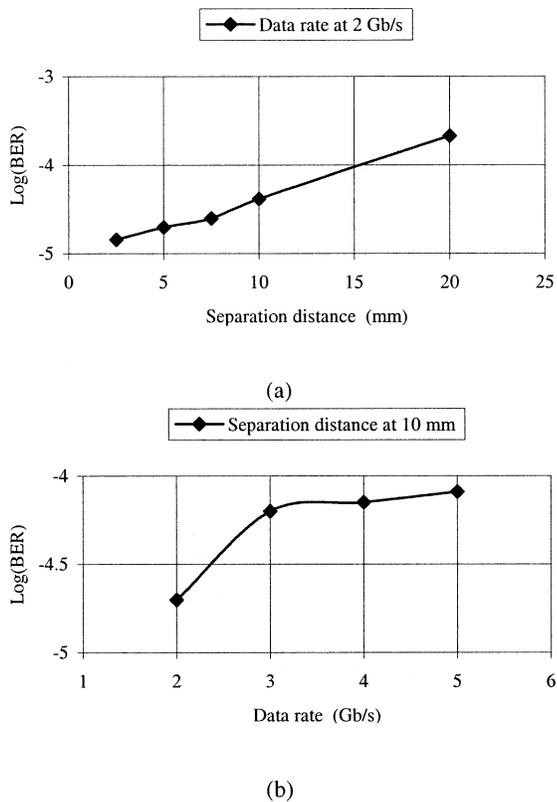
(a)

(b)

Fig. 3.   BER versus transmitter-receiver separation distance and data rate.

helps save real estate of the chip area. It is therefore believed that the heat problem and area penalty originated from the circuitry of the intra-chip wireless interconnect systems for data communication will not severely affect its feasibility. They will become less problematic as CMOS and radio technologies advance.

III. CONCLUSION

The performance of a coherent BPSK interconnect system operating on an intra-chip wireless channel at 15 GHz has been evaluated for the first time. The evaluation shows that the performance of the coherent BPSK intra-chip wireless interconnect system degrades with the separation distance and the data rate. A high data rate at 2 Gb/s with a low $\mathrm{BER} < 10^{-5}$ over the entire chip of size 20×20 mm is achievable with the transmitted power of 10 dBm.

one can simply increase the transmitted power, for example, to 10 dBm. The increase in the transmitted power results in large power consumption, which generates extra heat in the chip and may affect the realization of the intra-chip wireless interconnect systems for data communication. Alternatively, one can increase the transmission gain by properly inserting aluminum nitride (AIN) layer. The insertion of an AIN layer does not generate extra heat but provides an efficient means for heat removal [10]. Furthermore, one can use a channel-coding technique to improve BER performance or employ the principle of minimum energy design of on-chip wireless data network by sharing common RF front-ends among many transmitters and receivers. The concept of sharing common RF front-ends also

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