Minimum input sensitivity of high-order multi-stage sigma-delta modulator with first-order front-end

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described in Table I have been used, as well as three transition filters having lengths 1024, 512, 256. For this bank, we obtained $E_r = 6.18E - 04$ and $E_{at} = -98.0$ dB. As can be seen, even if relatively long filters and large decimation factors are involved, the proposed procedure yields a good reconstruction performance.

V. CONCLUSION

In this brief, we have proposed an extension of the eigenfilter approach to design approximately power complementary filters having both real and complex coefficients. In spite of its simplicity, when associated to properly chosen weighting functions, it allows to design high attenuation prototypes that can be used to implement uniform, and nonuniform banks with good reconstruction properties.

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Minimum Input Sensitivity of High-Order Multi-Stage Sigma-Delta Modulator with First-Order Front-End

C. K. Ong, L. Siek, and L. S. Ng

Abstract—Employing multi-stage sigma-delta modulators has provided an effective means of eliminating stability problems while achieving high-resolution analog-to-digital conversion. However, component matching has become more stringent than a single-stage modulator. Mismatches cause loss in the modulators signal-to-noise ratio (SNR), but to a certain class of multi-stage modulators, discontinuity is also apparent in its SNR characteristics. This class of modulators employs a first-order modulator in its first stage. The discontinuity is caused by the nonlinearity of a first-order modulator's noise, which is related to the minimum input requirement for the first-order modulator. This brief includes the formulation of the first-order modulator's minimum amplitude, nonlinear characteristics, and its effect on multi-stage modulators.

Index Terms—Cascade sigma-delta modulator, first-order sigma-delta, minimum input, modulator noise, SNR discontinuity.

I. INTRODUCTION

Oversampling analog-to-digital conversion (ADC) using sigma-delta ($\Sigma\Delta$) modulation is very popular for high-resolution audio-band applications [1]–[3]. The continual reduction of feature size in the CMOS integrated circuit process has caused higher packing density and popularized digital signal processing (DSP). Integrating the ADC and digital-to-analog conversion (DAC) circuitry on to the same die creates a complete and cost effective DSP system. $\Sigma\Delta$ modulation ADC employing high sampling rate and digital filtering is able to achieve low noise performance and high linearity with reduced analog circuit complexity. Due to the modulator's robustness to circuit imperfections, $\Sigma\Delta$ ADC can be implemented in a digital CMOS process. Such ADC is best suited for integrating into a single-die DSP system.

The performance of the $\Sigma\Delta$ modulator is often measured by its signal-to-noise ratio (SNR), and is governed by the oversampling ratio (OSR) and the order of the modulator [4]. Various architectures were implemented over the years to increase the SNR of the modulator by means of increasing the order of the modulator. One of them is the cascaded modulator architectures [2], [5], [6]. However, cascaded architectures with first-order modulator in the first stage suffer discontinuity in its SNR when plotted against its input amplitude. This phenomenon will be further discussed in Section VI.

II. SIGNAL ANALYSIS

Fig. 1 shows the block diagram of a first-order $\Sigma\Delta$ modulator.

The output of the modulator is a form of pulse density signal as shown in Fig. 2. A modulator with higher input level yields more logic "1" at the output than one with a lower input level.

The input level shown in Fig. 2(a) is at 90% of its full scale and its corresponding output has 90% of logic "1" for a certain period. Likewise, in Fig. 2(b), the percentage is 30%. Hence, for a certain period, the integration of the input signal is equivalent to the integration of its

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 Fig. 1. First-order $\Sigma\Delta$ modulator.

Fig. 2. First-order modulator's output. Input level at (a) 90% and (b) 30%.

corresponding output. The previous statement is only valid for some period, which are constrained by the following conditions:

$$t_P = \frac{N_Q}{x_{in}}$$

where

- t_P nonzero positive integer representing the unit time period;
- N_Q total number of logic "1" at the output within t_P ;
- x_{in} real number the input level;

e.g., for $x_{in} = 0.3$ and $N_Q = 3, 6, 9$, or $\dots$ $t_P = 10, 20, 30$, or $\dots$

For the unit time between 0–20 in Fig. 2(b), the integration of the input signal is

$$\int_0^{20} x(t) dt = 0.3 \times 20 = 6$$

and the output has six logic "1." Hence, integrating the output within the period gives a value equal to the integration of the input signal.

III. MINIMUM DC INPUT LEVEL

For a given period, the minimum dc input must be able to trigger the modulator to have a single logic "1" at the output. Hence, for that given period, the integration of minimum input level is a single logic "1."

Fig. 3. Minimum dc input level.

Fig. 4. Minimum input amplitude.

Using the same theory mentioned in the previous section, Fig. 3 shows that the minimum input level for a period of 10-unit time is 10% of the quantizer level. Hence, the minimum input level is given by the following formula:

$$x_{min} = \frac{Q}{t_u} \quad (1)$$

where

- x_{min} minimum input level;
- Q quantizer level;
- t_u even unit time.

IV. MINIMUM SINEWAVE AMPLITUDE

The minimum amplitude of a sinewave to be detected by the first-order $\Sigma\Delta$ modulator is presented in this section. From the Nyquist sampling rule, the minimum sampling frequency is two times the signal frequency. Hence, the minimum representation of a sinewave by the modulator is to trigger the output of the modulator with one logic level for each half of the signal.

For simplicity in analysis, the quantizer levels used are one and zero, and the input signal used for the modulator is the positive half of the sinewave. Fig. 4 shows the graph plotted with mathematical manipulation of the first-order $\Sigma\Delta$ modulator with the positive half sinewave input.

Applying the same theory as the dc-level input

$$\begin{aligned} &\text{Integration of the input signal} \\ &= \text{Integration of the modulator output} \end{aligned}$$

$$\int_0^{T/2} A_{min} \sin\left(2\pi f_x \frac{n}{f_s}\right) dn = Q \quad (2)$$

Fig. 5. Output power of first-order modulator, with OSR at (a) 64, (b) 128, and (c) 256.

TABLE I
FIRST-ORDER MODULATOR MINIMUM AMPLITUDE

f_x , kHz	OSR=64		OSR=128		OSR=256	
	Sim.	Cal.	Sim.	Cal.	Sim.	Cal.
0.5	-65.09	-65.09	-71.12	-71.11	-77.14	-77.14
1	-59.08	-59.07	-65.09	-65.09	-71.12	-71.11
5	-45.09	-45.09	-51.12	-51.11	-57.14	-57.14
10	-39.07	-39.07	-45.09	-45.09	-51.12	-51.11
15	-35.55	-35.55	-41.57	-41.57	-47.59	-47.59
20	-33.05	-33.05	-39.07	-39.07	-45.09	-45.09

where

- T period of the input signal f_s/f_x ;
- $A_{\min}$ minimum input amplitude;
- f_x input frequency;
- Q quantizer level;
- f_s sampling frequency $N \cdot f_n$;
- N oversampling ratio;
- f_n Nyquist rate $2 \cdot f_b$;
- f_b maximum signal frequency.

Hence

$$\frac{A_{\min}}{Q} = \pi \frac{f_x}{f_s}$$

$$20 \log \left[\frac{A_{\min}}{Q} \right] = 20 \log \left[\pi \frac{f_x}{f_s} \right], \quad 20 \log \left[\pi \frac{f_x}{N f_n} \right]. \quad (4)$$

Fig. 6. First-order modulator with noise extraction.

(3) Fig. 7. Output and noise power of first-order modulator.

Simulations were done on a first-order $\Sigma\Delta$ modulator using MIDAS [7] with its output feeding through a filter, filtering out the out-of-band frequency components. The power of the filtered output against input

Fig. 8. Three-stage third-order modulator.

amplitude level with various input frequencies were plotted as shown in Fig. 5.

Fig. 5(a)–(c) were plotted with OSR at 64, 128, and 256, respectively. The sudden loss of power within the signal band implies the inability to replicate the input signal at the output. Hence, the input amplitude before the power lost would hereafter be known as the minimum amplitude. Table I tabulated the comparison between the simulated (Sim.) results from Fig. 5 and calculated (Cal.) results from (4).

Hence, the power of the modulator output below the input's minimum amplitude is solely contributed by the modulator's noise. The next section demonstrates that the noise power below the input's minimum amplitude are significantly lesser than those above. This phenomenon has a great effect on previously reported multi-stage $\Sigma\Delta$ modulator, with its first stage being a first-order modulator.

V. FIRST-ORDER $\Sigma\Delta$ MODULATOR NOISE

To date, the first-order modulator's noise had been discussed and studied [8], [9] in the region above the input's minimum amplitude. This is not complete for studies of multi-stage modulator with first-order modulator in the first stage. The output of a first-order modulator is represented by the input signal delayed by one unit sample time and the modulator's noise. In order to extract the modulator's noise, the input signal has to be delayed by one unit sample time before noise extraction can be done. Fig. 6 shows the block diagram for extracting the modulator noise.

Simulation was done using MIDAS with input signal, $x(t)$ at 1 kHz, an OSR of 64, and Nyquist frequency of 44.1 kHz. The outputs, $y(t)$ and *noise* were passed through a low-pass filter to remove the out-of-band components before their power were obtained. Fig. 7 shows the filtered power of the output, $y(t)$ and the extracted noise, *noise* plotted against the input amplitude.

The graph, shown in Fig. 7, is divided into the modulator's normal operation mode and the nonoperation mode by the input's minimum amplitude line at -59 dB. In the normal operating mode, $y(t)$ represents the normal modulator output and *noise* represents the modulator's noise. In the nonoperation mode, $y(t)$ could not represent the input signal, and hence, only represents the modulator's noise. The power of *noise* in the nonoperation mode represents the combination of the input signal and the modulator noise, as the cancellation of input signal is no longer possible as in the normal operating mode.

Hence, the modulator's noise is represented by *noise* during the operation mode and by $y(t)$ during the nonoperation mode. These suggested that the power of the modulator's noise gradually increases as the input approaches the minimum amplitude line in the normal op-

erating mode and dropped sharply when the modulator is in the non-operating mode. This phenomenon would hereafter be known as the nonlinear first-order modulator's noise.

VI. EFFECT ON MULTI-STAGE MODULATOR

A multi-stage $\Sigma\Delta$ modulator with a first-order modulator in its first stage [10], [11] would hereafter be known as multi-stage first-order front-end. Such a multi-stage modulator will be affected by the nonlinear first-order modulator's noise. Fig. 8 shows the basic architecture of a three-stage third-order $\Sigma\Delta$ modulator formed by cascading three first-order modulators.

The first-order modulator's output is represented by a delayed input and a differentiated quantizer error, e.g.,

$$y_1 = xz^{-1} + e_1(1 - z^{-1}) \quad (5)$$

where

$$z^{-1}$$

delay unit;

$$e_1$$

quantizer error introduced at Q_1 ;

$$I(z) = \frac{z^{-1}}{(1-z^{-1})}$$

transfer function of a delay integrator.

In order to obtain a higher order performance in a multi-stage modulator, the first-stage quantizer error is extracted via gains F_1 , $1/G_1$, and B_1 , and fed to the second-stage modulator. The gains are set to unity value for proper extraction of the quantizer noise in a first-order modulator. The output of the second-stage modulator would be

$$y_2 = x_1z^{-1} + e_2(1 - z^{-1}) \quad (6)$$

where

$$x_1 = -e_1.$$

The error e_1 is canceled by delaying y_1 by one unit sample time and differentiating y_2 before adding them together.

Hence

$$D(z) = z^{-1} \\ H(z) = 1 - z^{-1}.$$

Once e_1 is cancelled, e_2 has become a second-order noise, and hence a second-order performance is achieved. Likewise, to obtain a third-order modulator, the third-stage modulator can be analyzed as before.

Fig. 9. Three-stage third-order modulator's SNR.

When the amplitude of input x becomes smaller than the minimum amplitude, y_1 does not replicate the input anymore. Hence, x_1 is now the integrated signal of input x and the first-stage nonoperating mode quantizer's noise. Though the input signal and the modulator's noise are fed through the second stage, noise cancellation still takes place. The effect of the nonlinear first-order modulator's noise surfaces when error is introduced at gain blocks G_1 and G_2 , resulting in the inability to cancel the previous stage noise completely in the normal operating mode. Fig. 9 shows a SNR graph plotted against input amplitude variation with different values of gains and input frequency at 1 kHz, OSR of 64, and Nyquist frequency of 44.1 kHz.

When $G_1 = G_2 = 1$, the modulator operates in a perfect noise cancellation condition. When gain error is introduced, such that $G_1 = G_2 = 0.99$, and the SNR suddenly deteriorates when input amplitude goes above the minimum amplitude line (MAL). This is due to the cancellation of error, e_1 is not complete due to the gain errors. Below MAL, the SNR does not change much due to the low power noise in the non-operation mode of the first-stage first-order modulator. This suggested the discontinuity in the SNR graph at the MAL in Fig. 9.

VII. CONCLUSION

Every $\Sigma\Delta$ modulator requires minimum amplitude to operate, and this amplitude is related to its input frequency and sampling rate. Presented in this brief are the first-order $\Sigma\Delta$ modulator's minimum amplitude and its effect on a third-order multi-stage first-order front-end modulator. Though studies had shown that first-order in the first stage is less preferred than a second-order [10], [11], this brief presents the discontinuity in the dynamic range that is introduced by a multi-stage first-order front-end architecture. The previous section implies that any multi-stage modulator with first stage being a first-order modulator will suffer the cleft in SNR as described previously in a third-order multi-stage modulator.

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