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Sensitivity Analysis of Coupled Interconnects for RFIC Applications

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***Abstract*—This paper investigates the sensitivity of on-wafer coupled interconnects to the Si CMOS process parameters. Experiments are conducted to emulate state-of-the-art and future technologies. Some important parameters characterizing the coupled interconnects have been examined. The influence of the process parameters on transmission, reflection, near-end, and far-end crosstalk capacities of the coupled interconnects are discussed.**

***Index Terms*—CMOS process, coupled interconnects, sensitivity.**

I. Introduction

THE recent decade has witnessed the explosion of the development of wireless communication. Portable devices such as pagers, cellular and cordless phones, global positioning system (GPS) devices, wireless local-area network (WLAN) devices, etc., have penetrated into all aspects of our daily lives. Boosted by the demands of this rapidly growing wireless mobile communication market, there is an increasing interest in the development of the radio frequency (RF) integrated circuit (IC). Because of the mature technology, low fabrication cost, high packing density, as well as low power consumption, complementary metal oxide (CMOS) technology has become a strong contender compared with other available technologies, such as the GaAs metal semiconductor field effect transistor (MESFET), heterojunction bipolar transistor (HBT), etc. [1].

Due to the combination of the increasing circuit complexity and higher operating frequencies of CMOS ICs, the circuit performance becomes more and more subjected to the interconnects [2]. On the other hand, the evolving pace of the CMOS process technology is truly spectacular. The process parameters are optimized to improve the circuit performance. However, influences of the process parameter variations on the interconnects have rarely been reported in the literature.

In our previous work [3], influences of the process parameters, such as conductivity of the substrate, thickness, and permittivity of the dielectric, as well as conductivity of the metallic conductor on the transmission and reflection capacities of the single interconnect, are examined. However, in a real case, the density of the interconnects are very high. The crosstalk among interconnects is one of the most important internal EMC problems [4]. Hence, it would be very useful to provide information about the sensitivity of the interconnects.

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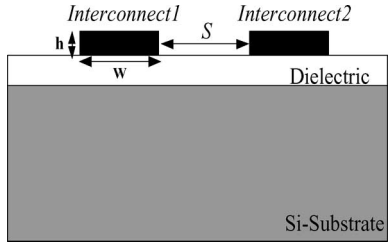

Fig. 1. Cross view of the test structure.

The objective of this paper is to investigate the sensitivity of two interconnects to the process parameters at radio frequencies. The dependance of the transmission, reflection, far-end, and near-end crosstalks of the two interconnects on the process parameters are investigated. This examination is dedicated to the interconnects on the top metal layer since it is most commonly allocated for routing critical high-frequency paths.

This paper is organized as follows. In Section II, the test structure is presented. The influences of the process parameters to the coupled interconnects are examined in Section III. Finally, the paper is concluded in Section IV.

II. Test Structure

In order to analyze the sensitivity of the two interconnects, a large number of interconnect samples with various process parameters are needed. There are two ways to obtain the required samples. The most straightforward one is to design and fabricate all the possible test structures with different process parameters. However, it is extremely costly, time-consuming, and impractical. An alternative way is to design and fabricate several typical test structures and adopt an electromagnetic (EM) simulator, using the fabricated samples to calibrate the EM simulator. Then, other possible interconnect stuctures can be investigated using calibrated EM simulation.

In this work, IE3D from Zeland Software Inc. is employed to do the EM simulations. The IE3D is a full-wave, method of moment (MOM) simulator and employs an automatic nonuniform mesh generator with rectangular and triangular cells [5].

The cross view of the test structure is shown in Fig. 1. Three sets of the test structures with various lengths and widths are designed and fabricated using a 0.18-μm RF CMOS process by Chartered Semiconductor Manufacture Ltd. (CHRT). In order

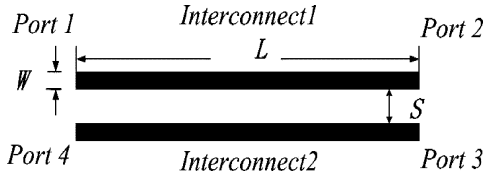

Fig. 2. Top view of the test structure.

to calibrate the settings of the EM simulator, on-wafer measurements of the three sets of fabricated test structures are performed [6].

In the next section, the interconnect structure, as illustrated in Fig. 1, is examined. The length (L) of both the interconnects is 400 μm, the width (W) is 10 μm, the height (h) is 3.5 μm, and the line spacing (S) of the two interconnects is 10 μm. The top view of the structure and the assignment of the ports are shown in Fig. 2. *Interconnect* 1 is assumed to be the active line, and *Interconnect* 2 is assumed to be the victim line. An input signal is applied to *port1*. S-parameters, i.e., S_{11}, S_{21}, S_{31}, and S_{41} are examined.

III. Influences of the Process Parameters

Four major process parameters are considered, namely conductivity of the substrate, permittivity of the dielectric, thickness of the dielectric, and conductivity of the metallic conductor. During simulation, these four parameters are changed respectively. Only one parameter is changed each time, while the rest are kept unchanged. The variation range of the parameters is chosen to emulate the state-of-the-art and future Si CMOS technologies.

A. Conductivity of the Substrate

In CMOS technology, low-resistivity substrate is used to improve the yields and suppress the latchup. The performance of the on-wafer interconnects is significantly affected by the lossy nature of the silicon substrate [7]. In the current technology, the substrate conductivity (σ_1) is approximately 6–50 S/m (2–18 Ω-cm) [8]. In some processes, the conductivity of the substrate may reach as high as 5×10^3 to 1×10^4 S/m (10–20 m Ω-cm) [9].

In order to study the influence of the substrate conductivity, typical values of 6, 50, 5×10^3, and 1×10^4 S/m as well as 19 S/m, which is provided by the CHRT process, are used for the simulation. Comparisons of S_{11}, S_{21}, S_{31}, and S_{41} are shown in Figs. 3–6, respectively.

For S_{11}, as shown in Fig. 3, it is observed that both its dependence on the substrate conductivity and the corresponding values are the same as that of the depicted single interconnect in [3]. It indicates that the reflection of the active line is not influenced much by the appearance of the victim line. For S_{21}, it follows the same dependent trend [3]. However, there is an interesting phenomenon that can be noticed in Fig. 4. For low conductivities, the corresponding values of S_{21} are smaller than those of the single interconnect in [3]. However, for interconnects with very high substrate conductivities, i.e., 5000 and 10 000 S/m, the values of S_{21} do not change much from those

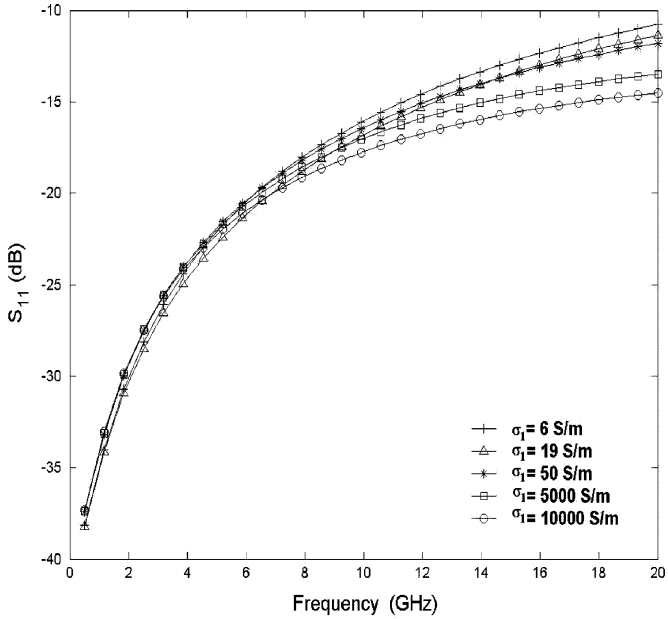

Fig. 3. Comparison of S_{11} with respect to various substrate conductivities.

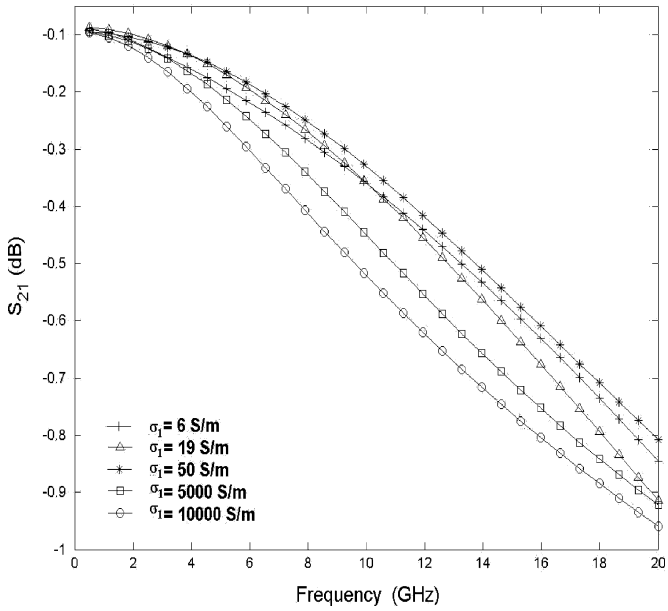

Fig. 4. Comparison of S_{21} with respect to various substrate conductivities.

of the single interconnect. The reason is that the energy loss caused by the coupling can be neglected compared to the substrate losses due to a high conductivity of the substrate. Figs. 5 and 6 illustrate the crosstalks at the far and the near-end of the victim interconnect. It can be observed that the interconnect with larger S_{11} has larger near-end crosstalk, while the interconnect with larger S_{21} suffers more from far-end crosstalk. This is because the energy in the victim line is originated from the energy in the active line. Given the same dielectric permittivity and interconnect physical dimension, the coupling capacitance [10] of the two interconnects is identical. The more the energy at the active line, the more the coupled energy at the corresponding victim line.

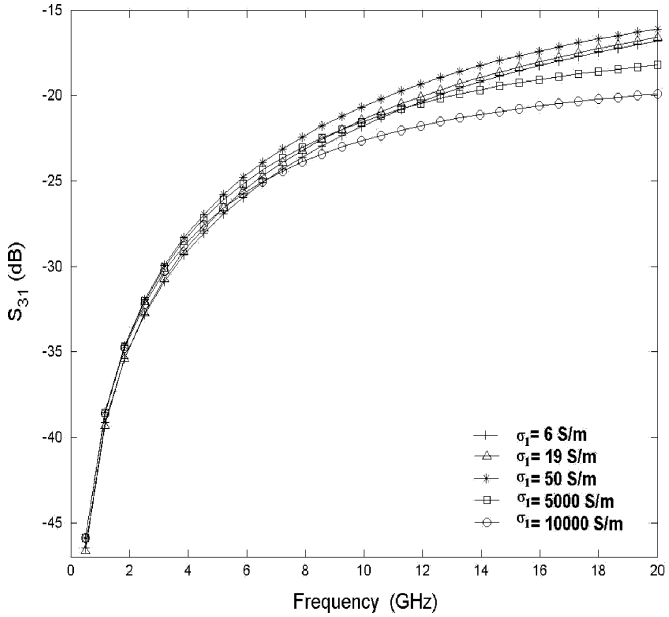

Fig. 5. Comparison of S_{31} with respect to various substrate conductivities.

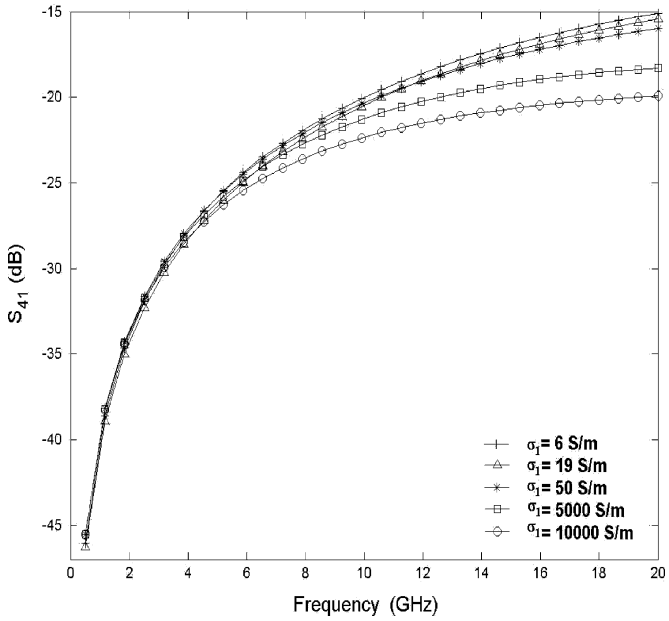

Fig. 6. Comparison of S_{41} with respect to various substrate conductivities.

B. Distance From the Substrate

The current trend of the metal technology evolution is shown in Fig. 7. Due to the increase of the metal layers, the vertical dimensions do not scale down with the horizontal dimensions. When it comes to 2007, there will be up to 10 metal layers, and the top metal layer will be away from the Si substrate up to 16 μm [11].

From Figs. 8–11, comparisons of S_{11}–S_{41} with different top metal distances (T) from the substrate are illustrated. Three chosen distances are 5.5 μm, which is provided by CHRT; 16 μm, which is the predicted value for the year 2007; and 10 μm, which is the value in between.

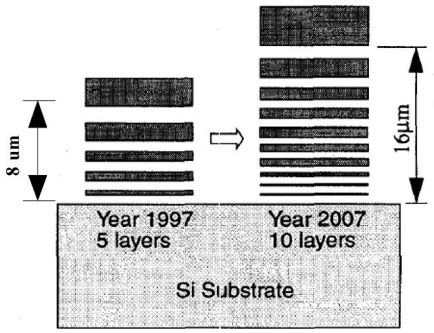

Fig. 7. Trend of interconnect stack.

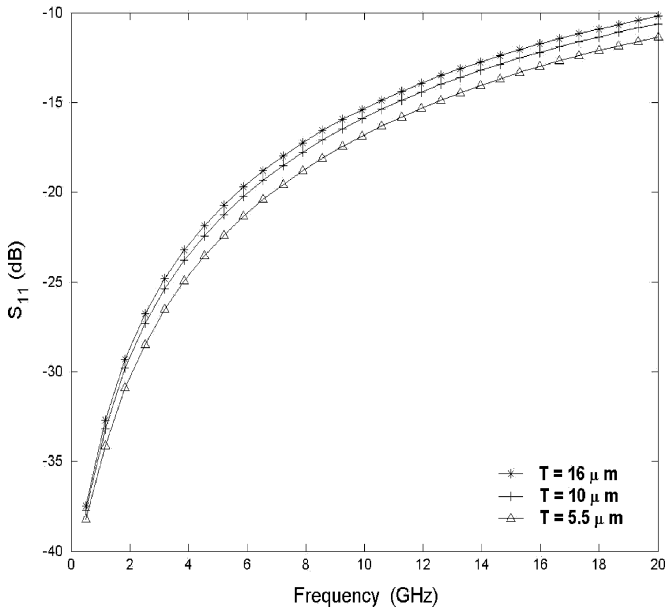

Fig. 8. Comparison of S_{11} with respect to various distances from the substrate.

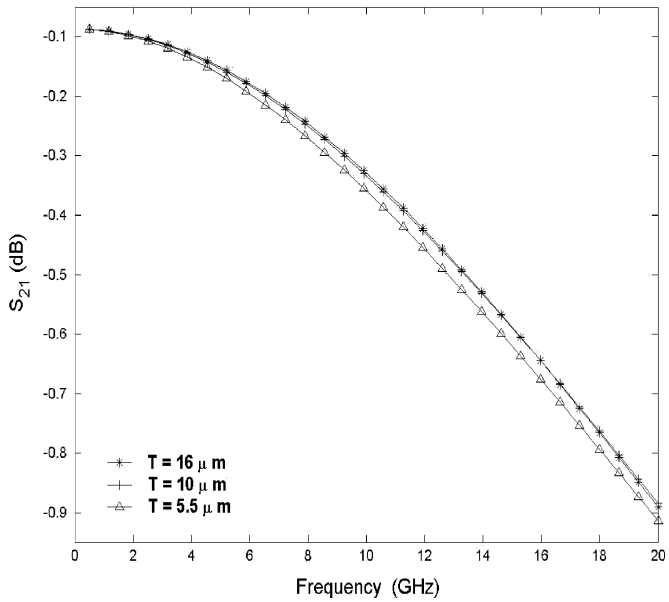

Fig. 9. Comparison of S_{21} with respect to various distances from the substrate.

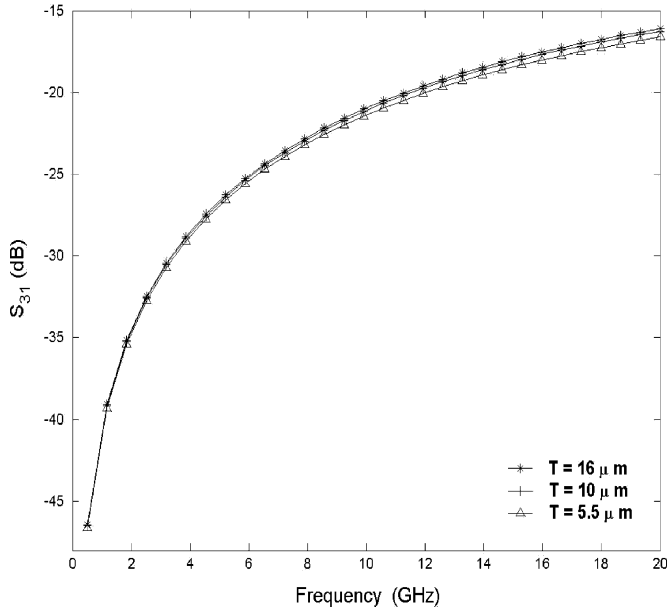

Fig. 10. Comparison of S_{31} with respect to various distances from the substrate.

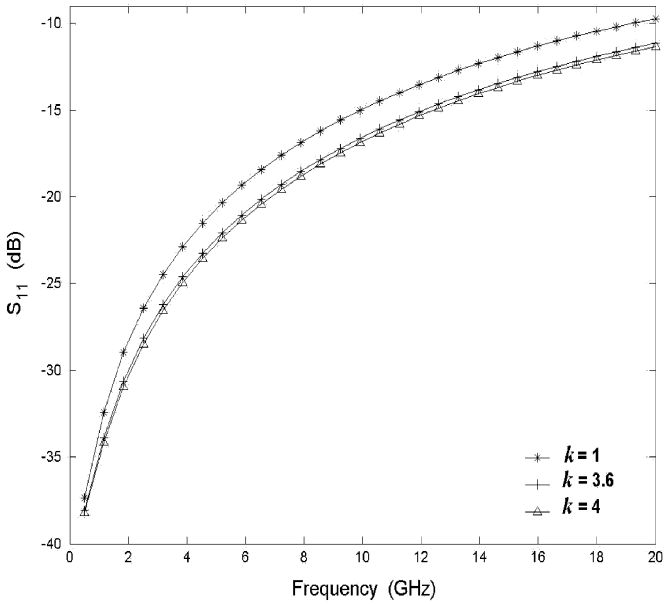

Fig. 12. Comparison of S_{11} with respect to various dielectric permittivities.

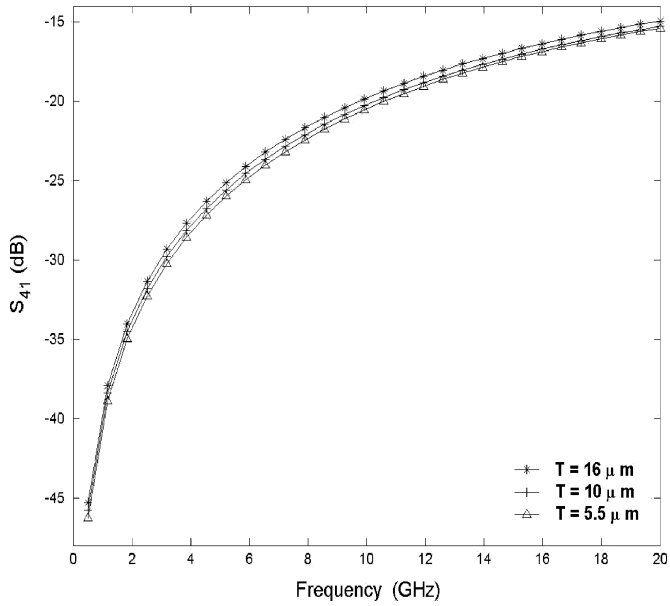

Fig. 11. Comparison of S_{41} with respect to various distances from the substrate.

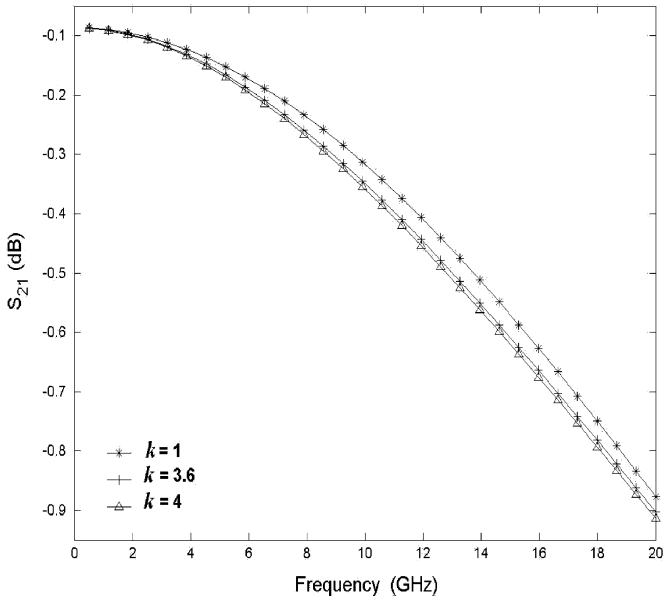

Fig. 13. Comparison of S_{21} with respect to various dielectric permittivities.

For S_{11}, as shown in Fig. 8, both its dependence on the substrate conductivity and the corresponding values are the same as those of the depicted single interconnect in [3]. It indicates that the reflection of the active line is not influenced much by the appearance of the victim line. For S_{21}, the same dependent trend can be noted. However, the corresponding values are smaller than those of the single interconnect in [3]. The reason is that a portion of the input energy has been coupled to the victim line.

Figs. 10 and 11 demonstrate that the coupling is more severe for the interconnects located further from the substrate. As is known, metal layers further away from the substrate are recommended for critical interconnects to reduce the substrate losses. However, it is noticed from our investigation that the thicker dielectric does not bring in merit only, but severer coupling is also caused in the meantime, which downgrades circuit performance.

C. Permittivity of the Dielectric

Recently, numerous low-k materials spanning a wide range of dielectric constants, from air $(k = 1)$ to fluorinated oxides $(k = 3.6)$, have been explored for interconnect systems [12].

The values of 4.0 (parameter of the fabricated structures), 3.6, and 1 are used as the relative permittivity (k) of the dielectric for the simulation. The values correspond to the traditionally used silicon dioxide and novel low-k materials. Corresponding

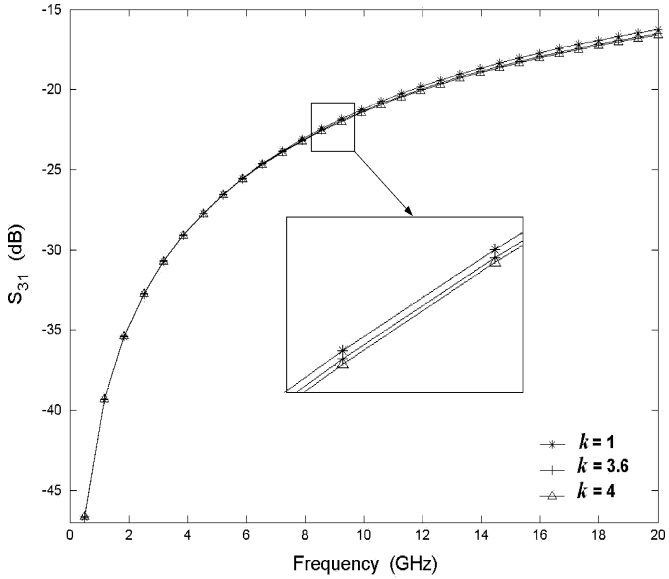

Fig. 14. Comparison of S_{31} with respect to various dielectric permittivities.

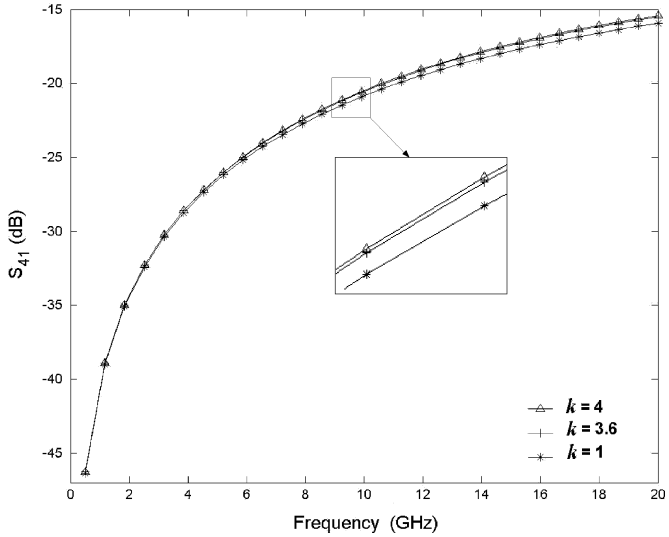

Fig. 15. Comparison of S_{41} with respect to various dielectric permittivities.

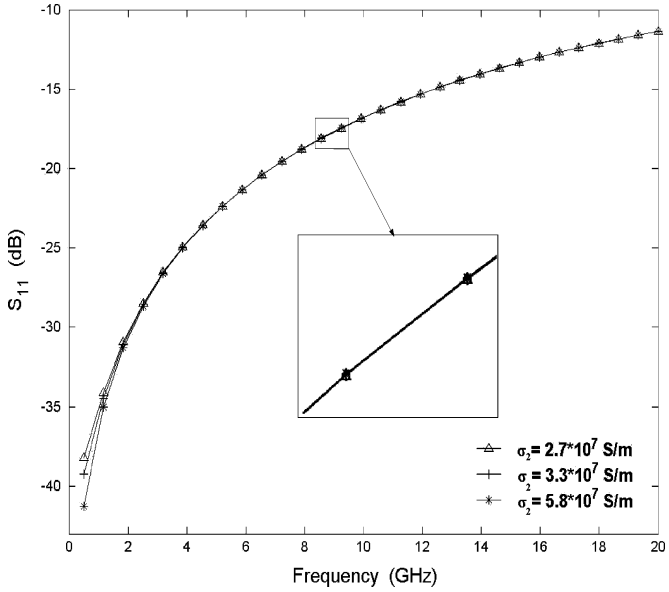

Fig. 16. Comparison of S_{11} with respect to various metallic conductor conductivities.

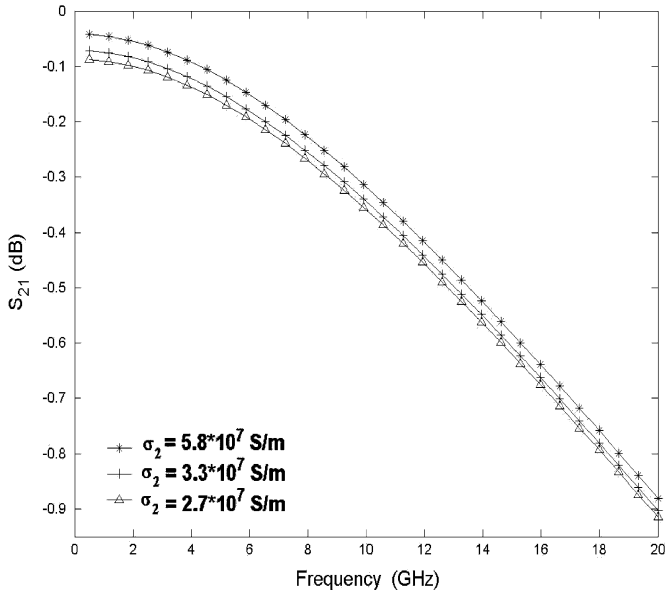

Fig. 17. Comparison of S_{21} with respect to various metallic conductor conductivities.

comparisons of S_{11}–S_{41} are given in Figs. 12–15, respectively. As shown in Figs. 12 and 13, both S_{11} and S_{21} are inversely proportional to the relative permittivity of the dielectric. It follows the same trend as the single interconnect in [3]. From Fig. 15, it can be observed that the interconnect structure with higher dielectric permittivity suffers more near-end crosstalk. As presented in (1), given the same physical dimension (A and d, i.e., the area of each plane electrode and the separation between the electrodes, respectively), the structure with larger dielectric permittivity (k) has larger coupling capacitance. With the same energy in the active line, the larger the coupling capacitance, the greater the coupling capacity. Therefore, the near-end crosstalk is proportional to k:

$$C = \varepsilon_0 \frac{k\mathbf{A}}{d} \tag{1}$$

The far-end crosstalk, as shown in Fig. 14, is inversely proportional to the dielectric permittivity. This can be understood as the crosstalk is affected by both the coupling capacitance and the energy in the active line. Interconnects with larger k have larger coupling capacitances but smaller transmitted energy at the far-end port, which is characterized by S_{21}.

D. Conductivity of the Metallic Conductor

Due to its higher conductivity (σ_2) $(\sim 5.8 \times 10^7$ S/m), copper metallization has been introduced for the aggressive interconnects instead of traditional Al $(\sim 2.7 \times 10^7$ S/m) (used by the fabricated structures) or AlCu $(\sim 3.3 \times 10^7$ S/m) metallization [12].

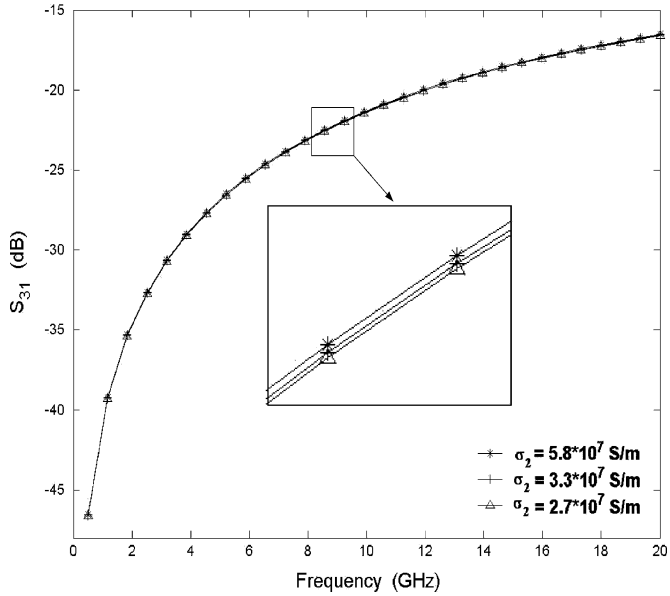

Fig. 18. Comparison of S_{31} with respect to various metallic conductor conductivities.

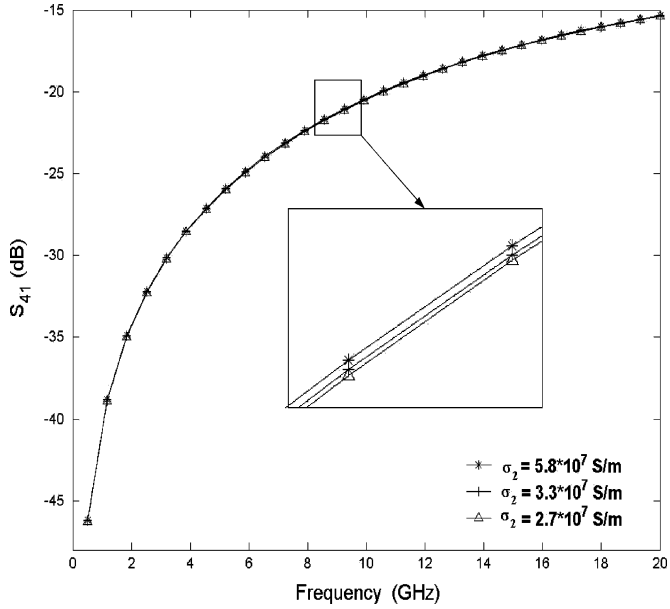

Fig. 19. Comparison of S_{41} with respect to various metallic conductor conductivities.

As shown in Fig. 16, at low frequency, S_{11} is inversely proportional to σ_2. However, when the frequency approaches several gigahertz, the influence of σ_2 on S_{11} becomes negligible. The reason is that at high frequency, the impedance is dominated by the inductance and capacitance instead of resistance. S_{21} in Fig. 17 follows the same trend in [3], while the transmission capacity (S_{21}) is slightly downgraded compared to the single interconnects because of the energy coupling. From Figs. 18 and 19, it is observed that the interconnects with larger conductivity suffer slightly more from coupling than those with lower conductivities. It can be understood that the conductor with higher conductivity has larger currents and hence a larger induced magnetic field and severer coupling. However, at high frequencies, the resistance is not dominant compared with inductance. Therefore, as shown in Figs. 18 and 19, couplings are not strongly affected by the variations in the conductor's conductivities.

IV. Conclusion

The sensitivity of on-wafer coupling interconnects of current and future Si CMOS technologies has been investigated based on the calibrated deck of a 0.18-μm RF CMOS process. With comparisons to the sensitivity study of a single interconnect in [3], it is observed that the reflection (S_{11}) and transmission (S_{21}) of the coupled interconnects follow the same trend when the process parameters (conductivity of the substrate, permittivity of the dielectric, thickness of the dielectric, and conductivity of the metallic conductor) vary. Both the far-end crosstalk (S_{31}) and the near-end crosstalk (S_{41}) are proportional to the conductivity of the conductors and the distance between the conductors and the substrate. It is highlighted that although further distance between the interconnects and the substrate can reduce the effect of substrate losses, severer coupling is caused, which will downgrade the circuit performance. Hence, a tradeoff must be made. As for the dielectric permittivity, S_{31} is inversely proportional to it, while S_{41} has a proportional relationship. The impact of the substrate conductivity is more complicated. No monotonic relationship can be observed.

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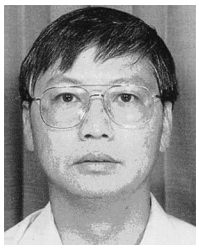
In 1996, he joined the School of Electrical and Electronic Engineering, Nanyang Technological University, as a Lecturer, and became an Assistant Professor and an Associate Professor in 1999 and 2002, respectively. He was appointed as Sub-Dean (Student Affairs) in 2001 and Head of the Department of Circuits and Systems in 2005. He provides consultancy services to statutory boards and multinational corporations in the areas of semiconductor devices and electronic circuit design. He has been extensively involved in the modeling and fabrication of small MOS/bipolar integrated technologies for the last 12 years. His current research interests include the design of new circuits and systems (based on scaled technologies) for low-voltage low-power applications, radio frequency integrated circuit (RFIC) design, integrated circuit design of BiCMOS/CMOS multiple-valued logic circuits, domino logic and memories, and device characterization of deep submicrometer MOSFETs.

Jian-Guo Ma (SM'97) received the B.Sc. and M.Sc. degrees (with honors) in electrical engineering from Lanzhou University, Lanzhou, China, in 1982 and 1988, respectively. He received the Doctoral degree in engineering from Gerhard-Mercator University, Duisburg, Germany, in 1996.

From 1982 to 1991, he was with Lanzhou University, where he worked on RF and microwave engineering. He then joined the Technical University of Nova Scotia, Halifax, NS, Canada. From 1997 to 2005, he was an Associate Professor and a Director of the Center for Integrated Circuits and Systems, Nanyang Technological University, Singapore. Currently, he is with the University of Electronic Science and Technology of China (UESTC), Chengdu, China. His current research interests include RFIC designs for wireless applications, RF characterization and modeling of semiconductor devices, RF interconnects and packaging, SoC, and applications and electromagnetic compatibility/electromagnetic interference (EMC/EMI) in RFICs. He is the author or coauthor of more than 180 technical papers and two books. He is a holder of seven patents in CMOS RFICs.

Dr. Ma is now an Associate Editor for the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.



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