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2009

Pan, R., Yeo, K. S., Do, M. A., Boon, C. C., & Gu, J. M. (2009). A low-voltage fully-integrated CMOS power amplifier for mobile WiMAX subscriber station. In proceedings of the 6th International SoC Design Conference: Busan, Korea, ( pp.21-24).

https://hdl.handle.net/10356/91417

# A Low-Voltage Fully-Integrated CMOS Power Amplifier for Mobile WiMAX Subscriber Station

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*Abstract*—**This paper describes a low-voltage fully-integrated CMOS power amplifier for 3.5 GHz mobile WiMAX (IEEE 802.16 standard) subscriber station application based on Chartered's 0.18 μm IC process. Through simulations using a supply voltage of 1.8 V indicate a capability to deliver a maximum output power of 24 dBm to a 50Ω antenna, with $P_{O1dB}$ of 22.7 dBm corresponding to $P_{I1dB}$ of -1.89 dBm. A power gain of 25.87 dB and a voltage gain of 27 dB can be obtained through a 3-stage cascade configuration, and the power added efficiency (PAE) at $P_{O1dB}$ can achieve almost 24%. In addition, this is the first WiMAX power amplifier that can operate under 1.8 V supply in the literature.**

***Keywords-WiMAX, power amplifier, low voltage, CMOS, fully-integrated.***

## I. INTRODUCTION

The demand for broadband wireless access (BWA) is growing exponentially today. WiMAX, an abbreviation for Worldwide Interoperability for Microwave Access, based upon the IEEE 802.16 standard, is one of the most popular BWA technologies today. Besides the capability of providing high data rate over a wide range, the evolution of utilizing scheduling algorithm in WiMAX's media access control (MAC) layer guarantees the quality of service (QoS) of users' data flow. It is also more bandwidth efficient as compared to today's existing BWA techniques [1]. Ultimately, WiMAX aims to provide high-speed, compatible and interoperable solutions across multiple broad band segments, which makes it a promising candidate for the next generation BWA technique.

Be inspired by the rapidly grow of demand in WiMAX market, the research of WiMAX power amplifiers is growing into a hot zone. Several WiMAX power amplifiers have been published in the literature, but most of them are designed for WiMAX base station while only a few are for subscriber stations, much less in CMOS process [2]-[4]. Besides, the continuing scaling down of CMOS and the conception of power saving set the requirements that the future WiMAX transceivers should be able to operate under low supply. However, none of the published CMOS WiMAX power amplifiers are designed to operate under 1.8 V supply voltage. The impact of scaling down supply voltage includes limited output power, poor linearity and large transistor size which bring new challenges in circuit design, circuit performance and IC layout and fabrication. In addition, to maintain the required output power, reduction in the supply voltage also indicates a higher current density in the devices, resulting in lower PAE.

In this paper, we demonstrate a fully-integrated CMOS power amplifier based on Chartered's 0.18 μm IC process, which is capable of meeting the stringent requirements of mobile WiMAX subscriber station. At a supply voltage of 1.8 V, the proposed power amplifier delivers over 22 dBm output power and 26 dB gain at its 1 dB compression point, with 23.9% PAE. This paper is organized as follows: section II gives the general description of the proposed WiMAX power amplifier, followed by the detailed discussion associated with the design of each stage. In section III, simulation results is released and discussed. Finally, the conclusion is in section IV.

## II. DESIGN OF THE POWER AMPLIFIER

The proposed power amplifier is shown in Fig. 1. It consists of 3 cascade stages, with two driver stages utilizing the conventional cascode configuration to obtain reasonable gain and linearity. For the output stage, common source configuration operating at class AB mode is proposed for both linearity and efficiency consideration. A LRC feedback loop is introduced for stabilizing the output transistors. On-chip capacitors and inductors $Cc_{in}$, $C_{in}$, $L_{in}$ and $C_s$, $L_s$ serve as the input and output matching network.

### *A. Output Stage with LRC Feedback Loop*

The design of the power amplifier includes the output stage and the driver stages. All the devices are optimized to achieve the required WiMAX performance. In addition, the dc bias condition of the transistor, i.e., the operating class and drain efficiency, the output impedance $Z_{out}$ and the input signal amplitude are varied to achieve the required output power. The cascode structure is used for the linear mode power amplifier because its output signal swing can be two or three times the supply voltage. However, it is not suitable for high linearity applications such as WiMAX. Instead, the common source configuration operating at class AB mode is proposed here for high linearity, high efficiency and large gain consideration. The proposed output stage is shown in Fig. 2.

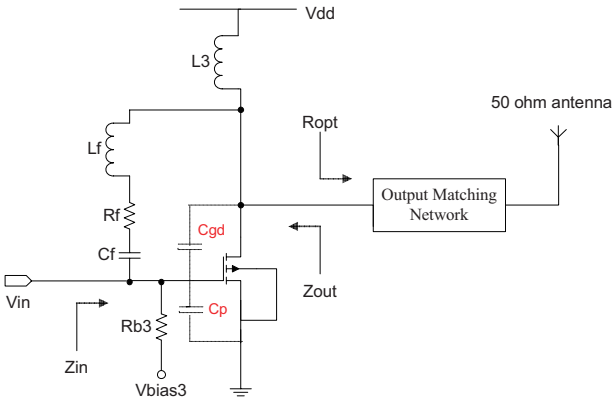


Figure 2. Output stage with a LRC stabilizer.

Stability is always an issue associated with common source configuration, especially when dealing with large output. The large output signal feeds back to the input through the parasitic capacitance $C_{gd}$ and causes instability of the transistor. The stability of output transistors must be guaranteed otherwise the power amplifier may well turn into an oscillator. The stability can be characterized by K (rollett's stability factor) and Δ values, and these S-parameters can be adjusted by tuning the input/output impedance. Unconditional stable ($|\Delta| < 1$ and $K > 1$) must be obtained.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}\cdot S_{21}|} \text{ and } |\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \quad (1)$$

From another point of view, instability can be characterized by a negative real impedance presented at the input of transistor through S-parameter simulation. To solve this problem, a LRC feedback loop is proposed to stabilize the output transistor, with the small signal analysis illustrated in Fig. 3.

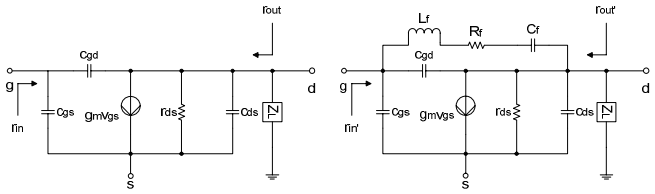


Figure 3. a) Output stage transistor small signal model. b) Output stage transistor small signal model with LRC stabilizer.

Without the LRC stabilizer, the input and output impedance are shown in equation (2) and (3), with $S_{11}$ and $S_{22}$ mainly controlled by the changing the bias condition and transistor size of the output stage, which is undesirable as it will shift the desirable value of $Z_{out}$. By adding the LRC stabilizer, the input/output impedances can be adjusted by tuning the value of $L_f$, $R_f$ and $C_f$, as shown in equation (4) and (5), thus achieves the purpose of stabilizing the output transistor.

$$\gamma_{in} = \frac{j\omega(C_{gd}+C_{ds})+\left(\frac{1}{r_{ds}}+\frac{1}{Z_L}\right)}{-\omega^2[C_{gd}(g_m+C_{gs}+C_{gd})+C_{gs}C_{ds}]+j\omega(C_{gd}+C_{gs})(\frac{1}{r_{ds}}+\frac{1}{Z_L})} \quad (2)$$

$$\gamma_{out} = [\frac{1}{r_{ds}} + \frac{1}{Z_L} + j\omega(C_{gd} + C_{ds})]^{-1} \quad (3)$$

$$\gamma'_{in} \cong \frac{1+\left(R_f+j\omega L_f+\frac{1}{j\omega C_f}\right)[j\omega(C_{gd}+C_{ds})+\frac{1}{r_{ds}}+\frac{1}{Z_L}]}{j\omega C_{ds}+\frac{1}{r_{ds}}+\frac{1}{Z_L}+g_m} \quad (4)$$

$$\gamma'_{out} = [\frac{1}{r_{ds}} + \frac{1}{Z_L} + j\omega(C_{gd} + C_{ds}) + \frac{1}{R_f+j\omega L_f+\frac{1}{j\omega C_f}}]^{-1} \quad (5)$$

### *B. Determination of the Optimal Load $R_{opt}$*

For a given transistor size, there is an optimal load impedance $R_{opt}$ at which the output power hits a peak. In other words, maximum power can be delivered to $R_{opt}$ when $R_{opt}$ equals to the complex conjugate of the output impedance $Z_{out}$. $Z_{out}$ is mainly a function of the output transistor size, the gate

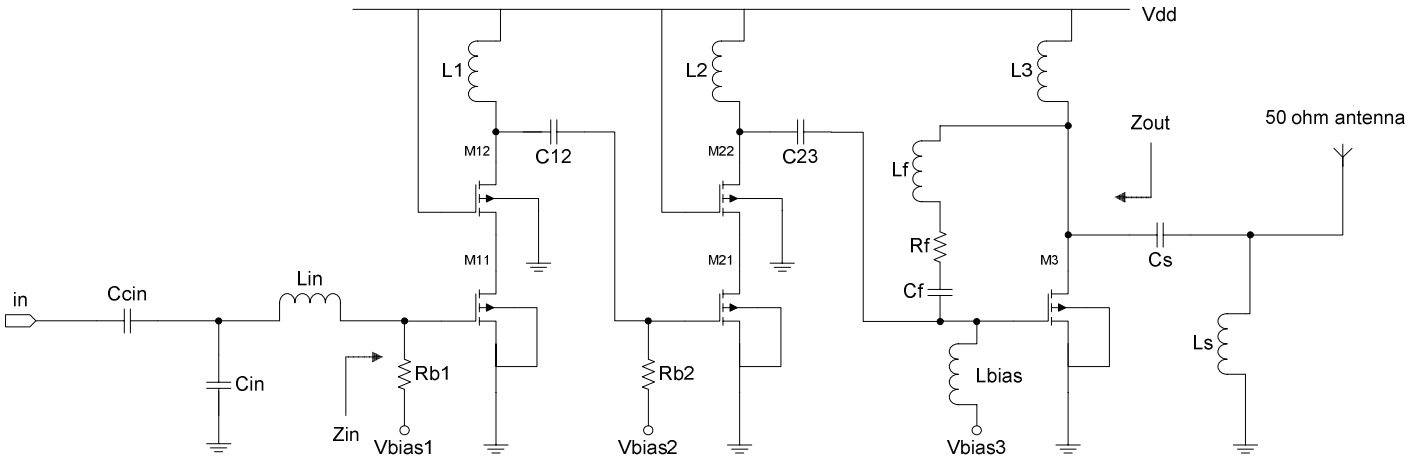


Figure 1. Full schematic of the proposed WiMAX power amplifier.

bias and the input signal amplitude, as well as factors that bring the same effects on $R_{opt}$, as expected in Fig. 4 and Fig. 5. In Fig. 4, a larger input signal level results in a higher $P_{av,\,max}$, but at the same time reduces the value of $R_{opt}$ where $P_{av,\,max}$ hits its peak. The shift in peak $P_{av,\,max}$ can be caused by output transistor size too. Specifically, a large device size gives a small $R_{opt}$. Also, in small devices, the maximum $P_{av,\,max}$ increases proportionally with the size of output device initially, reaches a peak value and starts decreasing as the device size increases further. Thus, with this finding, there exists an optimal size of the output transistor that can give both high power and high efficiency.

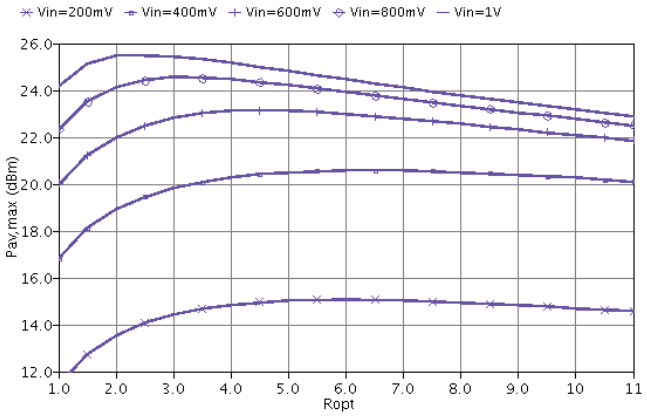


Figure 4. Plotted $P_{av,\,max}$ VS $R_{opt}$ under different input signal amplitudes.

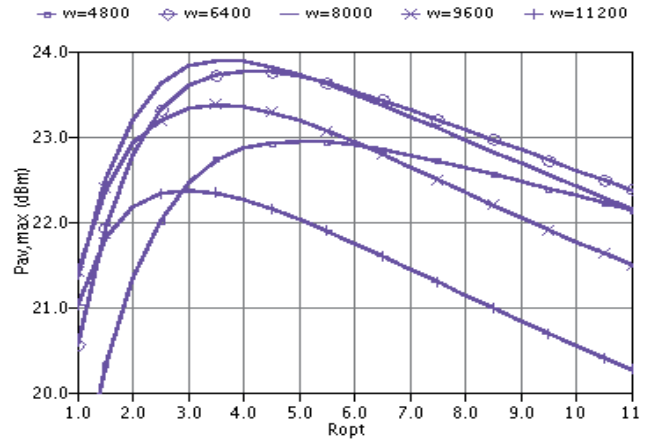


Figure 5. Plotted $P_{av,\,max}$ VS $R_{opt}$ under different device size.

To design a power amplifier under a low supply voltage is very challenging. As the supply voltage reduces, and in order to maintain the same output power level, the impedance $R_{opt}$ at the output must be reduced by the square value of the supply reduction. The optimal load $R_{opt}$ should be well designed to meet the required output power and it can be calculated from equation (6).

$$P_{av,max} = \frac{V_{pk}^2}{2R_{opt}} \tag{6}$$

$P_{av,\,max}$ is the maximum power available at output of the output stage, and $V_{pk}$ is the voltage swing at the output of output transistor which equals to the supply voltage for linear mode power amplifier. Theoretically, a low $R_{opt}$ is desirable to give a higher output power. However, this is not practical for a fully integrated CMOS design. Since a low $R_{opt}$ requests a very large size of output transistor, which results in a large capacitive load presented to the driver stage. This brings problems in the circuit layout. Furthermore, there are issues in the design of the output matching network to match a low $R_{opt}$ to the 50 Ω antenna, as it requires a very small inductance value. Obviously, the minimum inductance that can be placed on-chip becomes the limiting factor for the output matching network. In addition, a low $R_{opt}$ also indicates a large current flowing in the output matching network, thus increase the loss and pull down the efficiency.

To calculate $R_{opt}$, assume i) the maximum power $P_{max}$ can be delivered to the antenna is 23 dBm (0.2 Watt). ii) 20% power loss in the output matching network. iii) 0.1~0.2 V voltage drop on $L_3$. The maximum power available from the output stage $P_{av,\,max}$ and the optimal load $R_{opt}$ can be calculated in equation (7) and (8).

$$P_{av,max} = \frac{P_{max}}{(1-20\%)} = \frac{0.2\text{W}}{80\%} = 0.25\ \text{W} \cong 24\ \text{dBm} \tag{7}$$

$$R_{opt} = \frac{V_{pk}^2}{2\times P_{av,max}} = \frac{(1.6\sim1.7\ \text{V})^2}{2\times 0.25\ \text{W}} = 5\sim6\ \Omega \tag{8}$$

Note that the output stage will be working around its 1 dB compression point instead of its maximum power point, and $R_{opt}$ will be shifted to a larger value due to reduced input signal amplitude. Thus the transistor size and dc bias should be chosen when 24 dBm power can be delivered to $R_{opt}$ peaks around 3~5Ω. From Fig. 4 and Fig. 5, we can conclude that the optimal device size is around 8000$\mu m$ and an input signal swing of 0.6~0.8 V should be enough to drive the output stage in order to achieve the required power level. A further increase in the driving signal level does not increase the output power but only lead to reduce the overall PAE.

### *C. Design of Driver Stages*

The design specification of the second driver is set by the input requirements of the output stage. Similarly, the design specification of the first driver is set by the second driver stage. Since the linearity requests for these two stages are not as stringent as the output stage, the input transistors are designed to operate in deep class AB mode, which is also for the consideration of high efficiency. To reduce the large capacitive loading, on-chip inductor $L_{bias3}$ is used to resonate with $C_{gs}$.

## III. SIMULATION RESULTS

The new power amplifier is designed using Chartered's 0.18 µm IC process. The simulation is conducted using Cadence and based on the device models provided by the foundry. This power amplifier operates at 1.8V voltage supply. Fig. 6 shows the results for small signal S-parameter simulation. Good matching can be obtained from 3.4 GHz to 3.6 GHz, with unconditional stable from 1 GHz to 6 GHz. A small signal voltage gain $S_{21}$ of over 25 dB with power gain $G_P$, transducer gain $G_T$ and available gain $G_A$ overlapped around 25 dB is observed over the interested frequency band.

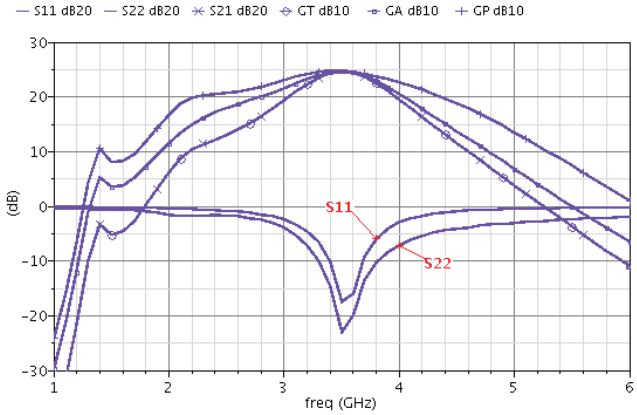


Figure 6. Results for small signal S-parameter simulation.

Fig. 7 shows the output power and PAE versus the input power. An output 1 dB compression $P_{O1dB}$ of 22.7 dBm is observed at $P_{I1dB}$ equals to -1.89 dBm, with 23.92% PAE. The input and output voltage waveform at $P_{O1dB}$ is shown in Fig. 8. The performance of the power amplifier is summarized in Table I.

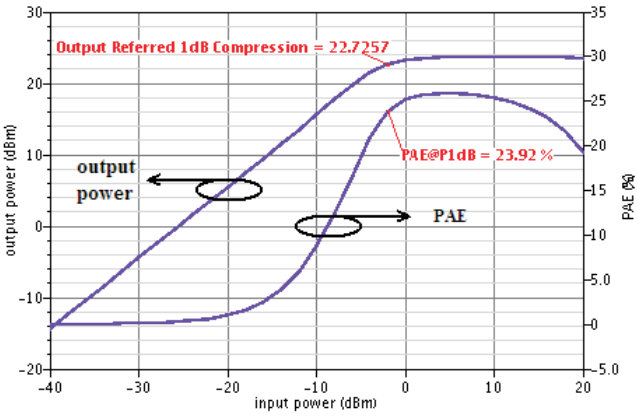


Figure 7. Output power and PAE VS input power.

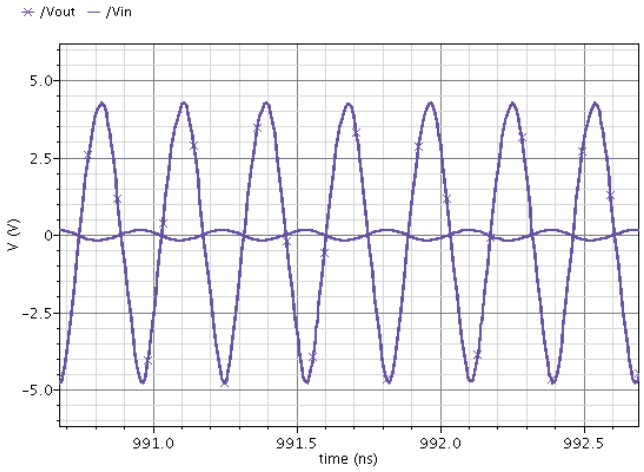


Figure 8. Input and output voltage @ $P_{1\,dB}$.

TABLE I. PERFORMANCE OF PROPOSED DESIGN.

| | **This work** |
|---|---|
| **technology** | Chartered's 0.18um IC |
| **application frequency (GHz)** | 3.5 |
| **bandwidth (MHz)** | 200 |
| **supply voltage (V)** | 1.8 |
| **architecture** | 3-stage cascade, fully-integrated |
| **maximum output power (dBm)** | 24 |
| **output power @ $P_{I1dB}$ (dBm)** | 22.7 |
| **power gain (dB)** | 25.87 |
| **voltage gain (dB)** | 27 |
| **PAE @ $P_{I1dB}$ (%)** | 23.92 |
| **power consumption @ $P_{I1dB}$ (W)** | 0.786 |

## IV. CONCLUSION

The design and analysis of a low-voltage fully-integrated CMOS power amplifier has been presented. The simulation results show that it is suitable for 3.5 GHz mobile WiMAX subscriber station application. The proposed design offers a voltage gain of 27 dB, a power gain of 25.87 dB and $P_{O1dB}$ of 22.7 dBm with 23.9% PAE at 1.8 V supply. This is the first WiMAX power amplifier that can operate under a 1.8 V power supply voltage in the literature.

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