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A Differential CMOS T/R Switch for Multistandard Applications

Y. P. Zhang, Qiang Li, *Student Member, IEEE*, Wei Fan, Chew Hoe Ang, and He Li

Abstract—This brief presents a differential transmit–receive (T/R) switch integrated in a 0.18- μm standard CMOS technology for wireless applications up to 6 GHz. This switch design employs fully differential architecture to accommodate the design challenge of differential transceivers and improve the linearity performance. It exhibits less than 2-dB insertion loss, higher than 15-dB isolation, in a $60\ \mu\text{m} \times 40\ \mu\text{m}$ area. 15-dBm power at 1-dB compression point ($P_{1\text{dB}}$) is achieved without using additional techniques to enhance the linearity. This switch is suitable for differential transceiver front-ends with a moderate power level. To the best of the authors' knowledge, this is the first reported differential T/R switch in CMOS for multistandard and wideband wireless applications.

Index Terms—CMOS integrated circuits, differential switches, microwave switches, MOSFET switches, transmit–receive (T/R) switch.

I. INTRODUCTION

WITH THE development of modern silicon technology, more and more high-frequency circuits can be implemented in standard CMOS processes. Radio-frequency (RF) integrated circuits (ICs) in standard CMOS technology have proven feasible [1] and the trend of system-on-chip (SoC) requires further integration of the transmit–receive (T/R) antenna switch.

For years, the RF switch has been dominated by discrete components using PIN diodes and III-V MESFETs. Recently, CMOS T/R switch design has been explored to a certain extent. The effect of substrate resistance on the insertion loss is studied in [2] and [3], where low insertion loss was obtained by minimizing the substrate resistance and dc biasing the T/R nodes. A high isolation was achieved using CMOS silicon-on-insulator (SOI) technology [4]. In both cases, however, the linearity was limited due to the parasitic capacitance and source/drain junction diodes. An asymmetric design of the T/R switch is reported using an LC-tuned substrate bias to enhance the power handling capability [5], where the transmit path and the receive path are considered separately. A 28-dBm power 1-dB compression point ($P_{1\text{dB}}$) in the transmit mode was obtained. The disadvantages of this asymmetric approach are the design complexity and large silicon area consumed.

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Fig. 1. Architecture of the proposed differential T/R switch.

A differential T/R switch designed in commercial CMOS technology has not been reported to date. Comparing with single-ended architecture, the differential nature permits higher linearity and lower offset and makes it immune to power supply variations and substrate noise. Therefore, differential architecture is normally preferred in applications requiring higher signal quality. Exploring the design of integrated differential T/R switch is essential for transceiver front-ends with fully differential architecture.

In this brief, the design and implementation of differential T/R switches are explored. Design issues on the transistor sizing, crosscoupling, and matching are considered. A fully differential T/R switch is demonstrated in a 0.18- μm standard CMOS technology. Measurement results exhibit less than 2-dB insertion loss and higher than 15-dB isolation. The 15-dBm $P_{1\text{dB}}$ is achieved without using additional techniques to enhance the linearity. The silicon area occupied is only $60\ \mu\text{m} \times 40\ \mu\text{m}$. These results show that the proposed switch is suitable for multistandard and broadband wireless front-ends with moderate power levels.

II. ARCHITECTURE AND CONSIDERATIONS

A. Architecture

The schematic of the proposed differential T/R switch is shown in Fig. 1. Transistors M1, M2, M3, and M4 perform the main switching function. A high control voltage V_{ctrl} turns M1 and M3 on, which enables the differential path between the antenna and receiver. Similarly, the differential transmit path is turned on when the control voltage is low. The control voltage is biased through a resistance R_G to reduce the effect due to capacitive coupling around the gate of the OFF transistors [4].

Fig. 2. Small-signal equivalent circuit of a MOS transistor switch.

The differential nature results in an improved power handling capability comparing with single-ended configurations. From the power point of view, a differential output scheme is able to handle twice the single-ended output power, that is, 3-dB higher $P_{1\text{dB}}$ could be achieved in the proposed differential switch. As the power handling capability is the bottleneck of CMOS T/R switches, differential architecture is of great advantage in current silicon technology.

B. Design Considerations

Theoretically, transistor sizing in differential T/R switches is the same with that in single-ended switches. In the case where the MOS transistor is turned ON, the equivalent circuit is shown in Fig. 2 [2]. R_{ON} is the on-resistance of the transistor which is operating in the linear region. At low frequencies, the insertion loss is determined by R_{ON} . R_B is the substrate resistance. C_{DB} , C_{SB} , C_{GB} , C_{GS} , and C_{GD} are parasitic capacitances of the transistor. The parameters are eventually frequency-dependent. The capacitive coupling effect increases with the increase of operating frequency, resulting in the increase of the power loss on the substrate resistance R_B .

The insertion loss can be calculated as

$$\begin{aligned} \text{IL} &= \frac{\text{Power Available from Source}}{\text{Power Delivered to Load}} \\ &= \frac{P_{\text{AVS}}}{P_L} \\ &= \frac{1}{|S_{21}|^2} \\ &= \frac{\omega^2 C_T^2 [(R_{ON} + 2Z_0)R_B + (R_{ON} + 2Z_0)Z_0]^2}{(2Z_0)^2 (1 + \omega^2 C_T^2 R_B^2)} \\ &\quad + \frac{(R_{ON} + 2Z_0)^2}{(2Z_0)^2 (1 + \omega^2 C_T^2 R_B^2)} \end{aligned} \quad (1)$$

where Z_0 is the characteristic impedance the source and load are terminated with. ω is the operating radian frequency. The total effective parasitic capacitance C_T makes the insertion loss frequency-dependent. The first term in (1) increases as frequency increases, which can be minimized by optimizing the values of R_B and R_{ON} . Previous research shows that low substrate resistance is preferred in the high-frequency switch design [3]. The second term in (1) is actually the intrinsic insertion loss in dc due to the on-resistance R_{ON} of the transistor, which decreases as frequency increases. This term can also be minimized by minimizing R_{ON} . In the linear/triode region, R_{ON} can be expressed as [6]

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})}. \quad (2)$$

Thus, the second term in (1) can be minimized by increasing the W/L ratio of the switch transistors, where tradeoff occurs since a large transistor leads to a large parasitics, resulting in a large C_T , and, thus, the frequency-dependent first term in (1) will be increased. An optimal W/L ratio exists to minimize the insertion loss.

When the MOS transistor is turned OFF, the undesired signal couples from drain–source path and substrate parasitics. The isolation of a T/R switch severely depends on technology [4]. In a bulk CMOS process, the isolation is determined by the parasitics around the drain and source [7]; increasing of the gate width leads to the degradation of isolation performance. Previous research [7] and simulation show the trend is monotonous; transistor size can be optimized to provide the minimum insertion loss while maintaining a reasonable isolation.

The linearity, or power handling capability, is directly related to the bias condition of the MOS transistors. A large signal at the drain/source may cause the junction diodes forward biased and clip the signal. The unintentional turn-on of the OFF transistors can also distort the signal. As a result, the dc bias of the TX/RX nodes affects the linearity significantly [2]–[4]. High dc bias and high control voltage are often used in the CMOS T/R switch for better linearity. However, the reliability problems may exist potentially with a large gate–source voltage. In this design, the differential architecture is employed that improves the linearity fundamentally rather than overstress the CMOS transistors, the control voltage is provided by the build-in inverter with a 1.8-V standard supply voltage.

Shunt transistors are commonly used to improve the isolation [2]–[4], [7], which provides a low-impedance path for the undesired signal to the RF ground. However, the additional transistors increase the possibility of unintentional turn-on and thus degrades the linearity. Considering the stringent voltage limitation that gives little space to safely bias the shunt transistors, they are not used in this design. Therefore, the total number of components in this differential switch is exactly equal to that of the single-end switch, but the linearity or voltage requirement is expected to be better. The price is that isolation performance will be degraded without shunt transistors.

Note that, in (2), R_{ON} can also be reduced simply by increasing the term $V_{GS} - V_{th}$ with the transistor size unchanged, which improves the insertion loss intuitively. In fact, the performance of the T/R switch depends significantly on the working condition. Assuming that the TX/RX nodes are biased at 0.8 V, and control voltage is 1.8/0 V, numerical calculation shows a $105 \mu\text{m}/0.18 \mu\text{m}$ transistor should be chosen to achieve the lowest insertion loss at 4 GHz. In this design, however, $100 \mu\text{m}/0.18 \mu\text{m}$ is used due to the scale limit of RF CMOS transistors provided by the foundry.

R_{G1} – R_{G4} should be chosen sufficiently large to create a floating-gate terminal at RF. Considering that a large bias resistance will lower the switch speed, 3.9-k Ω bias resistance is chosen. The values of the circuit elements used in this design are given in Table I.

C. Layout Considerations

Practical problems in the single-ended T/R switch include substrate resistance, source/drain parasitics, dc biasing, and

TABLE I
CIRCUIT ELEMENT VALUES

Circuit element	Value
NMOS: $M1 - M4$	$100\mu\text{m}/0.18\mu\text{m}$
PMOS in Inverter	$100\mu\text{m}/0.18\mu\text{m}$
NMOS in Inverter	$100\mu\text{m}/0.18\mu\text{m}$
$R_{G1} - R_{G4}$	$3.9\text{ k}\Omega$

Fig. 3. Layout of the proposed differential T/R switch.

transistor sizing [2], [4], [5]. In differential T/R switch design, issues on cross coupling and transistor matching between the two signal paths should also be considered carefully. A tradeoff exists among these issues, e.g., good matching of transistors requires a close placement, whereas crosstalk increases when transistors are placed near to others.

Choosing the layout strategy depends on the application and system requirement. In general, crosstalk and coupling increase the nonlinearity in the circuits, resulting in degradation on the insertion loss performance and power handling capability. On the other hand, mismatch is a signal-independent process, which does not produce other signal-dependent problems as cross coupling does, e.g., cross coupling may affect dc biasing conditions. Therefore, considerations are focused on reducing the effect of cross coupling at the price of matching degradation.

Fig. 3 is the layout of the differential T/R switch. The matching transistors in the same signal path (e.g., M1 and M3, M2 and M4) are placed together without special arrangement (e.g., interdigitize) to improve the matching. The transistors in different ON/OFF status are placed far away to avoid cross coupling. In addition, substrate contacts are placed densely to reduce the substrate resistance R_B .

III. MEASUREMENT RESULTS AND DISCUSSIONS

The differential switch is fabricated in a 1.8-V one-poly six-metal $0.18\text{-}\mu\text{m}$ standard CMOS technology. The active area of the switch is $60\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$. Fig. 4 is the die photograph of the fabricated switch. Four GSSG pads were designed for on-chip measurement purpose. All measurement at I/O pads were carried out using Cascade Microtech's $100\text{-}\mu\text{m}$ differential GSSG probes. A four-port network analyzer was used in the experiment, which avoids the complicated on-chip balun design for testability. The control voltage is 1.8/0 V and the TX/RX nodes

Fig. 4. Die photograph of the fabricated differential T/R switch.

Fig. 5. Measured insertion loss and isolation parameters for the differential-mode small signals.

are biased at 0.8 V. Note that the differential impedance at each port is $100\text{ }\Omega$, and the common-mode impedance is $25\text{ }\Omega$.

In the differential T/R switch circuits, performances need to consider include not only the differential-mode parameters, but also common-mode parameters and common-mode rejection performance.

A. Differential-Mode Performance

Consider only the small differential signal applied to each port; the insertion loss and isolation are shown in Fig. 5. An extremely low insertion loss of 0.53 dB is obtained at 0.9 GHz. In the frequency range up to 2.5 GHz, the insertion loss is lower than 0.8 dB. Insertion losses of 0.72 and 0.79 dB are obtained at 1.8 and 2.4 GHz, respectively. At 5.2 GHz, the insertion loss is 1.7 dB. The results obtained indicate that ON-resistance R_{ON} of the switch transistor is extremely small with a large W/L ratio, whereas C_T is increased, and the frequency-dependent component in (1) has an obvious effect on the insertion loss

Fig. 6. Measured insertion loss and isolation parameters for the common-mode small signals.

when the operating frequency is increased. The isolation at 0.9, 1.8, 2.4, and 5.2 GHz are 30, 23, 20, and 16 dB, respectively.

In the frequency range from 40 MHz up to 6 GHz, the differential-mode insertion loss is within 2 dB and differential-mode isolation is above 15 dB. Although in the differential case cross coupling and mismatch further degrade the insertion loss and isolation, these results are comparable with other single-ended CMOS T/R switches [3], [5].

B. Common-Mode Performance

Fig. 6 shows the common-mode insertion loss and isolation parameters. This is obtained by applying common-mode small signals to each port. Comparing with the differential-mode performance, both insertion loss and isolation are degraded at high frequencies. Insertion losses of 0.83, 1.1, 1.3, and 3.3 dB and isolation of 28, 22, 20, and 14 dB are obtained at 0.9, 1.8, 2.4, and 5.2 GHz, respectively. This is reasonable since the common-mode signal with the same amplitude and phase result in a more severe cross coupling between the two signal paths. However, the common-mode signal is not of the same importance as the differential signal which affects the signal quality fatally, and thus a slightly inferior performance in the common mode is sustainable.

C. Common-Mode Rejection

The common-mode rejection ratio (CMRR) is measured by the forward transmission coefficient from the transmitted common-mode signal to the received differential-mode signal. Obviously, the CMRR is related to the ON-OFF conditions of the differential switch. In the ON and OFF states, the CMRR are shown in Fig. 7. It is clear that CMRR is almost constant when the switch is ON and varies significantly when the switch is OFF. CMRRs of 28, 27, 27, and 27 dB in the ON-state and CMRRs of 53, 45, 42, and 33 dB in the OFF-state are obtained at 0.9, 1.8, 2.4, and 5.2 GHz, respectively. In the OFF state, the CMRR is much higher, which is actually part of the isolation parameters.

D. Power Handling Capability

The linearity of the switch determines the maximum power it can handle. A power compression point of 1 dB ($P_{1\text{dB}}$) is

Fig. 7. Measured common-mode rejection ratio in the ON and OFF states of the differential T/R switch.

Fig. 8. Linearity of the differential T/R switch at 5.2 GHz. The control voltage is 1.8/0 V, and the TX/RX nodes are biased at 0.8 V.

Fig. 9. Linearity of the differential T/R switch at different frequencies. The TX/RX nodes are biased at 0.8 V with 1.8/0-V control voltage and 1.6 V with 3.6/0-V control voltage.

used to measure the linearity. Since the switch is fully symmetric, the linearity in the transmitted mode and receive mode is identical. Fig. 8 shows the large-signal result at 5.2 GHz. A 15.2-dBm $P_{1\text{dB}}$ is obtained. As mentioned above, the differential switch should have 3-dB higher $P_{1\text{dB}}$ than the single-ended switch in theory. This is proved by other single-ended CMOS T/R switches where a maximum of 11–12-dBm power handling are reported without tuning the substrate bias [2], [4], [7]. In the case that reliability is not a big concern, higher control voltages can be used and the resultant $P_{1\text{dB}}$ is about 17–18 dBm [2], [3]. Under similar condition where 3.6/0-V V_{ctrl} and 1.6-V

TABLE II
SUMMARY OF DIFFERENTIAL SWITCH PERFORMANCE

Specifications		This work				[2]	[5] (T/R)		[7]	[3] (H/L R_B)
		0.9-GHz	1.8-GHz	2.4-GHz	5.2-GHz	900-MHz	2.4-GHz	5.2-GHz	2.4-GHz	5.8-GHz
Insertion Loss (dB)	DM *	0.53	0.72	0.79	1.7	0.7	1.5/1.6	1.5/1.4	1.5	1.0/0.8
	CM *	0.83	1.1	1.3	3.3					
Isolation (dB)	DM *	30	23	20	16	42	32/17	30/15	24	29/27
	CM *	28	22	20	14					
CMRR (dB)	ON	28	27	27	27	—	—	—	—	—
	OFF	53	45	42	33					
P_{1dB} (dBm)	HV †	19	20	20	20	17	—	—	—	18/17
	NV ‡	14	15	15	15	11.5	28.5/12.5	28/11.5	11 ‡	—

* DM—Differential Mode, CM—Common Mode.

† HV—High DC bias and control voltage, NV—Normal DC bias and control voltage.

‡ 0.2-dB gain compression point ($P_{-0.2dB}$).

drain/source bias are used, 20-dBm P_{1dB} is obtained for this differential switch.

The P_{1dB} obtained at different frequencies up to 6 GHz are shown in Fig. 9. At frequencies of 0.9, 1.8, 2.4, and 5.2 GHz, the P_{1dB} 's obtained are 14, 15, 15, and 15 dBm, respectively. With 3.6/0-V V_{ctrl} and 1.6-V drain/source bias, the P_{1dB} 's are 19, 20, 20, and 20 dBm, respectively. The result shown here provides a possible design flexibility on the power handling and reliability.

Table II shows a summary of the measured performance of the differential T/R switch at 0.9, 1.8, 2.4, and 5.2 GHz, which are the most widely used bands by current wireless systems. These results show that the proposed switch is suitable for a wide range of wireless applications with moderate peak power levels.

IV. CONCLUSION

The feasibility of a differential T/R switch in CMOS is demonstrated, which improves the power handling capability without performance degradation of insertion loss and isolation. A fully differential T/R switch has been implemented in a 0.18- μ m standard CMOS technology. The designed consideration of the differential switch is discussed. Measurement results exhibit less than 2-dB insertion loss and higher than 15-dB isolation with reasonable common-mode rejection performance at frequencies up to 6 GHz. A 15-dBm power 1-dB compression point is obtained which is theoretically 3 dB superior to the single-end switches. Effects of cross coupling and mismatch can be reduced by careful layout. The broadband

characteristics make it suitable for multistandard and wideband wireless applications with moderate power levels.

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