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2007

Yu, X. P., Do, M. A., Ma, J., Lim, W. M., Yeo, K. S., & Yan, X. L. (2007). Sub-1 V low power wide range injection-locked frequency divider. *IEEE Microwave and Wireless Components Letters*, 17(7), 528-530.

<https://hdl.handle.net/10356/91513>

<https://doi.org/10.1109/LMWC.2007.899318>

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Sub-1 V Low Power Wide Range Injection-Locked Frequency Divider

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Abstract—In this letter, the sub-1 V low power, wide range operation of an injection-locked frequency divider with a common-gate configuration is presented. The performances in terms of locking range and power consumption have been improved in the sub-1 V low supply voltage. Two set of prototypes, performing divide-by-2 and divide-by-3, have been fabricated in CSM 0.18 μm CMOS process to verify the proposed designs. In the proposed units, a locking range of 40% has been achieved with a power consumption of 0.24 mW in the 0.8 V supply voltage. The operating range of 2.2 GHz to 5.2 GHz has been achieved with a power consumption of 1.1 mW for a 1.5 V supply voltage.

Index Terms—Frequency divider (FD), frequency synthesizer, injection lock (IL), phase-locked loops (PLLs), wireless local area network (WLAN).

I. INTRODUCTION

PHASE-locked loops (PLLs) are widely used in modern wireless communication systems. The crucial components in the PLL are the voltage-controlled oscillator (VCO) and the high frequency dividers (FDs). The challenges of the frequency divider design are the power consumption and the operating speed. The CMOS high-speed FDs are usually implemented with the MOS current mode logic (MCML) [1]. However, the MCML has a large dc power dissipation. Injection-locked frequency dividers (ILFDs) have the merit of high operating frequency and low power consumption [2]–[6]. However, such a low power consumption is obtained at the expense of a narrow locking range. Moreover, the operating range of the ILFD is highly dependent on many factors, e.g., supply voltage, injection power and resonance frequency of the frequency selective block. As the input frequency increases, the output frequency of the ILFD will be locked in the high order superharmonics of the input frequency. Based on this operation, there have been claims of high frequency wide band operation [2], [5]. However, the reported highest operating frequency is based on higher order superharmonics. The operating range of the ILFD can not be precisely controlled and the output power is decreased with the increase of division ratio since the power is concentrated on the fundamental harmonic. As a result, although most wireless communication systems operate over a narrow band, ILFDs are still

not widely used in modern communications system. There are few reports on the operation of the ILFDs in a full frequency synthesizer [3]. In this letter, a common-gate (CG) configuration input for the ILFD is proposed. Compared with conventional common-source (CS) implementation, it exhibits a larger locking range under a low supply voltage.

II. DESIGN CONSIDERATIONS OF THE ILFD

The design considerations of the ILFD includes the operating frequency, power consumption and locking range. The operating frequency of the ILFD is set by the speed of the injector and the frequency selective block. The frequency selective block is usually based on an oscillator (band-pass filter) and is the major bottleneck of this approach. To achieve high operating frequencies for the ILFD, an LC cross-coupled oscillator or a ring oscillator with an inductor load is usually used as the frequency selective block [4]. However, the implementation of the inductor requires a large silicon area. Moreover, the LC tank based ILFD has a narrow locking range. For a lower operating frequency, the inductor-less CMOS ring oscillator is commonly used since the operating frequency is higher than that of the conventional digital FD [2], [3]. Moreover, it has a wider locking range compared with the LC tank based ILFD. In most major wireless standards, the operating frequencies are below 6 GHz, the single-ended ILFD can meet the speed requirement and the power consumption is lower than that of the digital FD. And the single-ended logic with large output swing can be easily integrated to the VLSI system. Therefore, the ring oscillator based ILFD is preferred for wide range WLAN applications.

III. PROPOSED DESIGNS

The major difficulty of the existing ring oscillator based ILFD designs is to achieve a large locking range with a lower power consumption. To reduce the power consumption, two MOS transistors cascoded topology is used in [7]. The mixing of signals is carried out by introducing a parallel MOS as a switch. However, it introduces a shift of dc voltages between the two stages. Therefore, careful transistor sizing is needed [7]. Moreover, similar to the varactor tuning in [3], an extra biasing voltage (for the PMOS load) is needed to obtain large locking range. The optimization of input stage is also important to improve the performance of the ILFD. For example, power matching is used to improve the locking range of the ILFD [8].

The input stage of an ILFD conventionally uses a CS input, even if both CS and CG configurations are widely used in the design of amplifiers[9]. The CS input is usually used as a gain

Manuscript received January 7, 2007; February 2, 2007.

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Digital Object Identifier 10.1109/LMWC.2007.899318

Fig. 1. Proposed ring oscillator based divide-by-2 ILFD.

Fig. 2. Proposed ring oscillator based divide-by-3 ILFD.

stage for its high gain and low noise. It is widely implemented in the low noise applications. The CG configuration, however, is used as a wide-band amplifier for better input matching [9]. In the ILFD design, large locking range is the major consideration. Therefore, in the proposed design, a CG input stage is used instead of the conventional CS input. Moreover, the dc biasing of the tail MOS transistor can be close to zero. This helps the FD to work properly with a lower supply voltage [1]. In [1], the sub-1 V operation of the FD is presented. By using a common-gate configuration, the minimum supply voltage for a stable operation can be reduced, where the FD is able to work with a low supply voltage close to $\Delta V_{gs} + |V_{tp}|$. Figs. 1 and 2 show the topologies of the proposed divide-by-2 and divide-by-3 ILFDs. Here $MN1$ is the input stage, while other six MOS transistors form a ring oscillator. The output is fed back to the gate of $MN2$ to mix with the input signal.

It is not easy to give a very fair comparison for the CS and CG input since they have different gains. That means, if identical dc bias is applied to the two configurations, their power consumptions are not the same. Similar to the method in [9], here we set the power consumption of the ILFDs with CS and CG configurations to be the same by using different transistor size for the tail NMOS $MN1$. Then different input powers are injected to the two ILFD. For example, Fig. 3 shows the case for divide-by-2 ILFDs with two kind of input stages, where the CG

Fig. 3. Simulated center frequency and locking range of the divide-by-2 ILFDs with CS and CG input stages.

Fig. 4. Locking range of the two configurations in the divide-by-2 units.

configuration has a larger locking range. It also provides more stable center frequencies over different input power. Similar results can also be obtained in the divide-by-3 operation.

IV. EXPERIMENTAL RESULTS

To verify the performance of the proposed topology, besides the two topologies based on conventional designs, two ILFDs with common gate configurations as shown in Figs. 1 and 2 are fabricated. The four designs are implemented using the CSM 0.18- μm 1P6M CMOS process. Here the minimum transistor size is 4 $\mu\text{m}/0.18 \mu\text{m}$ instead of 1.6 $\mu\text{m}/0.2 \mu\text{m}$ in [7] to minimize the impact of process variations. Because there are only seven transistors in these designs, the core circuit is only about $20 \times 15 \mu\text{m}^2$, while the test chip is about $400 \times 300 \mu\text{m}^2$ due to the added output buffer and contact pads. The measurement is carried out on-wafer with a Cascade RF probe station. The input frequency is provided by Anritsu 68347C 10 MHz–20 GHz signal generator, the output is captured by the Lecroy Wave-master 8600A 6G oscilloscope. Fig. 4 shows the locking range of the two FDs at 0.8 V and 1 V operation, where $P_{\min}$ is the minimum input power. The proposed divider has a larger locking range and higher operating frequency. In the case of the

Fig. 5. Locking range of the two configurations in the divide-by-3 units.

1-V supply voltage, a locking range of 38% has been achieved in the proposed design. The proposed design is able to operate with a supply voltage of 0.7 V, while it can work up to 4.5 GHz with 1.5-V supply voltage.

The performance of the two divide-by-3 dividers are also measured and compared. Compared with the divide-by-2 operation, because of the improved method of injection, the locking range and the operating frequency of the divide-by-3 units have been increased. Fig. 5 shows the locking ranges of the two divide-by-3 units at 0.8 V and 1 V supplies. The proposed design with common gate configuration has a large locking range with 1 V supply voltage. A locking range of 40% has been achieved in the proposed design with a dc biasing current of 0.3 mA at 0.8 V supply. A locking range of 30% is achieved for the common source design at the same supply voltage. At higher supply voltage, both common source and common gate configurations have similar performances. For the supply voltage of 1.5 V, the two dividers have similar locking range from 2.2 GHz to 5.4 GHz with a power consumption of 1.1 mW. This operating range is able to cover most of the WLAN standards. The proposed design achieves a larger operating range with a low power consumption at a sub-1 V supply voltage. The phase noise varies under different input frequencies or supply voltages. The typical value of phase noise under locked condition at 1 MHz offset is -120 dBc/Hz.

Table I compares the performance of the proposed designs with other works reported. The measured performances of the divide-by-2 and divide-by-3 unit in sub-1 V operation with conventional common source configuration are included as a reference. In this table, the operating frequency locked in higher order of superharmonics in literature is not included since they can not be integrated in the full system. To make a fair comparison, the topology in [7] is also simulated using the same process and transistor size. For a fixed biasing for the PMOS load, the operating range is from 2.5 to 3.1 GHz with a power consumption

TABLE I
COMPARISON WITH OTHER WORKS

Work	V_{dd}	Process	f_{center}	Locking Range	DC Power Consumption
[1]	1	0.35 μm	3.1 GHz	140%	2.5 mW
[2]	/	0.13 μm	5 GHz	20%	10.4 mW
[3]	1.5	0.24 μm	4.9 GHz	20%	0.8 mW
[4]	2.5	0.25 μm	6.6 GHz	13%	3.75 mW
[5]	1.8	0.18 μm	3.3 GHz	60%	6.84 mW
[6]	1.5	0.24 μm	1GHz	2%	0.23 mW
[7]	0.8	0.2 μm	3.5GHz	43%	0.08 mW
[7] sim.	0.8	0.18 μm	2.8 GHz	22%	0.18 mW
divide-by-2	0.8	0.18 μm	1.3/1.3 GHz	30%/21%	0.21 mW
(CG/CS)	1	0.18 μm	3/1.9 GHz	38%/31%	0.36 mW
divide-by-3	0.8	0.18 μm	1.4/1.3 GHz	40%/30%	0.24 mW
(CG/CS)	1	0.18 μm	3/2.8 GHz	33%/30%	0.4 mW

tion of 0.18 mW. Here, we set the biasing of CG and CS to be the same to show how a wide locking range is obtained with the CG configuration.

V. CONCLUSION

In this letter, the design considerations in the ILFD are reviewed. The improved performance of the ILFD is obtained by using a new common gate configuration in the input stage. The proposed designs have been implemented in the conventional divide-by-2 and divide-by-3 operations. In the sub-1 V operation, the proposed design has a larger locking range with and a higher operating frequency. The maximum locking range of 40% is achieved with a power consumption of 0.24 mW.

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