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Electrical Characterization of Dielectrically Isolated Silicon Substrates Containing Buried Metallic Layers

W. L. Goh, J. H. Montgomery, S. H. Raza, B. M. Armstrong, *Member, IEEE*, and H. S. Gamble

Abstract—Dielectrically isolated substrates containing buried highly conducting WSi_2 layers are characterized for the first time using MOS capacitors. The active silicon layer is approximately $3\ \mu\text{m}$ thick with a buried WSi_2 layer $120\ \text{nm}$ thick adjacent to the isolation layer. The buried metal forms the back contact of the capacitor and excellent MOS characteristics are observed. Minority carrier lifetimes in excess of $200\ \mu\text{s}$ were measured indicating the suitability of these substrates for use in device manufacture.

I. INTRODUCTION

DIRECT wafer bonding is an emerging technology for the production of dielectrically isolated (DI) substrates [1], [2]. Applications for the technology exist in linear integrated circuits and smart power devices [3]–[6]. With specialized thinning techniques the active wafer thickness can be reduced to sub-micron dimensions offering silicon on insulator (SOI) substrates for potential application in advanced MOS IC's [7], [8]. Considerable work is being undertaken to produce and characterize this material. The ability to include a buried metallic layer in the DI substrate offers further potential advantages [9]. The metallic layer is much more conducting than even a high dose ion implantation and therefore could replace the heavily doped buried collector in bipolar transistors with a resultant reduction in collector resistance. Smart power IC's incorporating a number of power switching devices could be manufactured with such a substrate without increasing voltage drop. The buried metallic layer permits the use of multiple vertical power device structures rather than lateral devices since the metal, which may form the buried drain or buried collector terminal, can be patterned prior to bonding. DI substrates with buried metallic layers will also find application in optoelectronic and millimeter wave components and circuits. This work briefly describes the technology developed to produce the substrates and very importantly establishes the electrical performance of the silicon layer. Properties such as minority carrier lifetime are critical if the layers are to be used for high-performance integrated circuits. Extensive

capacitance-voltage measurements have therefore been carried out on the substrates using MOS capacitor structures.

II. EXPERIMENTAL

Substrates were prepared with buried WSi_2 layers. The active wafers were $100\ \text{mm}$ diameter n-type $\langle 100 \rangle$ orientated silicon of resistivity $9\text{--}15\ \Omega\text{-cm}$. Tungsten was deposited by rf magnetron sputtering. Typically the layer deposited was $50\ \text{nm}$ in thickness and the resistivity was $11\ \mu\Omega\ \text{cm}$. The W layer was capped with $0.8\ \mu\text{m}$ of polysilicon in a standard LPCVD reactor. The polysilicon layer is relatively rough and unsuited to bonding. A Westech polisher was used to remove approximately $0.3\ \mu\text{m}$ of polysilicon and produce a specular surface. The active wafers were then bonded, at room temperature in a class 10 environment, to oxidized handle wafers. The bonding was verified to be voidless by Infra-red transmission microscopy. The wafer pairs were then annealed at $1000\ ^\circ\text{C}$ for 2 h. This strengthens the bonds between the polysilicon and the oxide and simultaneously forms WSi_2 as the tungsten reacts with the single crystal silicon. A scanning acoustic microscope was used to verify that the bonds were still void free as shown in Fig. 1. The buried tungsten silicide resistivity was monitored and found to be $30\ \mu\Omega\ \text{cm}$. The active wafers were then thinned to $5\ \mu\text{m}$ using a Shibayama grinder and polished to various control thicknesses to yield a device quality wafer surface.

MOS capacitors were then manufactured in the active silicon layer. Initially vias were manufactured down to the buried silicide layer. Silicon nitride was deposited and patterned to protect the exposed WSi_2 . The exposed silicon was then oxidized at $1000\ ^\circ\text{C}$ in a dry oxygen ambient to produce an oxide layer approximately $70\ \text{nm}$ in thickness. The total time at temperature was 120 min. including the nitrogen anneal. The nitride layer was selectively etched from the WSi_2 regions in orthophosphoric acid. Aluminum was deposited and delineated to form both circular capacitor electrodes and ohmic contact pads to the exposed buried WSi_2 layer. The capacitors were annealed for 20 min. at $400\ ^\circ\text{C}$ in forming gas. The final device structure is as shown in Fig. 2.

III. RESULTS AND DISCUSSIONS

The substrates underwent several thermal cycles during device manufacture with no apparent evidence of stress or delamination problems. A typical high-frequency $C\text{--}V$ plot is shown in Fig. 3. The solid line represents the experimentally measured values of capacitance as a function of gate voltage

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W. L. Goh was with Northern Ireland Semiconductor Research Centre, Department of Electrical and Electronic Engineering, The Queen's University of Belfast, Belfast BT9 5AH, Northern Ireland, U.K. He is now with the Department of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798.

J. H. Montgomery, S. H. Raza, B. M. Armstrong, and H. S. Gamble are with Northern Ireland Semiconductor Research Centre, Department of Electrical and Electronic Engineering, The Queen's University of Belfast, Belfast BT9 5AH, Northern Ireland U.K.

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Fig. 1. Scanning acoustic micrograph of a DI substrate with a buried WSi_2 layer exhibiting no voids.

Fig. 2. Cross section drawing of the MOS capacitor structures on the DI substrate.

Fig. 3. A typical high-frequency $C-V$ plot.

bias. The points plotted on the graph were calculated using ideal MOS analytical theory. The capacitors show excellent properties and were characterized with an oxide thickness

Fig. 4. Active layer doping concentration versus distance from the gate oxide-silicon interface. Measurements achieved using pulsed $C-V$ techniques.

of 67.5 nm, substrate doping of $3.5 \times 10^{14} \text{ cm}^{-3}$ and a fixed charge density of approximately $2 \times 10^{10} \text{ cm}^{-2}$. This value of fixed charge is typically what is obtained when using conventional silicon control samples. The low fixed charge density and the lack of distortion in the $C-V$ plot due to fast interface states is very encouraging. Pulsed $C-V$ measurements have been used to examine the substrate doping profile. This is shown in Fig. 4. The substrate doping is in good agreement with the value obtained from the high-frequency $C-V$ measurement. As expected there is pile up of the phosphorous dopant in the substrate at the oxide-silicon surface due

Fig. 5. C - t profiles for capacitors driven by a step in voltage from accumulation into deep depletion. Several voltage steps are shown.

to dopant segregation during silicon oxidation. There is also evidence of a snow-plow effect during silicide formation at the silicon-tungsten disilicide interface. The silicon thickness is marked by the rapid rise in apparent dopant as the depletion layer width extends out to the buried metal layer.

Capacitance-time plots are given in Fig. 5 for a series of applied voltage steps. These well behaved plots show a steady increase in capacitance with time as the device recovers from deep depletion to steady state inversion. The Zerbst analysis technique has been used to extract minority carrier lifetimes from this data. This yields a minority carrier lifetime for this device of $340 \mu\text{s}$. Most devices show values in the range

$200 \mu\text{s}$ – 1 ms indicating that the material has good lifetime well suited to device applications.

IV. CONCLUSIONS

Dielectrically isolated silicon substrates containing buried WSi_2 layers have been employed to manufacture MOS capacitors. The devices exhibit excellent MOS action as characterized by high-frequency C - V measurements. The pulsed C - V measurement has proved ideal for characterizing both the active layer doping level and the position of the buried metal layers. C - t and Zerbst analysis indicates relatively high lifetimes greater than $200 \mu\text{s}$. This shows that these substrates are not seriously stressed after 4-h postbond processing at 1000°C and are well suited for high-performance circuit fabrication.

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