Failure analysis of bond pad metal peeling using FIB and AFM

Tan, Cher Ming; Er, Eddie; Hua, Younan; Chai, Vincent Siew Heong

1998

Tan, C. M., Er, E., Hua, Y., & Chai, V. (1998). Failure analysis of bond pad metal peeling using FIB and AFM. *IEEE Transactions on Components, Packaging, And Manufacturing Technology-Part A*, 21(4), 585-591.

<https://hdl.handle.net/10356/91599>

<https://doi.org/10.1109/95.740049>

© 1998 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE. This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder. <http://www.ieee.org/portal/site>.

Downloaded on 26 Apr 2023 23:03:53 SGT

Failure Analysis of Bond Pad Metal Peeling Using FIB and AFM

Cher Ming Tan, *Member, IEEE*, Eddie Er, Younan Hua, and Vincent Chai

Abstract—Aluminum bond pads on semiconductor chips play an important role in chips functionality and reliability. Bond pad peeling during wire bonding process results in yield reduction. The failure mechanisms of the peeling must be identified so that potential reliability problem of poor bond pad adhesion can be avoided. In this work, FIB, SEM, EDX, and AFM are used to identify the root causes of the peeling. The possible root causes are found to be the presence of an extra layer of thickness of $0.14\text{ }\mu\text{m}$ and the poly-silicon surface roughness asperity due to prolonged BOE etching time.

Index Terms—AFM, bond pad, EDX, failure analysis, FIB, SEM.

I. INTRODUCTION

THE focus ion beam (FIB) technique has become one of the most necessary failure analysis tools for VLSI's in the past several years. Three functions are available in FIB technique, namely the partial etching, partial metal deposition, and scanning ion/electron microscopy [1]. The partial etching function of FIB can be used for microscopic cross sectioning on VLSI chip, and the scanning ion/electron microscopy can be used for in-situ observation on a VLSI. These applications were introduced by Kaito *et al.* [2], and applied to VLSI failure analysis by Nasu *et al.* [3] and Nikawa *et al.* [4], [5]. In this work, FIB is used to perform failure analysis on bond pad metal peeling problem on a $0.8\text{ }\mu\text{m}$ single poly double metal logic device.

The structure of the Al bond pad consists of several metal stacks as shown in Fig. 1. The bond pad peeling was observed after the wire bonding operation with average fallout of 0.75%. The shape of the peeling was same as the ball size. Both optical and SEM inspection showed no obvious Al or TiW barrier remain on the peeled surface as shown in Figs. 2 and 3. Investigation into the bonding machine parameters showed no commonality at any wire bonder, and no major changes of the bonding parameters has been made. Therefore, the bonding process was ruled out as the cause of the failure, and wafer fab process was suspected to be the source of failure mode.

Fig. 1. Schematic structure of a bondpad.

Fig. 2. Optical micrograph of the peeled bond pad.

Fig. 3. SEM micrograph of the peeled bond pad.

Manuscript received September 29, 1997; revised July 20, 1998. This paper was recommended for publication by Associate Editor L. Burton upon evaluation of the reviewers' comments.

C. M. Tan is with the Department of Electrical and Electronic Engineering, Microelectronic Division, Nanyang Technological University, Singapore 639798.

E. Er, Y. Hua, and V. Chai are with Chartered Semiconductor Manufacturing Ltd., Singapore Science Park, Singapore.

Publisher Item Identifier S 1070-9886(98)09138-0.

Fig. 4. SEM micrograph of the poly-silicon surface showing the roughness and porosity of the poly surface.

Fig. 5. EDX spectrum and quantification results at 5 kV on the peeled off surface as indicated by the arrow. The results showed mostly silicon (96.2 wt%), traces of O (2.8 wt%), and P (1.0 wt%). This suggests that the peeled off surface is the poly surface.

II. SURFACE SEM/EDX ELEMENTAL ANALYSIS

In order to investigate the failure mechanisms, we began the SEM and EDX analysis on the peeled pads. Surface SEM examination on the peeled off surface showed that the surface was very rough and porous as shown in Fig. 4. ZAF standardless quantification EDX on the peeled-off surface at 5 keV detected mostly Si (96.2 wt%) and traces of O (2.8 wt%) and P (1.0 wt%), and EDX on the peeled-off side of the Al

film detected mostly the present of W, Si, and Ti. The EDX spectrums are shown in Figs. 5 and 6. These results implied that the peeling occurred likely at the poly Si and TiW/Ti interface.

III. FIB CROSS-SECTIONING AND SEM/EDX ANALYSIS

In order to clarify the postulation, a cross-section on a bond pad is performed. However, it is difficult to cross-

Fig. 6. EDX spectrum and quantification results at 10 KV on the peeled off size of the film as shown by the arrow.

section the pad by mechanical polishing as the pad will be badly damaged or peeled off during polishing. Hence FIB is used to provide precise cross section to the bond pad so that minimum contamination and damage are introduced [4].

The sample was first coated with Pt using conventional coater in order to prevent possible sample charging problem during FIB operation. It was then put into FEI 611 single beam FIB system. Prior to cross sectioning, a strip of Pt was deposited on the area of interest using ion beam induced Pt deposition to protect the sample surface [6]. This measure can minimize the introduction of artifacts and avoid complicating SEM/EDX analyzes [7]. The FIB cross sectioning was performed from coarse chemical enhanced etching to fine milling using finely focused 25 keV Ga⁺ ion beams. Then, the cross-sectioned area was fine polished at low beam current to produce a final finish [7].

The locations of the cross-sectioning is shown in Fig. 7. The cross-sectioned bond pads are observed under FESEM using the Hitachi S-4100 machine. The results for the peeled pad are shown in Figs. 8 and 9. From the results, an extra layer of about 0.14- μ m-thick was found between the Ti and Poly Si layers. No such extra layer was found on the good adjacent bond pad as shown in Fig. 10. Peeling was observed to occur at the extra layer/poly Si and Ti/extra layer. It is therefore possible that this extra layer is one of

Fig. 7. SEM micrograph showing the locations of FIB cut on a good pad (denoted as G on the arrow) and a peeled pad (denoted as B on the arrow).

the causes of poor adhesion of Al bond pad on the poly Si.

In order to identify the nature of this extra layer, x-ray microanalysis is used. However, since the thickness of the extra layer is only 0.14 μ m, a proper selection of the incident beam energy is important. The spatial resolution b of x-ray microanalysis for bulk specimen can be computed as follows

Fig. 8. SEM micrograph of the FIB cross-sectional portion of the peeled pad.

Fig. 10. SEM micrograph of the FIB cross-sectional portion of the good pad.

Fig. 9. Enlargement of Fig. 7 showing the presence of the extra layer.

[8]:

$$b = \frac{2 \times 10^{-7}}{\rho} (E_o^{1.5} - E_c^{1.5}) \text{ meters} \quad (1)$$

where ρ is the density of the material in Mg/m^3 , E_o is the incident beam energy in keV, and E_c is the critical energy for X-ray line excitation in keV. Using (1), and since Ti and W are the suspected elements from the previous EDS analysis, one can calculate the required acceleration voltage of the incident electron beam as shown in Table I. Hence, 5 keV is chosen for the EDX examination on the extra layer.

The resulting EDX spectrum on the extra layer at 5 keV showed in Fig. 12 revealed the presence of Si, Al and W. Ti peak cannot be observed, if any, due to the low incident beam energy used. Comparing the EDX spectrum and quantification results of the barrier metal (Fig. 11) and that of the extra layer (Fig. 12), the weight % of W increases from 72% in Fig. 11 to 83% in Fig. 12. Since the extra layer is further away from the TiW layer, the increment of the weight % of W suggested

that the extra layer could be a W layer or Ti_xW_y layer. This is further substantiated by the presence of W and Ti on the peeled surface as shown in Fig. 6 (the Ti peak could also possibly come from the barrier metal underneath the extra layer). The cause of the extra layer is suspected to be the erroneous opening of the shuttles for Ti and W during the barrier metal deposition processes. Awareness of the bondpad metal peeling problem leads to a more cautious operation in the metal deposition, and the problem is no longer existent after the incident, without any process change or machine maintenance.

IV. SURFACE ROUGHNESS ANALYSIS USING AFM

Bond pad metal peeling is an adhesiveness problem. Besides the presence of the extra layer that may affect the metal adhesiveness to the poly silicon, the surface morphology of the poly silicon may also affect the adhesiveness [10], [11]. Kokini and Sheets [10] found that no normal stress is present in the film along the interface when the substrate roughness amplitude is small. When the roughness is increased, the normal stress remains essentially zero over the peaks and valley of the "rough" surface, and is maximum midway between these two locations. Hopple *et al.* [11] found that the load will be more evenly distributed when the surface asperity is smaller. Therefore, if a surface roughness is high, the tendency of peeling will be higher. The tendency will be enhanced if the surface asperity is high as well, and delamination of the overcoating film will be likely to occur at and near the location of the high asperity. In this work, the morphology of the poly-silicon surface was studied using the digi-atomic force microscope (AFM). The study examined five pads with a total of nine locations as illustrated in Fig. 13. The results of AFM were summarized in Table II. From the maximum peak and the mean roughness, one can qualitatively estimate the degree of localization of the peak distribution (asperity) of the surface under examination. If the peaks distribution is very localized, then the maximum peak will be high, while the mean roughness is low, and vice versa.

Fig. 11. EDX spectrum and quantification results at 5 KV on barrier metal 1 layer as shown by the arrow. The results showed mostly W (72.64 wt%) and traces of C, O, Al, and Si (Ga is from the FIB cross sectioning process).

TABLE I
RELATION BETWEEN EDX SPATIAL RESOLUTION AND INCIDENT
BEAM ENERGY FOR Ti AND W. NOTES: E_c FOR W IS
TAKEN AS 1.8 keV, AND THAT FOR Ti IS 4.5 keV [9]

Element	Density (Mg/m ³)	Accelerating Voltage (keV)	Spatial Resolution (μ m)
W	19.3	5	0.091
		10	0.30
		15	0.58
Ti	4.54	5	0.071
		10	0.97
		15	2.14

TABLE II
RESULTS OF AFM

Dice Type	Location	Max Peak (nm)	Mean Roughness (nm)	Localization Factor
Bad Dice	A2	254.55	13.88	18.34
	B1	158.23	13.70	11.55
	B2	150.47	15.68	9.60
	C1	168.77	15.34	11.00
	C2	138.18	15.22	9.08
Good Dice	D1	145.66	15.27	9.54
	D2	152.90	14.85	10.30
	E1	194.58	19.72	9.89
	E2	225.14	19.77	11.39

Thus, a localization factor defined as the ratio of maximum peak to the mean roughness can be used to show the asperity of the surface.

Compare the wire bonding region of the good and bad dices, B1 versus D1, and C1 versus E1 in Table II, one found the localization factor are higher for bad dice. Hence the distribution of the applied normal stress at the metal/poly Si interface due to the wire bonding force is expected to be much uneven in bad dice. This uneven stress distribution will leads to early failure, i.e., bond-pad peeling. Hence the study showed the importance of the localization factor of the surface roughness in bond-pad peeling.

To investigate the likely cause of high localization factor, comparison of the process conditions of all the processes for the bad lots and good lots was conducted. It was found that the etching time of BOE after poly densification was identified as the most possible cause. Experiments on the effect of etch time of BOE on the poly Si surface roughness were performed, and the results was plotted as shown in Fig. 14. One can see the direct impact of BOE etch time on the Poly Si surface roughness localization factor.

Fig. 12. EDX spectrum and quantification result at 5 kV on the extra layer as shown by the arrow. The results showed mostly W (83.11 wt%) and traces of C, O, Al, and Si (Ga is from the FIB cross sectioning process).

Fig. 13. Probe locations of atomic force microscope analysis.

Fig. 14. Effect of BOE etch time on the poly silicon roughness.

V. DISCUSSIONS

FIB and AFM studies showed that the possible failure mechanisms for the bondpad peeling problem could be the extra layer and the morphology of the poly-Si surface underneath the bondpad. To confirm the failure mechanisms, further experiments are required.

The first experiment is to examine if the extra layer is indeed one of the failure mechanisms. This experiment can be performed by producing wafers with the localization factors (in the bonding region) greater than 11 by prolonged BOE etch. These wafers can then be sent for wire bonding with the identical bonding parameters. Now that these wafers do not have the extra layer (as the problem of extra layer has disappeared), and their poly-Si have similar surface morphology as those in the bad dices. If no bondpad peeling is observed in this new experiment, then extra layer will be the confirmed root cause. Otherwise, the surface morphology of poly-Si as one of the causes will be confirmed.

Another experiment to examine the effect of BOE etch time on barrier metal adhesiveness without the extra layer is also important in establishing the root causes. These experiments will be planned and carried out in the future.

VI. CONCLUSION

Failure analysis on bond pad peeling problem was performed using FIB, SEM, EDX, and AFM. It was found that the problem was not assembly related, but was wafer fab related. The possible failure mechanisms of the bond pad peeling may be related to the presence of an extra layer and the morphology of the poly Si surface. The likely cause of the presence of the extra layer is the erroneous metal deposition operation during wafer fabrication, and the likely cause of the roughness asperity of the poly Si surface is the prolonged BOE etch time.

ACKNOWLEDGMENT

The authors would like to thank Z. Siping, IME, J. Chia, TMI, and J. W. Dong, CSM, for their support of this work.

REFERENCES

- [1] K. Nikawa, "VLSI failure analysis: A Review," *Microelectron. Reliab.*, vol. 32, no. 11, p. 1589, 1992.
- [2] T. Kaito and T. Adachi, "Focused ion beam system for IC development and its applications," in *Proc. 1st Micro Process Conf., Tokyo, Jpn. Soc. Appl. Phys.*, 1988, p. 142.
- [3] K. Nasu, M. Murase, K. Nikawa, S. Inoue, T. Kaito, and T. Adachi, "Application of focused ion beam to the failure analysis and reliability evaluation for LSI—Micro cross-sectioning and Al microstructure observation," in *Proc. Symp. Electron Beam Testing (EBTS)*, Osaka University, Japan, 1988, p. 13.
- [4] K. Nikawa, N. Nasu, M. Murase, T. Kaito, T. Adachi, and S. Inoue, "New applications of focused ion beam technique to failure analysis and process monitoring of VLSI," in *Proc. Int. Reliab. Physics Symp.*, 1989, p. 43.
- [5] K. Nikawa, S. Hosoi, M. Murase, N. Hirayama, K. Nasu, and H. Yuasa, "Failure analysis techniques for LSI," *NEC Tech. J.*, vol. 41, no. 14, p. 292, 1988.
- [6] K. Gamo, N. Takakura, N. Samoto, R. Shimizu, and S. Namba, "Ion beam assisted deposition of metal organic films using focused ion beams," *Jpn. J. Appl. Phys.*, vol. 23, pt. 2, no. 5, pp. 293-295, 1984.
- [7] S. P. Zhao, Y. N. Hua, G. P. Goh, Z. R. Guo, and K. W. Chau, "Contamination analyzes of Al bondpads using FIB/SEM/EDX," in *Proc. Int. Symp. Phys. Failure Anal. Integr. Circ.*, 1997, p. 254.
- [8] I. P. Jones, *Chemical Microanalysis Using Electron Beams*. London, U.K.: Institute of Materials, 1992, p. 176.
- [9] *Handbook of Chemistry and Physics*, 59th ed. Orlando, FL: CRC, 1978-1979.
- [10] K. Kokinin and B. E. Sheets, "Thermal stresses under engine heat flux: 2. Thin metallic films on ceramic coatings," *Composite Mater. Technol.*, vol. 37, p. 263, 1991.
- [11] G. B. Hopple, J. E. Keem, and S. H. Loewenthal, "Development of fracture resistant, multilayer films for precision ball bearings," *Wear*, vol. 162-164, p. 919, 1993.

Cher Ming Tan (M'98) was born in Singapore in 1959. He received the B.Eng. degree in electrical engineering from the National University of Singapore in 1984, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, Ont., Canada, in 1988 and 1992, respectively.

He has been in the field of reliability and failure analysis in semiconductor devices since 1984. In April 1997, he joined the Nanyang Technological University, Singapore, as a Lecturer in the School of Electrical and Electronic Engineering, teaching a reliability related course.

Eddie Er received the B.S. degree in chemical engineering from the University of Massachusetts, Lowell, in 1985.

He is a Principal Engineer in the QA Department, Chartered Semiconductor Manufacturing, Singapore. He has over 12 years of experience in many aspects of package and device failure analysis. His areas of research interest include application of emission microscopy technique in studying different failure mechanisms, application of voltage contrast and EBIC in studying submicron metal line and via EM failures, and application of TEM in thin-film interfacial problems and material characterizations.

Younan Hua received the B.S. degree in chemistry from Chang Chun Geol University, China, in 1982, the M.S. degree from Nanjing University, China, in 1988, and the Ph.D. degree in physics from the National University of Singapore in 1994.

He is a Principal Engineer at Chartered Semiconductor Manufacturing, Singapore, in the QA Department, working on the failure analysis of wafer fabrication. He has more than 15 years of working experience. His areas of research interest include application of various surface analytical techniques (SIMS, Auger, XPS, XRD, TXRF, etc.) in wafer fabrication.

Vincent Chai received the B.S. degree in chemical engineering from the University of Wisconsin at Madison in 1996.

He has been a Process Engineer in the Etch Department, Chartered Semiconductor Manufacturing, Singapore, for the past two years, working primarily in back-end wet and dry etching.