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A Temperature-Dependent DC Model for Quarter-Micron LDD pMOSFET's Operating in a Bi-MOS Structure

Kok Wai Chew, Samir S. Rofail, *Senior Member, IEEE*, and Kiat Seng Yeo

Abstract—A temperature-dependent analytical model for deep submicrometer LDD p-channel devices operating in a Bi-MOS structure is reported for the first time. This model is based on experimental data obtained from 0.25- μm process wafers with a wide range of technologies (0.25–1.0 μm). The measurements have been performed within the temperature range 223–398 K (–50 °C to +125 °C). The model accounts for the effects of independently biasing the source, drain, gate and body potentials, scaling, and the influence of temperature on the threshold voltage and the device currents. The effect of temperature on the device transconductance and the output conductance have also been examined. The results revealed that close agreement between the analytical model and the experimental has been achieved. Comparisons between the principal MOS current and the lateral bipolar current have been made to demonstrate the improvement of the latter with temperature for the quarter-micron devices.

NOMENCLATURE

Λ	LDD region fitting parameter.
A_{bipolar}	Effective cross-sectional area for the bipolar current.
A_{space}	Effective cross-sectional area for the space charge current.
C_{ox}	Gate oxide capacitance per unit area.
α	Space charge current model parameter.
α_1	Coefficient 1 in the effective hole mobility model.
α_2	Coefficient 2 in the effective hole mobility model.
α_3	Coefficient 3 in the effective hole mobility model.
D_i	Threshold adjust implant dosage per unit area.
D_p	Hole diffusion constant.
ΔE_g	Bandgap narrowing between source and body.
ϵ_{ox}	Permittivity of silicon dioxide.
ϵ_{si}	Permittivity of silicon.
E_{eff}	Effective transverse electric-field.
E_c	Critical electric field.
E_g	Bandgap energy.

E_F	Fermi level of extrinsic semiconductor.
E_{Fi}	Fermi level of intrinsic semiconductor.
γ	Forward source-body effect factor.
ϕ_s	Surface potential of silicon.
φ	Empirical parameter in defining E_{eff} .
g_{m1}	Transconductance associated with the variation of the source-gate voltage.
g_{m2}	Transconductance associated with the variation of the source-body voltage.
g_{sd}	Output conductance.
h	Planck constant.
η	Drain-Induced Barrier Lowering parameter.
I_S	Forward-bias saturation current of a pn junction.
I_{space}	Space charge limiting current.
I_{mos}	MOS current.
I_{bipolar}	Lateral bipolar current.
I_{body}	Body current.
ς	Bipolar current model parameter.
$\varsigma_1(V_{SB})$	Source-body bias dependent bipolar current parameter.
$\varsigma_2(T)$	Temperature-dependent bipolar current parameter.
λ	Source barrier height lowering fitting parameter.
k	Boltzmann constant.
l_c	Characteristic length.
L	Device drawn channel length.
L_e	Electrical channel length.
L_{eff}	Device effective channel length.
L_{effav}	Average effective channel length.
L_d	Electrical channel length for the MOS current.
L_p	Length of the LDD p-region.
μ_p	Hole mobility in the channel/bulk.
μ_1	Empirical parameter 1 in the effective hole mobility model.
μ_2	Empirical parameter 2 in the effective hole mobility model.
μ_3	Empirical parameter 3 in the effective hole mobility model.
μ_{peff}	Effective hole mobility.
m_e^*	Density-of-state effective mass for electrons.
m_h^*	Density-of-state effective mass for holes.
m_o	Electron mass at rest.
N_a	Source/drain concentration.
$N_a -$	LDD p-concentration.
N_{sub}	Channel doping concentration.

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N_c	Effective density of states in conduction band.
N_v	Effective density of states in valence band.
n_i	Intrinsic doping concentration of silicon.
n_f	Ideality factor.
P_e	Hole concentration at the edge of the source(emitter)/n-well junction.
Q_{dep}	Depletion carrier density.
Q_{inv}	Inversion carrier density.
q	Electronic charge.
R_{well}	Average well resistance.
r_j	LDD p-implant junction depth.
T_{ox}	Gate oxide thickness.
T	Temperature at which measurements are carried out.
TC_1	Temperature compensation factor 1.
TC_2	Temperature compensation factor 2.
T_{nom}	Ambient room temperature.
v_{sat}	Saturation velocity of the carriers.
V_{bi}	Built-in potential of the LDD p-/n-well regions.
V_{j1}	Junction potential between the source and the body.
V_{j2}	Junction potential between the drain and the body.
V_t	Thermal voltage.
V_{FB}	Flatband voltage.
V_{SB}	Source-body voltage.
V_{SBeff}	Effective source-body voltage.
V_{SD}	Source-drain voltage.
V_{SDeff}	Effective source-drain voltage.
V_{SG}	Source-gate voltage.
V_{Teff}	Effective threshold voltage.
ΔV_T	Threshold voltage shift.
V_{TO}	MOSFET threshold voltage at V_{SD} and $V_{SB} = 0$ V.
W	Device channel width.
θ	Charge-sharing factor.
X_{dep}	Depletion layer thickness.
X_{dm}	Depletion width at the drain's surface.
X_j	P ⁺ implant junction depth.
X_s	Depletion width at the source.
X_d	Depletion width at the drain.

I. INTRODUCTION

It is well known that bipolar transistors exhibit lower noise and higher speed performance as compared to MOSFET's. However, MOS devices have lower power dissipation, higher packing density, and can operate at very low currents. Hybrid-mode devices, employing lateral pnp BJT in a pMOS structure, have been able to capitalize on the advantages of both type of devices. Hybrid-mode devices can also be referred to as devices in the Bi-MOS structure.

Hybrid-mode devices have received much attention in the past due to their high-performance and their availability without any additional processing steps [1]–[5]. In recent years, they have received renewed interest and have been frequently employed in CMOS/BiCMOS digital circuits for low-voltage applications [6]–[8], as well as in analog circuits [9]. An

analytical model for deep submicrometer pMOSFET's operating in a hybrid-mode environment has been reported [10]. However, the earlier model caters for quite a narrow range of technologies (0.4–0.7 μm) and did not address the effect of temperature on the hybrid-mode device performance. Its prediction for the ratio of the lateral bipolar current to the principal MOS current when the channel length scales to sub-half-micrometer (at room temperature and under high-level injection) has been verified in the present work. This work takes into consideration also the additional punchthrough implants in the well that accompanied scaling to suppress short-channel effects.

In this work, the interdependencies between temperature, scaling, the different biases, the threshold voltage and the various current components that flow in the hybrid mode have been investigated and the findings incorporated into the analytical equations. The model caters for a wide range of technologies (0.25–1.0 μm) and biases, and it is based on experimental data obtained from 0.25- μm process wafers. The significance of this work arises from the fact that it accounts for the realistic operating conditions of hybrid-mode devices.

The paper is organized as follows. In Section II, we describe how the devices are fabricated. Sections III–VI outline the models of the threshold voltage, the space-charge current, the lateral bipolar current and the MOS current respectively. Section VII summarizes the effect of temperature on the device transconductance and the output conductance.

II. DEVICE FABRICATION

The transistors used in our study have been fabricated using the 0.25- μm process flow. To counter short-channel effects, the dual-doped polysilicon gate approach utilizing surface p-channel transistors has been adopted. The retrograde twin-well process has been used to improve the isolation and increase the packing density. Transistor sizes ranging from 20 μm down to 0.25 μm are available for characterization.

The transistor formation begins with the deposition of a thick resist to cater for high energy well implants. The retrograde n-well for the p-transistors is formed by the implantation of phosphorus (2e13 cm^{-2} , 490 keV) tilted at 7° to minimize channeling effects [11]. The n-well junction depth is about 1 μm with a sheet rho of approximately 675 $\Omega/\square$. Following that is the p-channel punchthrough implant (5e12 cm^{-2} , 140 keV) and the p-channel threshold adjust implant (3e12 cm^{-2} , 70 keV). A 50 Å nitrided (N_2O) gate oxide is next grown. The N_2O gate oxide prevents the diffusion of dopants from the p⁺ polysilicon gate into the silicon. After the polysilicon gate definition, boron difluoride (BF_2) p-LDD implant (2e14 cm^{-2} , 20 keV) is subsequently carried out. The p-LDD junction depth is approximately 0.075 μm . Next, LDD spacers are formed by the deposition of a 1500 Å tetraethylorthosilane (TEOS) liner, followed by anisotropic etchback. The p⁺ source and drain regions are formed using BF_2 (3e15 cm^{-2} , 30 keV) for shallower junction formation and anneal using a short thermal cycle. The p⁺ junction depth is approximately 0.15 μm with a sheet rho of approximately 100 $\Omega/\square$. Note that for surface p-channel transistors, the

Fig. 1. Annotated SEM microphotograph of the cross section of the 0.25- μm pMOSFET.

polysilicon gate is initially undoped but will be heavily p-doped during the p-LDD, source and drain implants.

The wafers have been processed to metal layer 1, etched and sent for electrical characterization. The device currents were extracted using the HP4142 semiconductor parametric analyzer interfaced with ICCAP version 5.0 in a HP workstation. The wafers were placed inside the micro-chamber of a Cascade probing system and the chamber temperature controlled to within $\pm 0.1^\circ\text{C}$ using the Temprotronics temperature controller. Fig. 1 shows an annotated SEM photomicrograph of the cross section of one of the devices fabricated.

III. THE THRESHOLD VOLTAGE MODEL

The threshold voltage model is formulated by extending the classical long-channel threshold voltage to account for short-channel effects that occur with the scaling of technology. The effects included are 1) charge-sharing, 2) drain-induced barrier lowering (DIBL), and 3) forward source-body effects. The experimental threshold voltages have been obtained using the transconductance peak method [12].

The proposed threshold voltage model including short-channel effects and temperature variations is given by

$$V_{T\text{eff}} = V_{T\text{eff}}(T = T_{\text{nom}}) + (TC_1 + TC_2 V_{SB\text{eff}}) \left(\frac{T}{T_{\text{nom}}} - 1 \right) \quad (1a)$$

where

$$V_{T\text{eff}}(T = T_{\text{nom}}) = V_{TO} - \eta V_{SD\text{eff}} - \gamma V_{SB\text{eff}} \quad (1b)$$

$$V_{TO} = -V_{FB} + \frac{qD_i}{C_{\text{ox}}} + \phi_s + \frac{\theta}{C_{\text{ox}}} \sqrt{2q\epsilon_{\text{si}} N_{\text{sub}} \phi_s} \quad (1c)$$

$$V_{FB} = \frac{E_g}{2} + \frac{\phi_s}{2} \quad (1d)$$

$$\theta = 1 - \kappa r_j \quad (1e)$$

$$\kappa = 23e^{-22L^2} + 5.3e^{-0.1L} \quad (1f)$$

T and T_{nom} are in kelvins, and r_j and L are in micrometers. V_{TO} is the threshold voltage at zero drain and body biases and it contains the charge-sharing factor θ [13], [14] to account for the lowering of the threshold voltage due to termination of the built-in field by the overlapping depletion regions of the source and drain junctions. The effective source-drain and source-body voltages represent the reduction in the applied voltages due to the LDD regions [15].

The DIBL factor and the forward source-body effect factor have been modeled using the methodology outlined in [10] and they are given by

$$\eta = 0.8e^{-70L^2} + 0.25e^{-10L} \quad (2)$$

$$\gamma = 0.5(1 - e^{-10L^{1.6}}) - V_{SB}e^{-50L} \quad (3)$$

L is in micrometers. The experimentally extracted DIBL factor showed its insensitivity to temperature. A similar finding has been reported in [16]. The forward source-body effect factor has also been found to be a weak function of temperature (experimental data to justify this will be shown later). Hence the device threshold voltage is modeled using two components: the first encompassing the various short-channel effects at room temperature, where T_{nom} is the ambient room temperature, and the second is the temperature compensation term.

The effect of scaling coupled with DIBL and forward source-body effects at two different temperatures is shown in Fig. 2. The threshold rolloff for $L < 0.4 \mu\text{m}$ is due to the severe charge-sharing effect of very short-channel devices. The graph reaffirms that the DIBL effect and the forward source-body effect are rather insensitive to temperature. The plot of the threshold voltage against temperature depicted in Fig. 3 also supports the latter claim. It can also be seen that the threshold voltage changes linearly with temperature for the two different channel lengths. It decreases with temperature due to Fermi level shifts [17]. Figs. 4 and 5 illustrate the match of the analytical threshold voltage model with the experimental data for the range of source-drain and source-body biases considered in the experiment.

The threshold voltage shift at room temperature is shown in Fig. 6. This shift is defined as

$$\Delta V_T(T = T_{\text{nom}}) = \eta V_{SD} + \gamma V_{SB} \quad (4)$$

Fig. 6 records the percentage contribution of ηV_{SD} and γV_{SB} to the room temperature threshold voltage shift respectively for each technology. For $L = 0.25 \mu\text{m}$, at large source-drain bias and forward source-body bias, the DIBL effect and the forward source-body effect have approximately equal contributions in the reduction of the threshold voltage. But for $L = 1.0 \mu\text{m}$, the DIBL effect is nonexistent and the forward source-body effect is the sole cause for the lowering of the threshold voltage.

The temperature-dependent threshold voltage shift is depicted in Fig. 7. ΔV_{T1} is obtained by finding the difference between the threshold voltages at $V_{SB} = 0.6 \text{ V}$ and $V_{SB} = 0.0 \text{ V}$ for each temperature, and ΔV_{T2} is found by subtracting the threshold voltage for each temperature from that at T_{nom} for a particular V_{SB} . The data for ΔV_{T1} confirms

Fig. 2. Effect of scaling the channel length on the threshold voltage for two different V_{SD} , V_{SB} and temperature values.

Fig. 3. Effect of temperature variation on the threshold voltage for two different V_{SB} and channel lengths.

that the forward source-body effect is a weak function of temperature. The data for ΔV_{T2} reveals that the threshold voltage shift due solely to temperature is linear over the range of temperatures concerned.

IV. THE SPACE-CHARGE CURRENT MODEL

Due to the close proximity of the source and drain regions of deep submicrometer devices, the depletion regions of the two reverse-biased p-n junction can spread and eventually touch each other giving rise to punchthrough condition. For very short-channel devices, carriers from the source can surmount

Fig. 4. Effect of varying V_{SD} on the threshold voltage for two different channel lengths and temperature values.

the source-body barrier height by thermionic emission and then be swept across from the source to the drain by the strong longitudinal electric field, hence constituting to space-charge current flow.

The space-charge current has been extracted using the methodology outlined in [10] and modeled as a function of temperature by [17]–[20]

$$I_{\text{space}} = \frac{\alpha A_{\text{space}} \epsilon_{\text{si}} \mu_p V_{SD}^2}{L_{\text{effav}}^3}, \quad \frac{\mu_p V_{SD}^2}{L_{\text{effav}}} < \nu_{\text{sat}} \quad (5a)$$

$$I_{\text{space}} = \frac{\alpha A_{\text{space}} \epsilon_{\text{si}} \nu_{\text{sat}} V_{SD}}{L_{\text{effav}}^2}, \quad \frac{\mu_p V_{SD}}{L_{\text{effav}}} \geq \nu_{\text{sat}} \quad (5b)$$

Fig. 5. Effect of varying V_{SB} on the threshold voltage for two different channel lengths and temperature values.

Fig. 7. Effect of temperature variations on the temperature dependent threshold voltage shifts for two different channel lengths and V_{SB} .

Fig. 6. Effect of channel scaling on the percentages of ηV_{SD} and λV_{SB} with respect to the room temperature threshold voltage shift for two different V_{SD} .

where [see (5c), shown at the bottom of the page]

$$\alpha = 5.0 \times 10^{-14} e^{T/19} \quad (5d)$$

$$N_{sub} = 0.9121 n_i e^{(E_F - E_{Fi})/kT} \quad (5e)$$

$$n_i = \sqrt{(N_c N_v)} e^{-(E_g/2kT)} \quad (5f)$$

$$N_c = 2 \left(\frac{2\pi m_e^* kT}{h^2} \right)^{3/2} \times 10^{-6} \quad (5g)$$

$$N_v = 2 \left(\frac{2\pi m_h^* kT}{h^2} \right)^{3/2} \times 10^{-6} \quad (5h)$$

$$m_e^* = (1.036 + 4.263 \times 10^{-4} T) \times m_o \quad (5i)$$

$$m_h^* = (0.58 + 7.72 \times 10^{-4} T) \times m_o \quad (5j)$$

$$E_g = 1.170 - \frac{4.73 \times 10^{-4} T^2}{T + 288} \quad (5k)$$

$$\nu_{sat} = \frac{6 \times 10^6}{1 + 0.8e^{T/600}} \quad (5l)$$

T and T_{nom} are in kelvins. The empirical parameter α is found to be exponentially increasing with temperature. L_{effav} is the average sum of the effective channel lengths taken near the Si/SiO₂ interface and at the extreme of the gate depletion region.

It has been found that the space-charge component is not negligible for the quarter-micron devices as it will contribute to a static power dissipation. Fig. 8 illustrates the effect of varying the source-drain bias and temperature on the space-charge current for quarter-micron devices. The source-drain bias has a modulating effect on the space-charge current flow. The temperature increment accelerates thermionic emission, which in turn results in a higher space-charge current flow. Fig. 9 shows that the space-charge current increases more than three decades of current when the temperature increases from

$$\mu_p = 54.3 \left(\frac{T}{T_{nom}} \right)^{-0.57} + \frac{1.36 \times 10^8 T^{-2.23}}{1 + \left[\frac{N_{sub}}{\left(2.35 \times 10^{17} \left\{ \frac{T}{T_{nom}} \right\}^{2.4} \right)} \right] \times 0.88 \times \left(\frac{T}{T_{nom}} \right)^{-0.146}} \quad (5c)$$

Fig. 8. Effect of varying V_{SD} and temperature on the space-charge current of the quarter-micron device.

Fig. 9. Effect of temperature variation on the space-charge current of the quarter-micron device for different V_{SD} .

223 to 398 K. However, a slight decrease in the analytical value of the space-charge current can be observed at room temperature. This is due to the two competing exponential terms in the N_{sub} equation [see (5e) and (5f)]. The intrinsic carrier concentration, increases with temperature, whereas the term $e^{E_F - E_{Fi}/kT}$ decreases with temperature. As a result, there is an unexpected peak in N_{sub} at room temperature. This phenomenon will affect all other current components, as well as the conductances.

V. THE LATERAL BIPOLAR CURRENT MODEL

Under forward source-body bias, high source-drain bias and for very short-channel lengths, lateral bipolar action occurs beneath the channel region [9]. Rofail and Yeo [10] have explained the need to model this secondary current component

and have modeled the lateral bipolar current using a modified transport equation. This model has been extended in the present work to quarter-micron devices and the effect of temperature variations taken into consideration as follows:

$$I_{bipolar} = \frac{q\mu_p V_t P_e A_{bipolar}}{L_e(1-\zeta)} (1 - e^{-(\zeta L_e v_{sat}/D_p)}) \quad (6a)$$

where

$$\zeta = \zeta_1(V_{SB})\zeta_2(T) \frac{V_{SB\text{eff}}}{V_{SD\text{eff}} + 1.6 \times 10^{-9} e^{700/L}} \quad (6b)$$

$$\zeta_1(V_{SB}) = 1 - e^{-12.1(1+(AL_p/l_c))V_{SB\text{eff}}} \quad (6c)$$

$$\zeta_2(T) = 0.755 + 0.245 \{1 - e^{-0.418(6.21 - (T/100))^{2.25}}\}. \quad (6d)$$

T is in kelvins, and L is in micrometers. ζ is a semi-empirical factor encompassing the effects of source-drain and source-body biases, device technology, and temperature. At room temperature, it approaches unity at high source-drain and source-body biases and for shorter channel lengths. When the temperature increases from 223 to 398 K, ζ decreases gradually from the unity asymptote.

Increasing the source-drain bias has a modulating effect on the lateral bipolar current as illustrated in Fig. 10. Fig. 11 shows that the bipolar current increases exponentially with temperature such that at higher temperatures and larger source-body biases, the lateral bipolar current is comparable to the principal MOS current. For $V_{SB} = 0.8$ V and $T = 398$ K, the ratio of the experimental lateral bipolar current to the experimental MOS current is approximately 1/16. This phenomenon can be explained by the fact that an increase in the operating temperature will cause 1) the intrinsic carrier densities to increase, 2) the bandgap energies to decrease, and 3) the carrier mobility to decrease. The first two effects overwhelm the last thus resulting in an overall increase in the lateral bipolar current with temperature. Furthermore, it has been reported in [1] that the injection barrier for holes in a hybrid-mode lateral BJT is given by

$$\psi_{Bh} = \left(V_{bi} - \frac{\Delta E_g}{q} \right) - V_{SB}. \quad (7)$$

Equation (7) suggests that the hole injection barrier in hybrid-mode devices decreases with temperature.

Fig. 12 depicts the effect of temperature coupled with scaling on the lateral bipolar gain, which is defined by

$$\text{Lateral Bipolar Gain} = \frac{I_{bipolar}}{I_{body}}. \quad (8)$$

$I_{bipolar}$ is the collector current of the lateral pnp transistor, whereas I_{body} is the base current. The gain is fractional because of the addition of the p-channel punchthrough implant during the transistor formation. This implant will impede the flow of carriers in the vicinity of the active region by increasing the rate of recombination. However, the implant is necessary to suppress short-channel effects in 0.25- μm CMOS process.

Fig. 10. Effect of variation of V_{SD} on the lateral bipolar current for two different channel lengths and temperature values.

Fig. 12. Effect of temperature variation on the lateral bipolar gain.

Fig. 11. Comparison of the effects of temperature variation on the MOS and lateral bipolar currents of the quarter-micron device for different V_{SB} .

VI. THE MOS CURRENT MODEL

Much work has already been done to model the effect of temperature on the carrier mobility of MOSFET's [21]–[23]. The piecewise MOS current model employed in [10] has been extended to quarter-micron devices with the temperature effects taken into consideration. The recent work on a temperature-dependent MOSFET inversion layer carrier mobility model for device and circuit simulation [24] has been adopted to account for the major scattering mechanisms in the MOSFET inversion layer. This is given by

$$\frac{1}{\mu_{\text{peff}}} = \frac{1}{\mu_1} \left(\frac{10^6}{E_{\text{eff}}} \right)^{\alpha_1} + \frac{1}{\mu_2} \left(\frac{10^6}{E_{\text{eff}}} \right)^{\alpha_2} + \frac{1}{\mu_3} \left(\frac{10^{18}}{N_{\text{sub}}} \right)^{-1} \left(\frac{10^{-12}}{Q_{\text{inv}}} \right)^{\alpha_3} \quad (9a)$$

where

$$E_{\text{eff}} = \frac{1}{\epsilon_{\text{si}}} (Q_{\text{dep}} + \varphi Q_{\text{inv}}) \quad (9b)$$

$$Q_{\text{dep}} = \sqrt{2q\epsilon_{\text{si}}N_{\text{sub}}(\phi_s - V_{\text{SBeff}})} \quad (9c)$$

$$Q_{\text{inv}} = C_{\text{ox}}(V_{\text{SG}} - V_{\text{Teff}}) \quad (9d)$$

$$\varphi = 0.42 - 2.9 \times 10^{-4}T. \quad (9e)$$

T is in kelvins. Fig. 13 demonstrates that a reasonably good agreement between the experimental data and the analytical model of the MOS current has been achieved for a wide range of technology in the triode and saturation regions for temperatures of 223 and 398 K. Fig. 14 illustrates that the MOS current decreases with temperature. In the triode region, devices with channel lengths of 0.25 and 1.0 μm show approximately equal enhancement (2–4 $\mu\text{A/K}$) of the drain current when the temperature reduces from 398 K to 223 K. This is due to the common sensitivity of the carrier mobility to temperature. In the saturation region, although the saturation velocity is relatively insensitive to temperature and has been reported to increase by only 30% [17], the effect of a greater reduction in the electrical channel length of the MOS current, L_d for $L = 0.25 \mu\text{m}$ results in approximately 6 $\mu\text{A/K}$ increase in the MOS current with lower temperature. In retrospect, the gradual decline in the MOS current with temperature can be compensated for by the exponential increase in the lateral bipolar current shown earlier in Fig. 11. At higher temperatures and larger source-body bias, the bipolar current will have approximately the same order of magnitude as the MOS current, thereby complementing the MOS current in enhancing the overall device performance.

VII. THE DEVICE PARAMETERS

A. The Device Transconductance

For a MOSFET operating in a hybrid-mode environment, its device transconductance can be written as

$$\Delta I_{SD} = g_{m1}\Delta V_{SG} + g_{m2}\Delta V_{SB} \quad (10a)$$

Fig. 13. Effect of scaling of channel length on the MOS current for two different V_{SD} , V_{SB} and temperatures.

Fig. 14. Effect of temperature variation on the MOS current for two different V_{SD} and various technologies.

where

$$g_{m1} = \frac{\delta I_{SD}}{\delta V_{SG}} \quad \text{at constant } V_{SB} \text{ and } V_{SD} \quad (10b)$$

$$g_{m2} = \frac{\delta I_{SD}}{\delta V_{SB}} \quad \text{at constant } V_{SG} \text{ and } V_{SD} \quad (10c)$$

$$\frac{\delta I_{SD}}{\delta V_{SG}} = \frac{\delta I_{mos}}{\delta V_{SG}} + \frac{\delta I_{bipolar}}{\delta V_{SG}} + \frac{\delta I_{space}}{\delta V_{SG}} \quad (10d)$$

$$\frac{\delta I_{SD}}{\delta V_{SB}} = \frac{\delta I_{mos}}{\delta V_{SB}} + \frac{\delta I_{bipolar}}{\delta V_{SB}} + \frac{\delta I_{space}}{\delta V_{SB}}. \quad (10e)$$

The expressions for the derivatives are shown in Appendix A.

Fig. 15 shows the effect of temperature on g_{m1} in the triode and saturation regions for $L = 0.25 \mu\text{m}$ and $L = 1.0 \mu\text{m}$. The

plot shows that g_{m1} of the quarter-micron device increases by approximately 2.2 and 1.5 $\mu\text{A/K}$ in the saturation and triode regions respectively, when the temperature reduces from 398 K to 223 K. For $L = 1.0 \mu\text{m}$, the respective rates are 1.5 $\mu\text{A/K}$ and 0.67 $\mu\text{A/K}$. This is in agreement with the explanation stated in the previous section for the variation of the MOS current with temperature.

Fig. 16 illustrates the variation of g_{m2} with temperature. As evident from the graph, g_{m2} in general increases with temperature. Furthermore g_{m2} in the triode region is larger than g_{m2} in the saturation region. This is because in the triode region the output resistance is relatively smaller, hence the drain current has a strong dependence on both the drain and the body potentials. In the saturation region, when the velocity

Fig. 15. Effect of temperature variations on g_{m1} in the triode and saturation regions for $L = 0.25 \mu\text{m}$ and $L = 1.0 \mu\text{m}$.

Fig. 16. Effect of temperature variation on g_{m2} in the triode and saturation regions for $L = 0.25 \mu\text{m}$.

of the carriers start to saturate, this dependence begins to diminish.

B. The Device Output Conductance

The output conductance of a MOSFET operating in a hybrid-mode environment is given by

$$g_{sd} = \frac{\delta I_{SD}}{\delta V_{SD}} \quad \text{at constant } V_{SG} \text{ and } V_{SB} \quad (11a)$$

$$\frac{\delta I_{SD}}{\delta V_{SD}} = \frac{\delta I_{mos}}{\delta V_{SD}} + \frac{\delta I_{bipolar}}{\delta V_{SD}} + \frac{\delta I_{space}}{\delta V_{SD}}. \quad (11b)$$

The expressions for the derivative are shown in Appendix B.

The effect of temperature on g_{sd} in the triode and saturation regions for $L = 0.25 \mu\text{m}$ and $L = 1.0 \mu\text{m}$ is shown in Fig. 17. The results reveal that scaling the channel length to $0.25 \mu\text{m}$ increases the saturation output conductance by approximately 1 order of magnitude. This is due to the nonsaturation of the drain current for the quarter-micron devices and is desirable in digital applications for faster switching. On the other hand, the lowering of temperature brings about very minimal increase in the saturation output conductance for $L = 0.25 \mu\text{m}$.

VIII. CONCLUSIONS

A model has been presented to account for the various short-channel effects and the influence of temperature on pMOS-FET's in a Bi-MOS structure fabricated using the $0.25\text{-}\mu\text{m}$ CMOS process. It caters for a wide range of technologies and biases.

The threshold voltage has been modeled as two components: one which includes short-channel effects and another being the temperature compensation term. The threshold voltage decreases with temperature due to Fermi level shifts. DIBL and forward source-body effects have been found to be weak functions of temperature. The forward source-body effect dominates for $L = 1.0 \mu\text{m}$, whereas both the DIBL effect and the forward source-body effect are comparable for $L = 0.25 \mu\text{m}$. The threshold voltage shifts linearly with temperature. Both the space-charge and the lateral bipolar currents have been found to be direct exponential functions of temperature. On the contrary, the MOS current decreases linearly with temperature. Hence, operating the transistor at higher temperature would mean degrading the MOS current and greater leakage at zero gate bias. On the other hand, elevated temperatures are able to increase the lateral bipolar current to approximately the same order of magnitude as the principal MOS current. For $V_{SB} = 0.8 \text{ V}$ and $T = 398 \text{ K}$, the ratio of the experimental lateral

Fig. 17. Effect of temperature variation on g_{sd} in the triode and saturation regions for $L = 0.25 \mu\text{m}$ and $L = 1.0 \mu\text{m}$.

bipolar current to the experimental MOS current of the quarter-micron device is approximately 1/16. This secondary current component can be utilized to enhance the switching speed of the transistor. In general, the transconductance associated with the variation of the source-gate voltage, and the output conductance, decrease with higher temperature. On the other hand, the transconductance associated with the variation of the source-body voltage, exhibits the opposite trend due to the exponential increase of the lateral bipolar and space-charge currents.

APPENDIX A DEVICE TRANSCONDUCTANCE

$$\frac{\delta I_{\text{mos}}(\text{tri})}{\delta V_{SG}} = I_{\text{mos}}(\text{tri}) \cdot \left\{ X_1 \mu_{\text{peff}} - \frac{2v_{\text{sat}} X_1 V_{SD\text{eff}} L_{\text{eff}}}{\left(1 + \frac{V_{SD\text{eff}}}{E_c L_{\text{eff}}}\right) (E_c L_{\text{eff}})^2} + \frac{1}{V_{SG} - V_{T\text{eff}} - \frac{1}{2} V_{SD\text{eff}}} \right\} \quad (\text{A1})$$

[and see (A2), shown at the top of the next page]

$$X_1 = \frac{\alpha_1}{\mu_1} \left(\frac{10^6}{E_{\text{eff}}} \right)^{\alpha_1 - 1} \left(\frac{C_{\text{ox}} \varphi 10^6}{\epsilon_{\text{si}} E_{\text{eff}}^2} \right) + \frac{\alpha_2}{\mu_2} \left(\frac{10^6}{E_{\text{eff}}} \right)^{\alpha_2 - 1} \cdot \left(\frac{C_{\text{ox}} \varphi 10^6}{\epsilon_{\text{si}} E_{\text{eff}}^2} \right) + \frac{\alpha_3}{\mu_3} \left(\frac{10^{18}}{N_{\text{sub}}} \right)^{-1} \left(\frac{10^{-12}}{Q_{\text{inv}}} \right)^{\alpha_3 - 1} \cdot \left(\frac{C_{\text{ox}} 10^{-12}}{Q_{\text{inv}}^2} \right) \quad (\text{A3})$$

$$\frac{\delta I_{\text{bipolar}}}{\delta V_{SG}} = 0 \quad (\text{A4})$$

$$\frac{\delta I_{\text{space}}}{\delta V_{SG}} = 0 \quad (\text{A5})$$

$$\frac{\delta I_{\text{mos}}(\text{tri})}{\delta V_{SB}} = \frac{I_{\text{mos}}(\text{tri})}{\left(1 + \frac{\Lambda L_p}{l_c}\right) \left(1 + \frac{V_{SD\text{eff}}}{E_c L_{\text{eff}}}\right)} \cdot \left\{ \left(1 + \frac{V_{SD\text{eff}}}{E_c L_{\text{eff}}}\right) \left(\frac{X_2}{\mu_{\text{peff}}} + \frac{\lambda}{1 + \lambda V_{SB\text{eff}}} \right) - \frac{X_3}{V_{SG} - V_{T\text{eff}} - \frac{1}{2} V_{SD\text{eff}}} - \frac{2\nu_{\text{sat}} X_2 V_{SD\text{eff}} L_{\text{eff}}}{(\mu_{\text{peff}} E_c L_{\text{eff}})^2} \right\} \quad (\text{A6})$$

$$X_2 = \left\{ \frac{\alpha_1}{\mu_1} \left(\frac{10^6}{E_{\text{eff}}} \right)^{\alpha_1 - 1} \left(\frac{(X_4 + \varphi X_5) 10^6}{\epsilon_{\text{si}} E_{\text{eff}}^2} \right) + \frac{\alpha_2}{\mu_2} \left(\frac{10^6}{E_{\text{eff}}} \right)^{\alpha_2 - 1} \left(\frac{(X_4 + \varphi X_5) 10^6}{\epsilon_{\text{si}} E_{\text{eff}}^2} \right) + \frac{\alpha_3}{\mu_3} \left(\frac{10^{18}}{N_{\text{sub}}} \right)^{-1} \left(\frac{10^{-12}}{Q_{\text{inv}}} \right)^{\alpha_3 - 1} \times \left(\frac{X_5 10^{-12}}{Q_{\text{inv}}^2} \right) \right\} \times \mu_{\text{peff}}^2 \quad (\text{A7})$$

$$X_3 = TC_2 \left(\frac{T}{T_{\text{nom}}} - 1 \right) - \gamma + V_{SB\text{eff}} e^{-50L} \left(1 + \frac{\Lambda L_p}{l_c} \right) \quad (\text{A8})$$

$$X_4 = \frac{-q \epsilon_{\text{si}} N_{\text{sub}}}{Q_{\text{dep}}} \quad (\text{A9})$$

$$\frac{\delta I_{\text{mos}}(\text{sat})}{\delta V_{SG}} = I_{\text{mos}}(\text{sat}) \left\{ \frac{(V_{SG} - V_{\text{Teff}}) \left(1 + \frac{E_c L_d}{V_{SG} - V_{\text{Teff}}} + 2\nu_{\text{sat}} X_1 L_d \right) + E_c L_d}{(V_{SG} - V_{\text{Teff}})^2 \left(1 + \frac{E_c L_d}{V_{SG} - V_{\text{Teff}}} \right)} \right\} \quad (\text{A2})$$

$$\begin{aligned} \frac{\delta I_{\text{mos}}(\text{sat})}{\delta V_{SB}} = & \frac{I_{\text{mos}}(\text{sat})}{\left(1 + \frac{\Lambda L_p}{l_c} \right) \left(1 + \frac{E_c L_d}{V_{SG} - V_{\text{Teff}}} \right)} \left\{ \left(1 + \frac{E_c L_d}{V_{SG} - V_{\text{Teff}}} \right) \left(\frac{\lambda}{1 + \lambda V_{SB\text{eff}}} - \frac{X_3}{V_{SG} - V_{\text{Teff}}} \right) \right. \\ & \left. - \frac{(V_{SG} - V_{\text{Teff}}) \left(\frac{E_c \epsilon_{\text{si}}}{q N_{\text{sub}} X_{dm}} - \frac{2\nu_{\text{sat}} X_2 L_d}{\mu_{\text{peff}}^2} \right) + E_c L_d X_3}{(V_{SG} - V_{\text{Teff}})^2} \right\} \end{aligned} \quad (\text{A11})$$

$$X_5 = C_{\text{ox}} \left\{ \gamma - V_{SB\text{eff}} e^{-50L} \left(1 + \frac{\Lambda L_p}{l_c} \right) - TC_2 \left(\frac{T}{T_{\text{nom}}} - 1 \right) \right\} \quad (\text{A10})$$

$$X_d^* = X_d \left(1 + \frac{I_s R_{\text{well}}}{n_f V_t} e^{V_{j2}/n_f V_t} \right) \quad (\text{A16})$$

$$\frac{\delta I_{\text{space}}}{\delta V_{SB}} = 0. \quad (\text{A17})$$

[see (A11) above]

$$\frac{\delta I_{\text{bipolar}}}{\delta V_{SB}} = \frac{I_{\text{bipolar}}}{1 + \frac{\Lambda L_p}{l_c}} \left(X_6 - \frac{X_7}{L_e(1 - \varsigma)} \right) \quad (\text{A12})$$

$$\begin{aligned} X_6 = & \frac{\nu_{\text{sat}} \varsigma e^{-(\varsigma L_e \nu_{\text{sat}}/D_p)}}{D_p(1 - e^{-(\varsigma L_e \nu_{\text{sat}}/D_p)})} \\ & \cdot \left\{ \frac{12.1 L_e e^{-12.1(1 + (\Lambda L_p/l_c))V_{SB\text{eff}}}}{\varsigma_1(V_{SB})} \left(1 + \frac{\Lambda L_p}{l_c} \right) \right. \\ & \left. + \frac{\epsilon_{\text{si}}}{q N_{\text{sub}}} \left(\frac{1}{X_s^*} + \frac{1}{X_d^*} \right) \right\} + \frac{1}{n_f V_t} \\ & \cdot \frac{1}{1 + \frac{I_s R_{\text{well}}}{n_f V_t} e^{V_{j1}/n_f V_t}} \end{aligned} \quad (\text{A13})$$

$$\begin{aligned} X_7 = & \frac{\epsilon_{\text{si}}(1 - \varsigma)}{q N_{\text{sub}}} \left(\frac{1}{X_s^*} + \frac{1}{X_d^*} \right) - \varsigma L_e \left(1 + \frac{\Lambda L_p}{l_c} \right) \\ & \cdot \left(\frac{12.1 e^{-12.1(1 + (\Lambda L_p/l_c))V_{SB\text{eff}}}}{\varsigma_1(V_{SB})} \right) \end{aligned} \quad (\text{A14})$$

$$X_s^* = X_s \left(1 + \frac{I_s R_{\text{well}}}{n_f V_t} e^{V_{j1}/n_f V_t} \right) \quad (\text{A15})$$

APPENDIX B

DEVICE OUTPUT CONDUCTANCE

$$\begin{aligned} \frac{\delta I_{\text{mos}}(\text{tri})}{\delta V_{SD}} = & \frac{I_{\text{mos}}(\text{tri})}{\left(1 + \frac{\Lambda L_p}{l_c} \right) \left(1 + \frac{V_{SD\text{eff}}}{E_c L_{\text{eff}}} \right)} \\ & \cdot \left\{ \left(1 + \frac{V_{SD\text{eff}}}{E_c L_{\text{eff}}} \right) (\eta C_{\text{ox}} \mu_{\text{peff}} X_8 \right. \\ & \left. + \frac{\eta - \frac{1}{2}}{V_{SG} - V_{\text{Teff}} - \frac{1}{2} V_{SD\text{eff}}} + \frac{1}{V_{SD\text{eff}}}) \right. \\ & \left. - \frac{2\nu_{\text{sat}} \eta C_{\text{ox}} X_8 V_{SD\text{eff}} L_{\text{eff}} + E_c L_{\text{eff}}}{(E_c L_{\text{eff}})^2} \right\} \end{aligned} \quad (\text{B1})$$

$$\begin{aligned} X_8 = & \frac{\alpha_1}{\mu_1} \left(\frac{10^6}{E_{\text{eff}}} \right)^{\alpha_1 - 1} \left(\frac{\varphi 10^6}{\epsilon_{\text{si}} E_{\text{eff}}^2} \right) + \frac{\alpha_2}{\mu_2} \left(\frac{10^6}{E_{\text{eff}}} \right)^{\alpha_2 - 1} \\ & \cdot \left(\frac{\varphi 10^6}{\epsilon_{\text{si}} E_{\text{eff}}^2} \right) + \frac{\alpha_3}{\mu_3} \left(\frac{10^{18}}{N_{\text{sub}}} \right)^{-1} \left(\frac{10^{-12}}{Q_{\text{inv}}} \right)^{\alpha_3 - 1} \\ & \cdot \left(\frac{10^{-12}}{Q_{\text{inv}}^2} \right) \end{aligned} \quad (\text{B2})$$

[see (B3) at the bottom of the page]

$$\begin{aligned} \frac{\delta I_{\text{mos}}(\text{sat})}{\delta V_{SD}} = & \frac{I_{\text{mos}}(\text{sat})}{\left(1 + \frac{\Lambda L_p}{l_c} \right) \left(1 + \frac{E_c L_d}{V_{SG} - V_{\text{Teff}}} \right)} \left\{ \left(1 + \frac{E_c L_d}{V_{SG} - V_{\text{Teff}}} \right) \left(\frac{\eta}{V_{SG} - V_{\text{Teff}}} \right) \right. \\ & \left. + \frac{(V_{SG} - V_{\text{Teff}}) \left(\frac{E_c \epsilon_{\text{si}}}{q N_{\text{sub}} X_{dm}} + 2\nu_{\text{sat}} \eta C_{\text{ox}} X_8 L_d \right) + E_c L_d \eta}{(V_{SG} - V_{\text{Teff}})^2} \right\} \end{aligned} \quad (\text{B3})$$

$$\frac{\delta I_{\text{bipolar}}}{\delta V_{SD}} = \frac{I_{\text{bipolar}}}{1 + \frac{\Lambda L_p}{l_c}} \cdot \left(\frac{X_9 \nu_{\text{sat}} e^{-(\zeta L_e \nu_{\text{sat}}/D_p)}}{D_p(1 - e^{-(\zeta L_e \nu_{\text{sat}}/D_p)})} + \frac{X_{10}}{L_e(1 - \delta)} \right) \quad (\text{B4})$$

$$X_9 = \zeta_1(V_{SB})\zeta_2(T)L_e \left\{ \frac{1}{V_{SD\text{eff}} + 1.6 \times 10^{-9}e^{700L}} - \frac{V_{SD\text{eff}}}{(V_{SD\text{eff}} + 1.6 \times 10^{-9}e^{700L})^2} \right\} - \frac{\epsilon_{\text{si}}\zeta}{qN_{\text{sub}}X_d^*} \quad (\text{B5})$$

$$X_{10} = \frac{\epsilon_{\text{si}}(1 - \zeta)}{qN_{\text{sub}}X_d^*} + \zeta_1(V_{SB})\zeta_2(T)L_e \cdot \left\{ \frac{1}{V_{SD\text{eff}} + 1.6 \times 10^{-9}e^{700L}} - \frac{V_{SD\text{eff}}}{(V_{SD\text{eff}} + 1.6 \times 10^{-9}e^{700L})^2} \right\} \quad (\text{B6})$$

$$\frac{\delta I_{\text{space}}}{\delta V_{SD}} = \frac{2I_{\text{space}}}{V_{SD\text{eff}} \left(1 + \frac{\Lambda L_p}{l_c} \right)} \quad \text{for} \quad \frac{\mu_p V_{SD\text{eff}}}{L_{\text{effav}}} < \nu_{\text{sat}} \quad (\text{B7a})$$

$$\frac{\delta I_{\text{space}}}{\delta V_{SD}} = \frac{I_{\text{space}}}{V_{SD\text{eff}} \left(1 + \frac{\Lambda L_p}{l_c} \right)} \quad \text{for} \quad \frac{\mu_p V_{SD\text{eff}}}{L_{\text{effav}}} \geq \nu_{\text{sat}}. \quad (\text{B7b})$$

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