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A Charge-Trapping-Based Technique to Design Low-Voltage BiCMOS Logic Circuits

Yeo Kiat Seng and Samir S. Rofail

***Abstract*— New BiCMOS logic circuits employing a charge trapping technique are presented. The circuits include an XOR gate and an adder. Submicrometer technologies are used in the simulation and the circuits' performances are comparatively evaluated with the CMOS and that of the recently reported circuits. The proposed circuits were fabricated using a standard 0.8-μm BiCMOS process. The experimental results obtained from the fabricated chip have verified the functionality of the proposed logic gates.**

***Index Terms*—BiCMOS digital circuit design, fabrication, simulation.**

I. Introduction

THE technology for BiCMOS has matured over the last decade, and now it is one of the dominant technologies used for high-speed, low-power, and highly functional very large scale integration (VLSI) circuits [1], [2]. However, the design of high-performance logic circuits and systems for low-voltage applications is still lagging.

It is a well-known fact that in the reduced supply voltage environment, the conventional BiCMOS logic circuits start to lose the leverage over the CMOS logic circuits. The degradation in performance is due to the increase in the propagation delay [3], [4] and the decrease in the output voltage swing [5]. It has also been reported that, as the supply voltage is scaled down, the pull-down delay time of the conventional BiCMOS circuit constitutes a large percentage of the propagation delay [6].

Many attempts have been made in the past to alleviate these degradation effects. Complementary BiCMOS has been proposed as an alternative to achieve full swing [7], [8]. However, it is based on the high cost of complementary BiCMOS technology. Lowering the threshold voltage of the NMOSFET down to 0 V, proposed in [6], would result in increasing the leakage current, thereby making the circuit unacceptable from the system's perspective. Although the circuit reported in [9] demonstrates a better performance as compared to the conventional BiCMOS logic gate, its design demands a twin-tub BiCMOS process. "Transient saturation" has been introduced in [8] to achieve full-swing and high speed at 1.5-V operation. The same technique has been adopted to design the bootstrapped full-swing BiCMOS circuit (BFBiCMOS) [10] in an attempt to improve the circuit performance over a wide range of supply voltages (1.2–3.3 V). However, these circuits have used a large number of devices and, therefore, tend to consume a relatively large power especially for supplies greater than 2 V.

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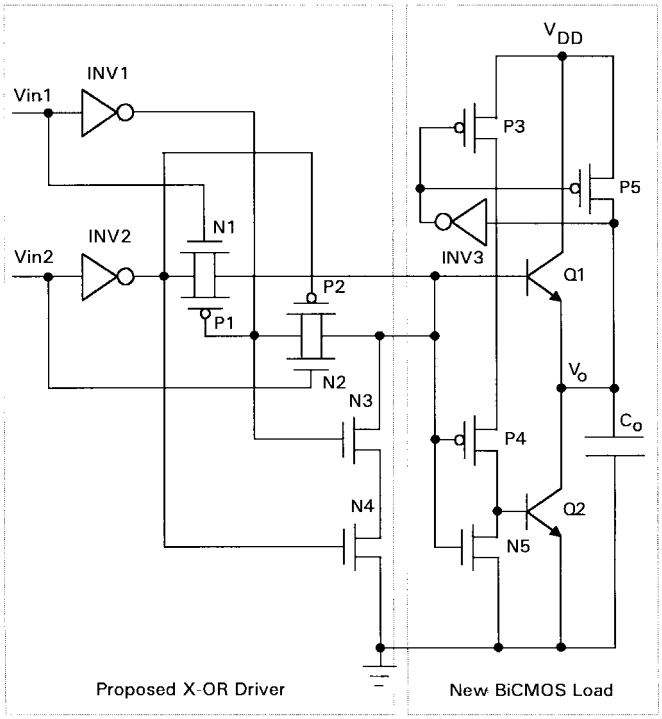


Fig. 1. The new BiCMOS XOR circuit.

In this paper, an innovative approach is adopted to develop new circuits and configurations for low-voltage applications. Section II describes the operation of the new XOR gate. The performance comparison of four XOR logic circuits (new BiCMOS, BFBiCMOS [10], MBiCMOS [11], and CMOS), and the experimental results of the proposed XOR gate are also given in the same section. Section III highlights the new BiCMOS adder as derived from the new XOR circuit configuration.

II. A New BiCMOS XOR Logic Circuit

The new BiCMOS XOR circuit, shown in Fig. 1, comprises two stages: a CMOS XOR driver and a BiCMOS load. The proposed CMOS XOR driver, made up of inverters and transmission gates, outperforms the standard CMOS configuration [12], illustrated in Fig. 2, for convenience in two main aspects: i) for the same area, the new circuit has a smaller input capacitance, and ii) since it can source/sink a larger current, the new circuit offers higher speeds than the conventional CMOS circuit.

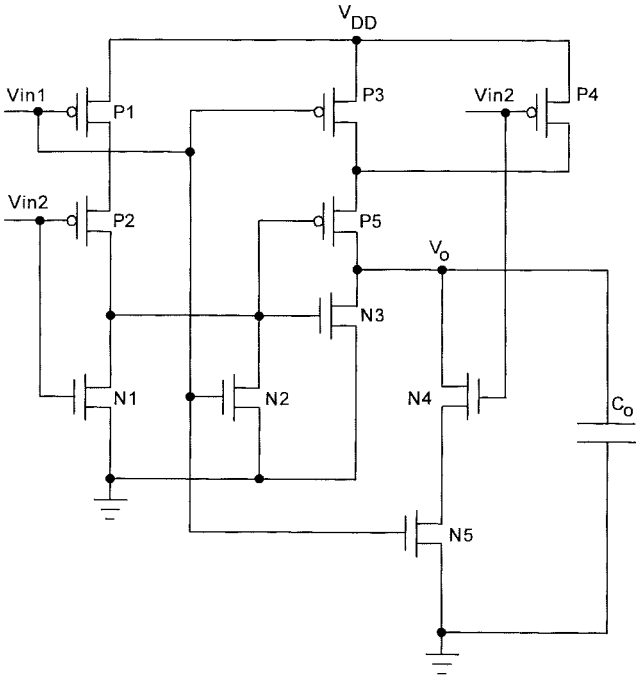


Fig. 2. The conventional CMOS XOR circuit [12].

A. Circuit Operation

Referring to Fig. 1, in the pull-up operation, Q_1 turns ON. The high base voltage of Q_1 forces N_5 to turn ON and deplete the base charge of Q_2. The high voltage established at the base of Q_1 also prevents P_4 from conducting. The rising output voltage sends a transition through the feedback inverter INV3, causing the conduction of P_5. In the pull-down phase, Q_1 is depleted through N_3 and N_4 when the inputs V_{in1} and V_{in2} are LOW, and through the transmission gates N_1P_1 and N_2P_2 when they are HIGH. At the same time, P_4 conducts, driving Q_2 first in the active region before saturating it at a later stage. P_3 turns ON as long as the output voltage maintains its high level. However, during the pull-down phase, the decrease in the output voltage turns P_3 OFF gradually. The excess minority charge, trapped in the base of Q_2, will continue to drive Q_2 in the saturation region and the output voltage decreases further.

B. Comparative Evaluation

In this section, four XOR logic circuits will be evaluated in terms of the propagation delay, the output voltage swing, and the average power consumption. These are: the CMOS (new XOR driver in series with an optimized two-stage CMOS [13] buffer), the MBiCMOS (new XOR driver in series with the MBiCMOS load), the BFBiCMOS (new XOR driver in series with the BFBiCMOS load), and the proposed BiCMOS (new XOR driver in series with the new BiCMOS load) XOR circuits. The comparison is performed for a ramp input of 200 ps rise time and based on an area ratio of 1:1:2:1 for the CMOS, MBiCMOS, BFBiCMOS, and the new XOR circuits, respectively. The large area allocated to the BFBiCMOS is necessary to accommodate its large number of devices used. The key MOS and bipolar junction transistor (BJT) process parameters, extracted from a real technology, are shown in Tables I and II, respectively.

TABLE I
TECHNOLOGY FILE FOR MOSFET'S

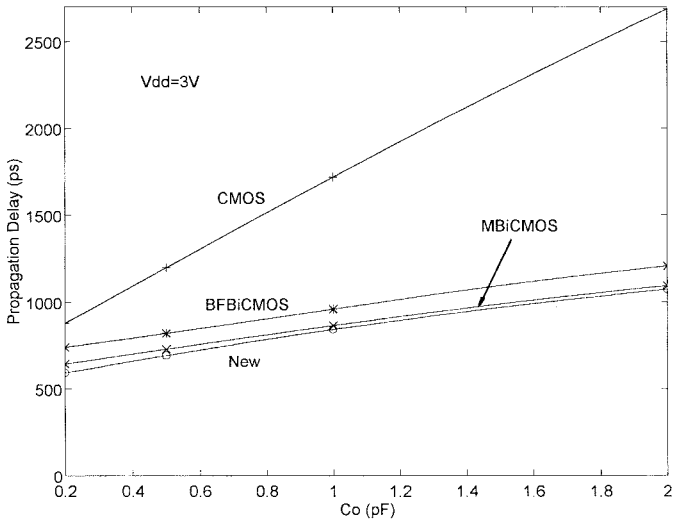
Technology		(3V, 0.8μm)	
Parameters	**Units**	**NMOS**	**PMOS**
V_T	V	0.7500	-0.750
T_{OX}	nm	15.000	15.000
R_{shm}	ohm/sq	25.000	45.000
C_{jw}	pF/m	220.00	220.00
C_{jm}	$\mu F/m^2$	300.00	450.00
C_{gdom}	pF/m	350.00	350.00
C_{gsom}	pF/m	350.00	350.00
C_{gbom}	pF/m	150.00	150.00

TABLE II
TECHNOLOGY FILE FOR BJT

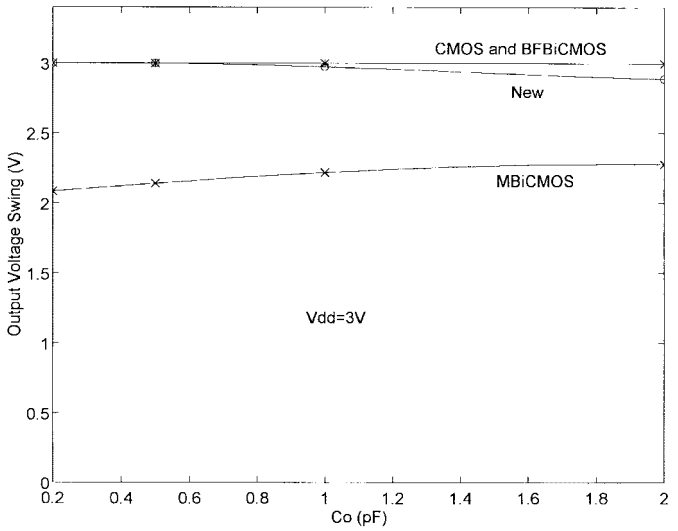
Technology		(3V, 0.8μm)
Parameters	**Units**	**NPN**
β	-	115.000
I_K	mA	1.70000
T_f	ps	11.0000
R_C	ohm	330.000
R_E	ohm	37.0000
R_B	ohm	2000.00
C_{je}	fF	4.00000
C_{jc}	fF	4.00000
C_{js}	fF	12.0000

Fig. 3(a)–(c) illustrates the performance of the circuits for different load capacitances and at a supply voltage of 3 V. The new circuit offers the best output voltage swing and propagation delay combination. Although the MBiCMOS XOR circuit has also a low propagation delay, this has been achieved at the expense of a smaller output voltage swing. From the system's perspective, a small output voltage swing is unsuitable for the design of buffer chains [13]. As for the CMOS XOR circuit, its high propagation delay makes it undesirable to drive heavy loads. As depicted from Fig. 3(c), the new circuit consumes only slightly more power than the CMOS circuit.

In Fig. 4, the propagation delay of the XOR circuits, under comparison, is evaluated as the technology is scaled down from (3 V, 0.8 μm) to (2 V, 0.5 μm). Besides scaling the supply voltage, the emitter areas of the bipolar devices, and the channel lengths and widths of the MOS transistors, the other key device parameters such as I_K, τ_f, β, V_T, and T_{OX} have been scaled according to [5]. As shown in Fig. 4, the new



(a)



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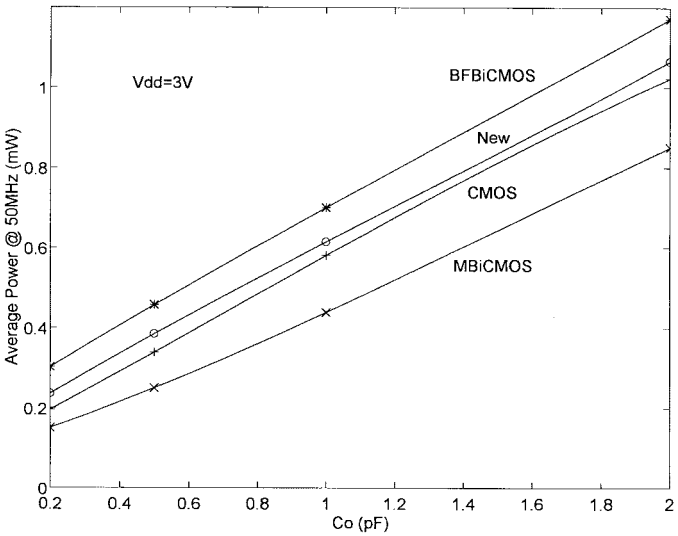

(c)

Fig. 3. The performance comparison of various XOR gates at (3 V, 0.8 μm) technology: (a) propagation delay, (b) voltage swing, and (c) average power dissipation.

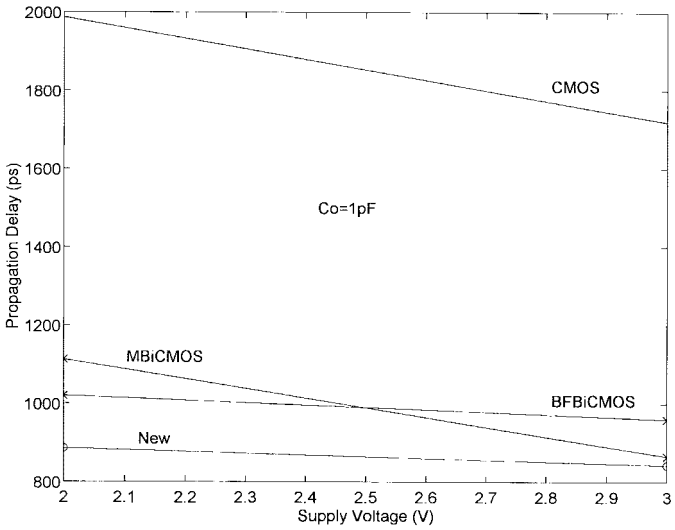

Fig. 4. The propagation delay of various XOR circuits against the supply voltage for scaled technologies.

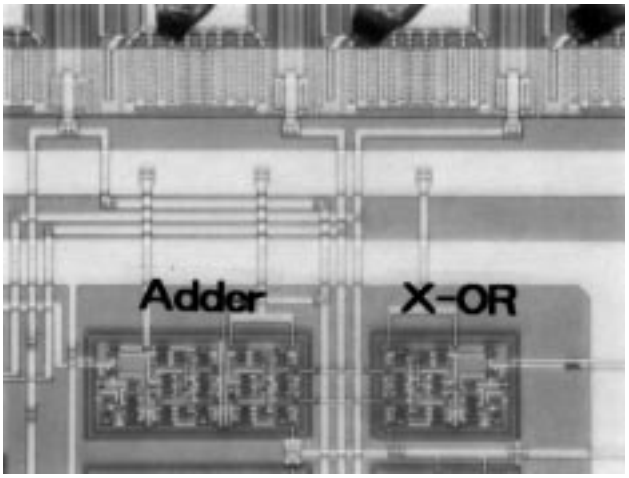

Fig. 5. The photomicrograph of the XOR and adder circuits.

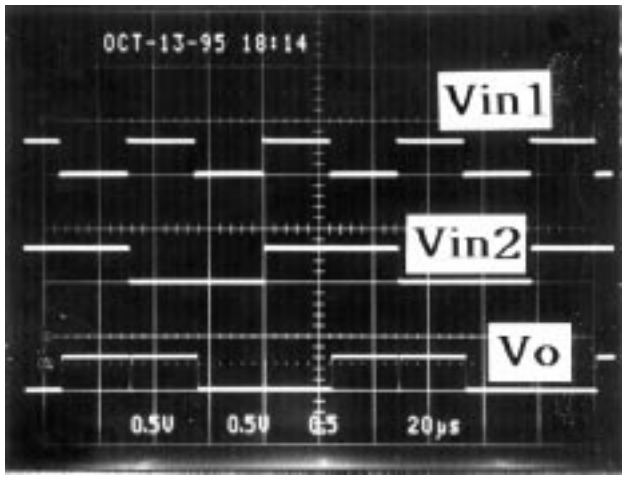

Fig. 6. The input and output waveforms of the XOR gate. (Horizontal scale: 20 μs/div., vertical scale: 5 V/div.)

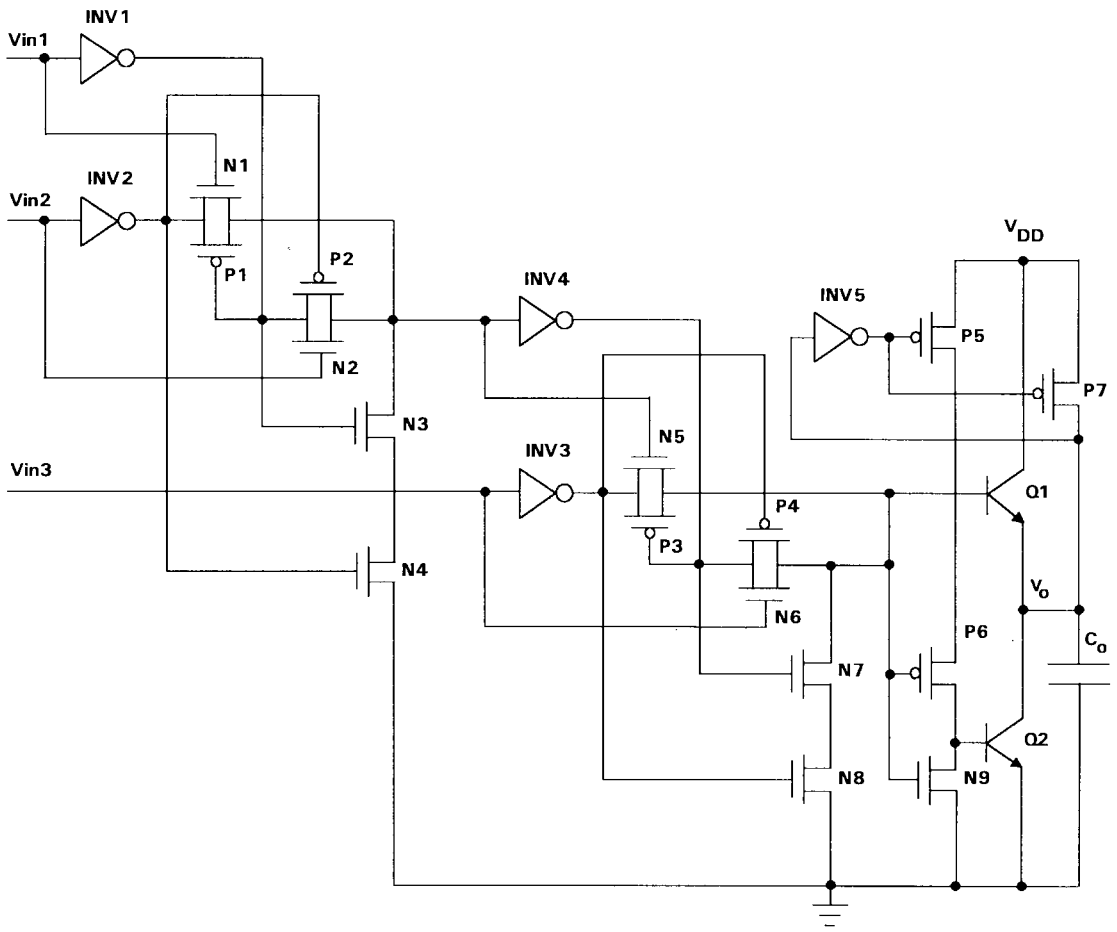

Fig. 7. The new BiCMOS adder.

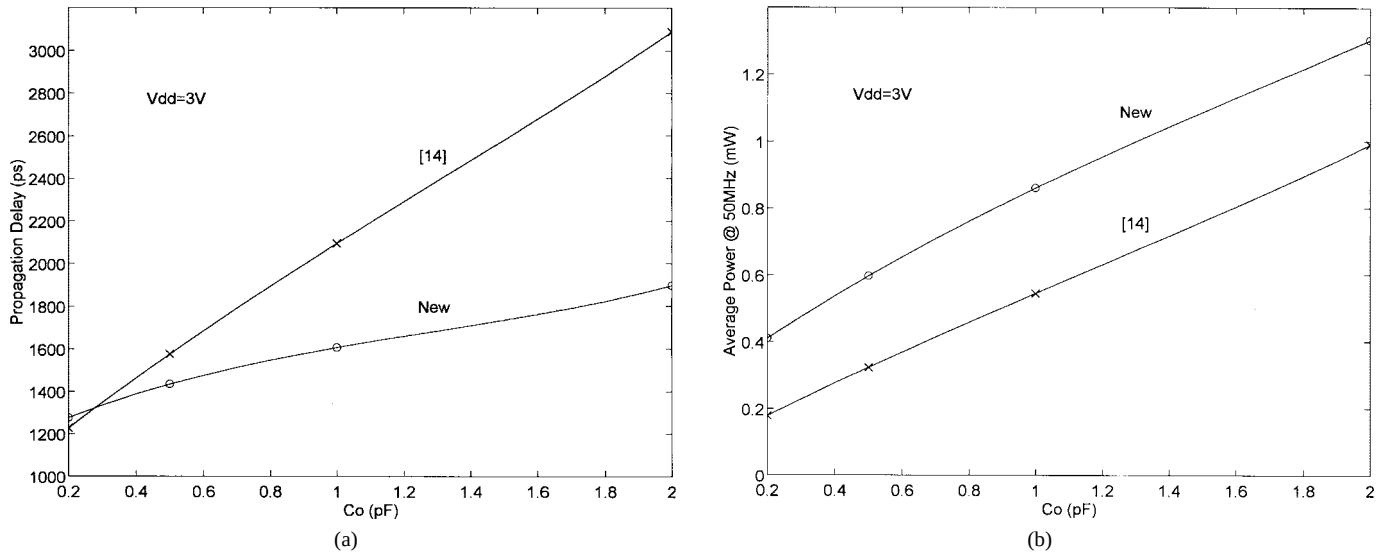

Fig. 8. The performance of the proposed adder as compared to [14] at (3 V, 0.8 μm) technology: (a) propagation delay and (b) average power dissipation.

circuit maintains its superiority at lower supply voltages with its propagation delay increasing very slightly as the technology is scaled down.

C. Experimental Results

The proposed BiCMOS XOR logic circuit has been fabricated using a standard 0.8-μm, n-well/p-substrate, double-polysilicon double-metal BiCMOS process. Fig. 5 shows the photomicrograph of the fabricated chip. In designing the circuit layout, the device size, orientation, and proximity have been considered. A supply voltage of 3 V was used to verify the circuit operation. Fig. 6 shows that for a given input condition, a correct output logical state can be obtained. With square wave inputs V_{in1} and V_{in2} of frequencies 10 and 20 kHz,

respectively, and equal input amplitudes of 3 V_{pp}, an output voltage swing of 3 V_{pp} is achieved for a load capacitance of 1 pF (using a 10 : 1 measuring probe).

III. A New BiCMOS Adder

The concept used in designing the proposed BiCMOS XOR circuit shown in Fig. 1 has been extended to implement the BiCMOS adder circuit shown in Fig. 7. The proposed adder circuit was fabricated using a standard 0.8-μm BiCMOS process and its photomicrograph is shown in Fig. 5. The new adder circuit is compared to [14] based on equal chip area and simulated for a ramp input of 200 ps rise time.

Fig. 8(a) and (b) shows the propagation delay and the average power dissipation for different load capacitances. As depicted from the results, the new circuit outperforms [14] in terms of speed. The speed improvement is even more significant at higher loads. However, the new circuit consumes slightly more power than [14]. The full-swing performance (not shown) of both circuits is sustained over a wide range of capacitance loadings.

IV. Conclusions

New low-voltage BiCMOS XOR and adder circuits are presented. The design is based on the charge trapping technique to achieve high speeds and full output voltage swings. The HSPICE results have verified the superiority of these new logic circuits over the previously reported BiCMOS and CMOS circuits. The new logic gates were fabricated using a standard 0.8-μm noncomplementary BiCMOS process. The experimental results obtained from the fabricated chip have confirmed the operation of these new logic gates.

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