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An Area Efficient High Turn Ratio Monolithic Transformer for Silicon RFIC

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Abstract — **A novel way of manufacturing an on-chip transformer that produces high inductance ratio ($L_{Sec}/L_{Pri} > 30$) with excellent area efficiency is presented. This technique uses an electrical all-round coupling effect of a conductor A (Primary Coil), having large effective width, and a densely routed conductor B (Secondary Coil). Thus, a high turn ratio monolithic transformer, using minimum die size, is realizable on silicon. The coil having the dense routing can also be doubled up as a monolithic RF choke on silicon. In this work, area efficiency is compared between various type of existing transformer structures (i.e. Interleaved and Stacked transformer), based on unit inductance. The method presented is fully compatible to all the foundry standard CMOS processes.**

Index Terms — **High Turn Ratio transformer, Coupling coefficient, Interleaved transformer, Stacked transformer, Inductance Ratio, RFCMOS, Vertical Deck, SoC.**

I. INTRODUCTION

The high demand for System-on-Chip on silicon, promotes the interest of integrating the on-chip transformers for RFCMOS applications. Due to the physical isolation property, transformers are profitably exploited in low-power circuits for impedance matching to achieve maximum power transfer, voltage step-up or step-down, low-noise feedback and DC isolation of two circuits while maintaining AC continuity.[1]-[3]. In recent years, on-chip transformers have become a spotlight in high frequency applications. This is mainly because many RFIC designers started to introduce transformer as part of the RF fundamental circuitry (i.e. VCO, PAs etc) [4]-[6]. Majority of the work done had shown significant improvement in circuit performance than that of a non-transformer integrated design. In general, the key advantage of using transformer is the ability to reduce the large silicon area consumption by as high as 50%. This reduction has become a figure-of-merit, as silicon area is a limiting factor in current and future RFIC design.

Commonly, there are two main types of transformer configuration (i.e., interleaved and stacked transformer) widely

used. In general, the inductance ratio of the existing monolithic transformers is usually limited to < 10 as the silicon area required is too large for SoC applications. The needs for high inductive devices have been identified in tuned amplifiers and mixers with high intermediate frequencies (IFs). In these applications, high equivalent parallel resistance is required to achieve high conversion gain. The equivalent parallel resistance is governed by the product of Q-factor and inductance value ($Rp = Q * \omega L$), the Q-factor of the on-chip inductor is generally not > 10. Thus, maximizing the inductance value is a common practice for high conversion gain design. Alireza et. al has proposed a technique to create high inductance inductor and transformer.[7] However, the unit inductance ($pH/\mu m^2$) of the reported transformer design is not as efficient as its inductor design, it is because the primary winding is inserted in-between the secondary winding, which degrades the secondary coil's intensive self-inductance effect.

In this work, a novel monolithic high turn ratio transformer is proposed. The proposed design demonstrates excellent performance in terms of area efficiency, coil impedance and inductance ratio. The design is able to achieve a large dynamic range of inductance ratio (as high as > 30), through simple design manipulation. This dedicated option offers high degree of selectivity that is important for customized RFIC designs. The paper is organized in the following four sections. In Section II, the detail introduction for the proposed design is discussed. In Section III, the measured device parameters are presented and discussed. The device reported is fabricated based on Chartered Semiconductor Manufacturing's 0.13μm technology node. Finally, the conclusion is drawn in Section IV.

II. HIGH TURN RATIO TRANSFORMER

A. Description

The proposed high turn ratio transformer has its concept evolved from a bundle cable as shown in Fig. 1. The primary coil of the proposed design forms the external conductor (A) that encloses the internal conductor (secondary coil, B) entirely. This enclosure method is expected to enhance the electrical coupling factor significantly. The proposed structure consists of two main components (i.e. Primary and Secondary) as depicted in Fig. 2.
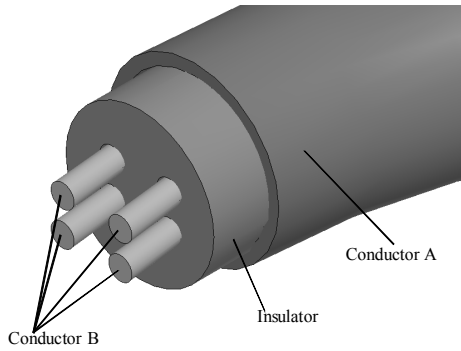
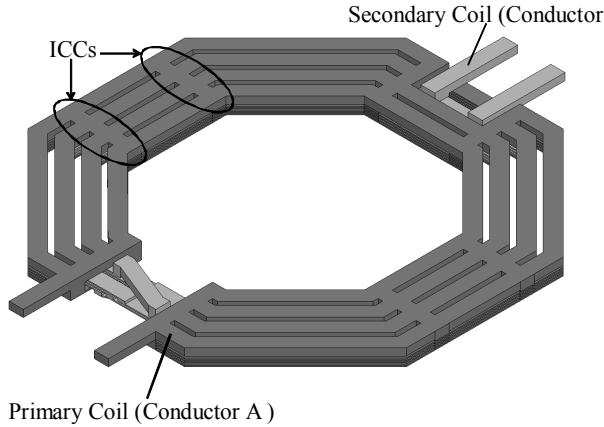Fig. 1: The concept of the proposed transformer design.

Fig. 2: 3D View of the proposed transformer design.

The primary component employs the inter-coil connection (ICC) that aims to reduce the winding effective inductance and resistance value. The design is not restricted by the number of ICCs used. (i.e. this proposed design uses 16 ICCs but the designer can opt to increase the number of ICCs to further lower the coil resistance or reduce the number of ICCs for simplicity.) In fact, a coil with physically wide width is an ideal implementation for this concept. However, the large metal layer coverage will translate to manufacturing Chemical Mechanical Polishing (CMP) dishing issue. This is particularly crucial, as the process problem will result in poor yielding and poor device's reliability. With the use of ICC, the process problem can be addressed by keeping a distance (turn spacing) in-between the coil that is filled with SiO_2. In Fig. 3b), the cross-sectional view of the proposed primary component demonstrates the best resemble of the all-round coupling concept. For the secondary component, Fig. 4 is extracted and expanded from Fig. 2 for a better pictorial explanation. Fig. 4a) demonstrates a systematic way of routing that creates an intensive self-inductance effect. Instead of the conventional way of routing multiple turns per layer, the proposed technique routes the design using multiple layers per turn. For this technique to work, the proposed design must fulfill the condition that the direction of the current flow does not travel in opposite direction within the secondary component as illustrated by the dotted line in Fig. 4a). This is critical, as any reverse current will result in negative self-inductance effect that substantially reduces the overall inductance. Based on this

unique routing method, the degree of inductance selectivity has also been enhanced. This is because any of the intermittent segment(s) can be removed, customizing to designers needs. (i.e In Fig. 4b), segment 1-6 can be selectively removed for inductance optimization, without disturbing the physical structure) Together with the inner diameter (ID) and the conductor width (W) parameters, this proposed design can perform a large dynamic optimization range. Fig. 5 shows the die photo of the proposed transformer design based on Chartered Semiconductor Manufacturing's 0.13μm technology node.
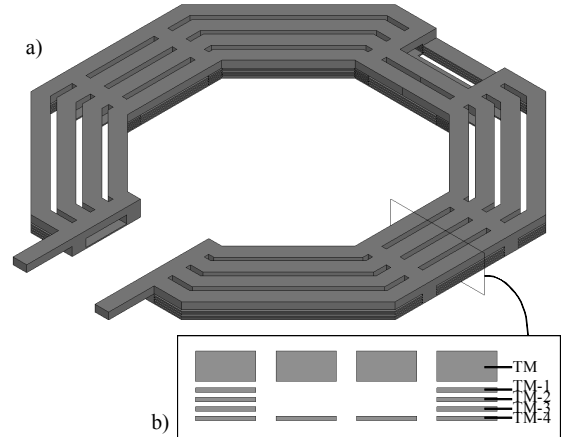

Fig. 3: a) isolated primary component of the proposed design and the b) Cross-sectional view of the primary component.
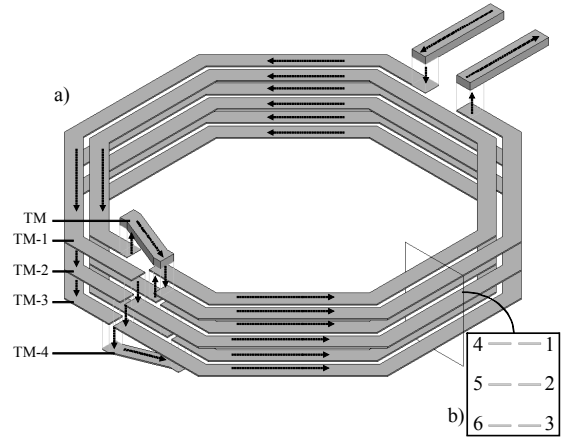

Fig. 4: Expanded 3D view of the a) isolated secondary component of the proposed design and the b) Cross-sectional view of the secondary component.

III. EXPERIMENTAL

The following measurement data is obtained using Agilent E8364B PNA Network Analyzer and Physical Layer Test System (PLTS).

1. Inductance and Inductance ratio: The existing transformer designs are studied in this section to demonstrate that the proposed design is able to yield excellent area efficiency, for a specific area (160 by 160 μm).
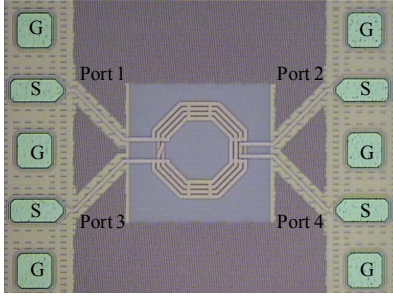
168

Fig. 5: The die photo of the proposed transformer design.
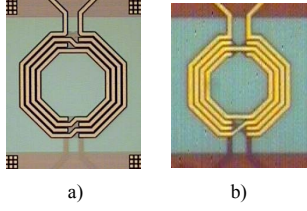

a)   b)

Fig. 6: The die photo of the a) Stacked and b) Interleaved configuration.

Fig. 6 illustrates the die photos of the a) stacked and b) interleaved transformer configurations. In this work, all the configurations will be standardized to octagonal shape. From the manufacturer's point of view, octagonal shape is a polygonal shape that is of a form closest to a circle, which does not violate any design rule. The inductance of the respectively design is extracted (1) and tabulated in Table I.

$$L = \frac{imag(1/Y_{11})}{2*\pi*f} \qquad (1)$$

In the last column of Table I, the inductance per unit silicon area shows that the proposed design has the best area efficiency among the 3 structures.

TABLE I: Inductance of the various transformer design

Design	Inductance (nH)	Unit Inductance (pH/μm^2)
Stacked Transformer	3.295	0.1287
Interleaved Transformer	0.91	0.0355
Proposed HETR Transformer	8.07	0.3152

Certainly, this design can be doubled up as a monolithic RF choke implementation. The inductance plot of the proposed design's primary and secondary coil is shown in Fig. 7. The inductance ratio for this proposed design is $L_{Sec}/L_{Pri} = 33.625$. In fact, the true formula for the turn ratio is (2). Thus, the effective turn ratio of the proposed design should be $\sqrt{33.625} = 5.8$.

$$\text{Turn ratio} = \sqrt{\frac{L_{sec}}{L_{pri}}} \qquad (2)$$

2. Impedance of the proposed design: The real impedance plot of the proposed transformer is extracted from (3) and illustrated in Fig. 8.

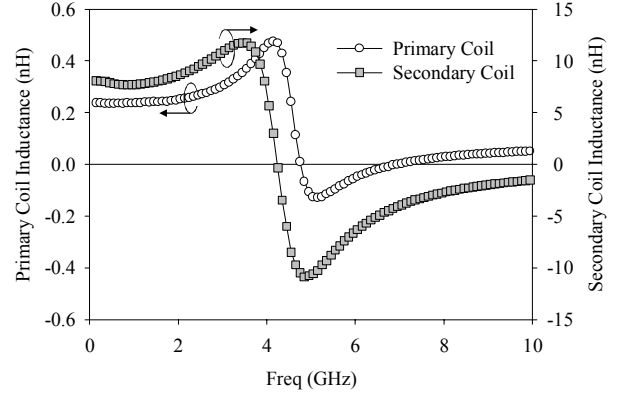$$Z_{in} = \text{real} (1/Y_{11}) \qquad (3)$$

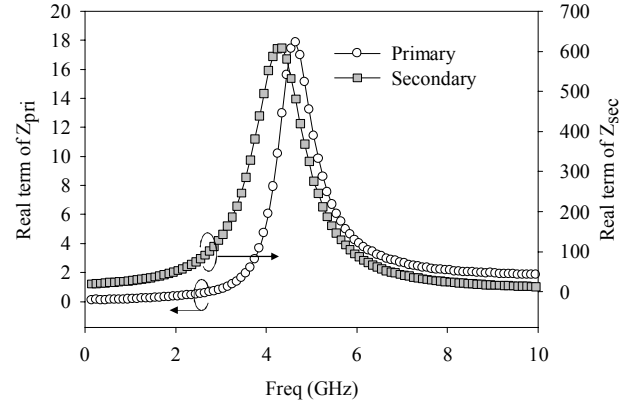Fig. 7: The inductance plot of the proposed transformer design.

Fig. 8: The real term of the input impedance of the proposed transformer.

The ICCs described in Fig. 2 has widened the overall conductor width of the primary coil. The inter-layers (vias) that aids in forming the hollow primary component (Fig. 3b)) have also increased the effective thickness of the coil. Based on the simplest sheet resistance formula (4), the increment in the effective conductor width and thickness, reduces the parasitic resistance significantly. As a result, the measured series resistances of the primary coil shown in Fig. 8 display a much smaller value than the secondary coil. Based on the Table II, the main contributor to the parasitic resistance for the secondary coil is layer 2 to layer 5 (i.e. TM-4 to TM-1), which has the thinnest dimension. With this knowledge, the designers can remove any undesirable segment(s) (reducing the overall length of the conductor in (4)) to optimize the device's

$$R = \rho * \frac{length}{width * thickness} \qquad (4)$$

parasitic resistance to his requirement. The measured impedance ratio of the high turn ratio transformer is $\sqrt{|Z_{sec}|/|Z_{pri}|} = 60.177$.

3. Q-factor: On the other hand, the drawback of the secondary coil high parasitic resistance value is the degradation of the quality factor as depicted in Fig. 9.

169

TABLE II: The back-end vertical metallization profile of the 0.13μm technology node

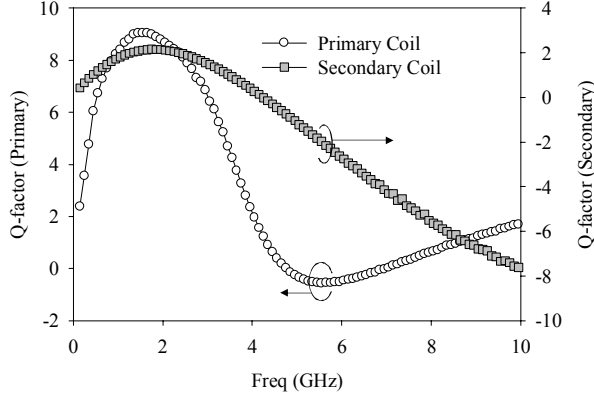| Layers	Thickness (μm)
Top Metal	3.03
Top Via	0.6
Metal 1-5	0.465
Via 1-4	0.42

Fig. 9: The Q-factor plot of the proposed transformer design.

The reported individual Q-factor plot is extracted based on (5). The measured peak Q-factors are 9.05 @ 1.5 *G*Hz and 2.15 @ 1.7 *G*Hz for primary and secondary coil, respectively.

$$Q = \frac{\text{imag}(1/Y_{11})}{\text{real}(1/Y_{11})} \quad (5)$$

4. Coupling Coefficient (k): The magnetic coupling coefficient (*k*) is extracted using (6) under 2-port configuration shown in Fig. 10.
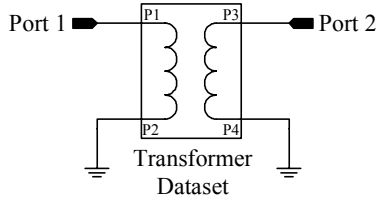

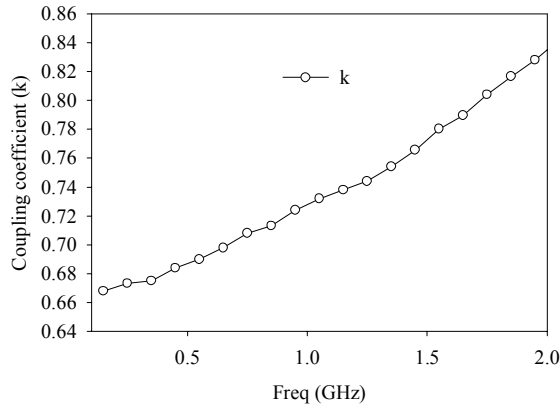Fig. 10: The 2-port schematic drawing of the transformer design.

Fig. 11: The k-plot of the proposed transformer design.

$$k = \sqrt{\frac{\text{imag}(Z_{12}) * \text{imag}(Z_{21})}{\text{imag}(Z_{11}) * \text{imag}(Z_{22})}} \quad (6)$$

The extracted *k*-plot is shown in Fig. 11. The *k* value at low frequency is ≈ 0.67 that is considered relatively high for a high turn ratio transformer design. In order to realize a transformer with *k* = 1, Ferro-magnetic material (i.e. Iron, Nickel, etc.) is required to minimize magnetic losses. In this work, reason for the low *k*-value is the isolation layer that surrounds the two conductors. (make of SiO_2) However, replacing the SiO_2 layers with the Ferro-magnetic material will not resolve the problem. In fact, it will result in process integration issues such as etching/trenching non-uniformity, unpredictable silicide formation and substantial defect density. Although fabricating an ideal *k* = 1 on-chip transformer is not feasible using standard foundry processes, a cost-free close to ideal ($k \approx 1$) highly efficient monolithic transformer has been reported in [8] by the authors.

IV. CONCLUSION

An area efficient high turn ratio transformer has been developed. Based on the area comparison with the existing transformers, the new design is able to achieve higher inductance value per unit silicon area. Thus, manufacturing a monolithic RF choke using minimum area is hereby plausible. The conceptual features of the design have been investigated and confirmed with the measured silicon data. It can be concluded that a high inductance and impedance ratio transformer have been realized on silicon. In addition, the novel transformer configuration has offered a larger dynamic range for the inductance parameter optimization.

REFERENCES

[1] J. J. Zhou and D. J. Allstot, "Monolithic transformers and their applications in a differential CMOS RF low-noise amplifier." *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2020–2027, Dec. 1998.
[2] J. R. Long, "Monolithic transformers for silicon RF IC design" *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.
[3] D. J. Cassan and J. R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18um CMOS" *IEEE J. Solid- State Circuits*, vol. 38, no. 3, pp. 427–435, Mar. 2003.
[4] M. Straayer, J. Cabanillas, G. M. Rebeiz,"A Low Noise Transformer- Based 1.7 GHz CMOS VCO," *IEEE Int. Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002,* Vol. 1, pp. 286–287, 3-7 Feb. 2002.
[5] W. L. Ping, S. I. Long,"A 5GHz CMOS low phase noise transformer power combining VCO," *IEEE Radio Freq Integrated Circuits (RFIC) Symp, 2006*, pp. 4, 11-13 June 2006.
[6] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully integrated CMOS power amplifier design using the distributed active-transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, pp. 371– 383, 2002.
[7] A. Zolfaghari, A. Chan and B. Razavi, "Stacked Inductors and Transformers in CMOS Technology," *IEEE J. Solid-State Circuits*, Vol. 36, Issue 4, pp. 620–628, Apr. 2001.
[8] C. C. Lim, K. S. Yeo, K. W. Chew, S. F. Lim, C. C. Boon and M. A. Do, "Fully Symmetrical Monolithic Transformer (True 1:1) For Silicon RFIC," *IEEE Trans. Micro. Theory and Tech.,* SUBMITTED Sep 2007.