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Temperature and Stress Distribution in the SOI Structure During Fabrication

Cher Ming Tan, *Senior Member, IEEE*, Zhenghao Gan, and Xiaofang Gao

Abstract—Silicon wafer bonding technology is becoming one of the key technologies in the silicon-on-insulator (SOI) structure fabrication. However, the high-temperature heat treatment during SOI fabrication is inevitable, and the thermal stress thus induced could have an adverse effect on the device fabricated and the bonding interface. In this work, a finite-element analysis software, ANSYS, is used to study the induced mechanical stresses at the interface during the withdrawal of wafers from a high-temperature furnace. It is found that the type of insulators and the geometric dimension of the devices such as the thickness of the work layer, insulator layer, and the substrate thickness are insignificant contributors to the induced thermal stresses. Although it is expected that the furnace temperature and withdrawal velocity are the key factors in determining the mechanical stresses, for the present bonding strength of wafers via wafer bonding technology, the withdrawal velocity must be less than 100 mm/min, and under such a withdrawal velocity, the furnace temperature is also an insignificant factor with regard to the induced stress.

Index Terms—ANSYS, finite-element analysis, mechanical stress, silicon-on-insulator (SOI), wafer bonding.

I. INTRODUCTION

SILICON wafer bonding technology for the production of silicon-on-insulator (SOI) structures is receiving considerable attention because of its process simplicity and cost effectiveness [1]. There has been considerable research on the electrical properties of SOI structures. However, the thermal stress distribution due to the inevitable high-temperature steps in the SOI processing received only little consideration. On the other hand, the existence of thermal stress due to temperature distribution could lead to the development of harmful effects in device properties and weaken the adhesive strength of bonded silicon wafers [2]. Furukawa *et al.* [3] showed that when the interfacial stress exceeds 5–12 MPa, depending on the bonding temperature, the bonded surfaces will be separated. Table I shows the maximum allowable interfacial stress for an SOI wafer obtained using a direct wafer bonding technique at different bonding temperatures. The table is an extraction from the work by Furukawa *et al.* [3].

Besides, the induced stress at the interface of silicon and the insulating layer can result in defects such as dislocation, which could lead to impurity redistribution and alter devices performance [4], [5]; the induced stress can also have influence on the effective mobility of carriers in silicon. Lee *et al.* [6] found that the electron mobility in silicon for the 100-nm buried oxide in

TABLE I
MAXIMUM ALLOWABLE INTERFACIAL STRESS FOR SOI WAFER
OBTAINED USING DIRECT WAFER BONDING TECHNIQUE AT
DIFFERENT BONDING TEMPERATURES

Bonding Temperature (°C)	Maximum Allowable Interfacial Stress (MPa)
400	3
600	4
800	4
1000	10
>1000	12

the SOI n-MOS is $370 \text{ cm}^2/\text{Vs}$ and that for the 400-nm buried oxide is $238 \text{ cm}^2/\text{Vs}$.

There are three processing steps in SOI fabrication where thermal stress can be induced:

- 1) insertion of wafers into high-temperature furnace for high-temperature processing;
- 2) high-temperature process itself, such as annealing, diffusion, oxidation, etc.;
- 3) withdrawal of wafer from high-temperature furnace.

The temperature distribution across a wafer is most nonuniform during the insertion and withdrawal steps compared to that in Step 2). Therefore, the corresponding induced stresses will be more severe in these steps than that due to Step 2). For the insertion step, the induced stress can be “softened out” when the wafers stay in the high-temperature zone for a period of time. Hence, Step 3) will induce the most severe and detrimental stresses among the three processing steps. Therefore, in this work, focus is placed on the thermal stress induced from the withdrawal of wafers from high-temperature furnace.

In this work, the thermal stress induced by Step 3) will be calculated under different furnace temperatures, withdrawal velocities, and structure dimensions. It is hoped that the calculation can provide a better understanding of the various contributing factors that affect the induced thermal stresses. Thermal stress analyses are simulated over a range of processing furnace temperatures from 800 °C to 1150 °C. The withdrawal velocities chosen are 100, 250, and 500 mm/min. The wafer is of 4-in diameter with an insulator in between the silicon work layer and silicon substrate. The thickness of the insulator ranges from 0.1 to 3.0 μm , the thickness of the work layer (epilayer) ranges from 20 to 100 μm , and the thickness of the substrate is 200 μm .

The large thickness of the insulator and work layer used in the work is due to the requirement of the power semiconductor devices. While the problem of thermal stress during SOI wafer fabrication is being controlled for VLSI as the fabrication has been successful, the application of SOI in power semiconductor devices is still behind partly due to the large thickness requirement for the insulator and the work layer, and the effect of thermal

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Fig. 1. Possible thermal induced stresses in the incremental volume of the structure.

stress can be significant. The purpose of this work is to investigate the thermal stress for such devices.

II. NUMERICAL FORMULATION

Due to the axial symmetry of a wafer, no displacement is expected at the center of a wafer; hence, the analysis is done on half of the wafer with the extreme left of the structure (i.e., the center of the wafer) considered as clamped rigidly as a boundary condition. Also, as a wafer is circular in shape, the polar coordinate is used in the analysis of this work.

In the presence of an insulator layer and nonuniform temperature distribution, the possible thermal stresses that can be induced are shown in Fig. 1. In this work, the temperature distribution along the y axis can be considered uniform. This is because the wafer is thin and silicon is quite a good thermal conductor. Thus, σ_{yy} could be very small. Under the extreme condition where the furnace temperature and withdrawal velocity are the highest, i.e., at 1150 °C and 500-mm/min withdrawal speed, the absolute maximum values (for the range of the thicknesses of the insulator and work layer) of the various stresses as computed from ANSYS are as follows:

$$\begin{aligned}\sigma_{xx} &= 29.3 \text{ MPa}; & \sigma_{yy} &= 0.33 \text{ MPa} \\ \sigma_{\theta\theta} &= 44.9 \text{ MPa}; & \tau_{xy} &= 0.36 \text{ MPa}.\end{aligned}$$

One can see that even under such an extreme condition, σ_{yy} and τ_{xy} are much smaller than the other stresses, and hence it can be omitted in this work, and the analysis of stress can therefore be reduced to two dimensions.

The finite-element program used in the calculation in this work is ANSYS (Release 5.4) [7]. The SiO₂ and Si are characterized as an isotropic linear elastic solid and an isotropic elastic perfectly plastic solid, respectively [8]. The other material properties for Si and SiO₂ are considered to be homogeneous, which are summarized in Table II [9], [10].

III. TEMPERATURE DISTRIBUTION

As the wafer is drawing from the high-temperature furnace, the temperature across the wafer will be very nonuniform. Fig. 2 shows the profiles of temperature difference across a wafer when it is being withdrawn from furnaces of different temperatures ranging from 800 °C to 1150 °C, under various

TABLE II
MATERIAL PROPERTIES OF Si AND SiO₂

Parameter	Symbol	Unit	Si	SiO ₂
Young's modulus	E	Pa	1.3×10^{11}	7.14×10^{10}
Poisson ratio	ν	-	0.28	0.16
Thermal expansion coefficient	α	$^{\circ}\text{C}^{-1}$	2.6×10^{-6}	$0.51 \times 10^{-6} + 5.4 \times 10^{-10} T$
Heat capacity	C_p	J/(Kg K)	700	0.816
Thermal conductivity	K	W/(m K)	130	1.3376
Density	ρ	Kg/m ³	2329	2200

Fig. 2. Distribution of the temperature difference across a 4-in wafer at various furnace temperatures with a withdrawal speed of 100 mm/min (curves without symbols) and at various withdrawal velocity with 1150 °C furnace temperature (curves with symbols). Left vertical axis is for curves without symbols and right vertical axis is for curves with symbols.

withdrawal velocities for a 4-in wafer, assuming the furnace temperature is uniform and only a single wafer is in the furnace.

The heat transfer coefficient h needed in the computation of the temperature profile in Fig. 2 is determined by fitting the computed temperature distribution to the experimental results obtained by Widmer [4], with an allowable error of $\pm 5\%$. Then, using the fact that the convection coefficient value h is only related to withdrawal velocity V given as $h \propto V^{2/3}$ [8], the value of h at other withdrawal velocities can be computed.

IV. STRESS CALCULATION AND DISTRIBUTION

For the nonuniform temperature distribution calculated in Fig. 2, three types of stresses will be induced at the interface of silicon and insulator.

- Stress due to temperature distribution itself, denoted as σ_1 (σ_{1-x} and $\sigma_{1-\theta}$) [12].
- Stress due to the difference in thermal expansivities between Si and insulator, denoted as σ_2 (σ_{2-x} and $\sigma_{2-\theta}$) [13].
- Due to the stresses in 1) and 2), and if the thicknesses of the silicon work layer (WL) and the silicon substrate (SU) are different, the wafer will warp. Hence, a third stress due to the warpage of the wafer will be developed, denoted as σ_3 (σ_{3-x} and $\sigma_{3-\theta}$).

Therefore, the total stress at the interface along the x direction is given by

$$\sigma_{\text{total}_x} = \sigma_{1_x} + \sigma_{2_x} + \sigma_{3_x} \quad (1)$$

and that along the θ direction is given by

$$\sigma_{\text{total}_\theta} = \sigma_{1_\theta} + \sigma_{2_\theta} + \sigma_{3_\theta}. \quad (2)$$

The total stress at any point along the interface is then given by

$$\sigma_{\text{total}} = \sqrt{\sigma_{\text{total}_x}^2 + \sigma_{\text{total}_\theta}^2}. \quad (3)$$

From the physical reasoning, the following factors are expected to affect the stress distribution of the structure, namely the furnace temperature, the withdrawal velocity, the thicknesses of WL, SU, and insulator, and wafer diameter. However, simulation shows that only the effect of furnace temperature, withdrawal velocity, and the wafer diameter are significant for the induced thermal stress [14]; hence, only these factors are discussed in this work.

A. Simulation Verification

To begin the simulation, the accuracy of the simulation must be verified. Consider the general case where the parameters used are listed in Table III, and the stress distributions are computed as shown in Fig. 3.

From the physical point of view, the stress distributions depicted in Fig. 3 are reasonable. The σ_{total_x} distribution shown in Fig. 3 is expected since no stress should exist at the edge of the wafer as that is a free surface. As the temperature at the center of the wafer is much higher than that at the edge, σ_{total_x} should be larger at the center and gradually decreasing. The concave shape of σ_{total_x} is due to the convex shape of the distribution of the temperature difference shown in Fig. 2.

The $\sigma_{\text{total}_\theta}$ distribution shown in Fig. 3 can be explained by considering a wafer as an integration of many incremental rings that “glue” to one another. Under high temperature with temperature difference across a wafer as depicted in Fig. 2, each incremental ring will be subjected to two stresses. The larger contraction of the outer ring versus that of the inner ring right next to it will exert a compressive stress to the inner ring, and a tensile stress in the outer ring. Hence, for any given ring, it will experience a compressive stress from the outer ring next to it and a tensile stress from the inner ring next to it. At the center of the wafer, there is no inner ring, and hence only compressive stress exists. At the edge of the wafer, there is no outer ring, and hence only tensile stress exists. Since the difference in temperature is smaller near the center of the wafer, and larger as the edge of the wafer is approaching, the slope of $\sigma_{\text{total}_\theta}$ is gradually increasing from the center to the edge of the wafer as seen in Fig. 3.

To verify the calculation accuracy, the analytical stress distribution is calculated using the expressions given by Tong and Gosele [13]. Comparing the computed stresses with that obtained from the analytical expression, we found that the accuracy of the numerical calculation can be assured.

Fig. 3. Stress distributions (σ_{total_x} and $\sigma_{\text{total}_\theta}$) at 1150 °C and the withdrawal velocity of 500 mm/min.

TABLE III
PARAMETERS USED TO CALCULATE THE STRESS DISTRIBUTION
SHOWN IN FIG. 4

Substrate thickness = 200 μm	Work layer thickness = 20 μm
Withdrawal velocity = 500 mm/min	Furnace temperature = 1150°C

B. Effect of Furnace Temperature

Now that the simulation is verified, we can proceed to study the effect of the various factors mentioned above. As σ_{3_x} and σ_{3_θ} are negligible [14], we can simplify the simulation by having the thicknesses of WL and SU to be equal. Fig. 4 shows the distribution of σ_{total} at furnace temperature of 1150 °C at withdrawal velocity of 500 mm/min. It can be seen that τ_{xy} can be neglected in the analysis, and the highest stress occurs at the center and the edge of a wafer.

Fig. 5 shows the maximum σ_{total} and its variation across a wafer as a function of furnace temperature at a withdrawal velocity of 500 mm/min. The variation of σ_{total} is defined as

$$\% \text{ variation} = \frac{\max(\sigma_{\text{total}}) - \min(\sigma_{\text{total}})}{\min(\sigma_{\text{total}})} \times 100. \quad (4)$$

From Fig. 5, one can see that the higher the furnace temperature, the larger the stress σ_{total} . However, the variation of σ_{total} across a wafer does not depend much on the furnace temperature.

C. Effect of Withdrawal Velocities

The effect of withdrawal velocities on the stress distribution can be similarly studied. Fig. 6 shows the effect of withdrawal velocities on the σ_{total} and its variation at the furnace temperature of 1150 °C. It can be seen that the lower the withdrawal velocity, the lower the stress. However, the variation in stress across a wafer will be higher at lower withdrawal velocity.

Fig. 6 also shows that when the withdrawal velocity decreases from 500 to 250 mm/min, a large decrease in the stresses is resulted. However, when the velocity decreases from 250 to

Fig. 4. Total stress distributions at 1150 °C and withdrawal velocity of 500 mm/min.

Fig. 5. Effect of furnace temperature on σ_{total} and its variation.

100 mm/min, the reduction of the stresses becomes smaller. Hence, there is a withdrawal velocity below which the advantage of reducing stresses by reducing the withdrawal velocity has marginal gain.

D. Effect of Silicon Wafer Size

As the wafer size increases, the temperature distribution across the wafer will be more severe. For qualitative analysis, assume the heat transfer coefficient h is independent of the wafer size; the tremendous difference in the thermal-induced stresses is shown in Fig. 7.

V. SUMMARY

The induced thermal stresses in a full SOI structure due to the withdrawal of a wafer from a high-temperature furnace are studied. From the studies, it is found that the major factors in determining the stress levels are the withdrawal velocity and furnace temperature, with the former being the most significant as summarized in Fig. 8. Therefore, the structure geometry can be optimal without taking into consideration its effect on thermal stress.

Fig. 6. Effect of withdrawal on σ_{total} and its variation.

Fig. 7. Stress distribution (σ_{total_x} and σ_{total_θ}) at the interface for different wafer sizes. D is the diameter of the wafer. Right vertical axis is for curves without symbols, and left vertical axis is for curves with symbols.

Fig. 8. Relationship between maximum σ_{total} at the interface and withdrawal velocity under different furnace temperature.

Fig. 8 also allows the acceptable furnace temperature and withdrawal velocity to be estimated once the allowable stress level is defined. For example, we see from Table I that since the maximum interface stress is 12 MPa for bonding temperature above 1000 °C [3], the withdrawal velocity must be less than

100 mm/min. Below this withdrawal velocity, the effect of the furnace temperature becomes insignificant as can be seen from Fig. 8.

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