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3D Circuit Model for 3D IC Reliability Study

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Abstract

3D integrated circuit technology is an emerging technology for the near future, and has received tremendous attention in the semiconductor community. With the 3D integrated circuit, the temperature and thermo-mechanical stress in the various parts of the IC are highly dependent on the surrounding materials and their materials properties, including their thermal conductivities, thermal expansivities, Young modulus, poisson ratio etc. Also, the architectural of the 3D IC will also affect the current density, temperature and thermo-mechanical stress distributions in the IC.

In view of the above-mentioned, the electrical-thermal-mechanical modeling of integrated circuit can no longer be done with a simple 2D model. The distributions of the current density, temperature and stress are important in determining the reliability of an IC. In this work, we demonstrate a method of converting 2D circuit layout into a 3D model. Simulations under real circuit operating condition are carried out using both Cadence (a circuit simulator) and ANSYS (finite element tool). Limiting our study to the electromigration failure, we compute the current density, temperature and stress distributions of the interconnect layers by considering the heat transfer and Joule heating, and the “weak spot” for electromigration is identified. Layout design can be modified based on the simulation results so as to enhance the 3D circuit interconnect reliability.

1. Introduction

As the size of integrated circuits continues to scale down, interconnect reliability has become a main factor that determines circuit reliability. Research had shown that, with narrower line width and higher current density, electromigration (EM) and time-dependent dielectric breakdown will be the most dominant failure mechanisms [1].

Many researches had been done on the effect of electromigration on the interconnect reliability [2-5]. However, the 3D EM modeling are mainly on simple straight line or two level line-via structure with electron wind force as the sole driving force for EM, which is no longer the case for line width below 200 nm [6]. The effect of surrounding materials and interconnect structures is found to greatly affect the EM performance which cannot be incorporated in the simple 2D model [7].

Electromigration has been taken into consideration during 2D circuit design phase in some works [8-10]. 2D modeling, though is much simpler and time saving than 3D modeling during both construction and simulation phases, will underestimate the peak current density when

the track and via width are different, and this may result in an electromigration susceptible process design [11]. Furthermore, due to layer overlapping, the entire circuit cannot be represented by 2D modeling, even for very simple circuit. Complex geometries like sharp corners or structures with varying width, which are essential for observing some of the important EM effects, are also difficult to be built using 2D modeling. The determination of the temperature, current density and hydrostatic stress distributions in the interconnections of integrated circuits requires a 3D circuit model as in its actual physical implementation in wafer fabrication. The above-mentioned distributions are essential to the evaluation of the electromigration of interconnect [6]. In short, there is an essential need for 3D circuit modeling for a reliable IC design.

In this work, we demonstrated the construction of a 3D circuit model from a 2D circuit layout. The finite element modeling of the 3D circuit model using the input from circuit simulator to obtain the temperature, current density and thermo-mechanical stress distributions in a 3D circuit structure will be illustrated. The above-mentioned distributions determine the reliability of an IC.

2. 3D Model Construction and Simulation

2.1. Layout Extraction and 3D model Construction

For simplicity, a two-transistor inverter circuit with one PMOS and one NMOS is used as an example in this work, as shown in Figure 1.

Figure 1. Schematic of a simple inverter.

The circuit layout is drawn in Cadence using CHARTERED 0.18 μ m/5V technology. The Cadence GDSII file is first converted into an ANSYS compatible SAT file. Thicknesses of the various layers are inputted during importing and a 3D SAT model is built as shown in Figure 2.

Figure 2. (a) Front, (b) isometric and (c) tilted view of the inverter circuit in the SAT model.

When the inverter circuit is in operation mode, there will be current flow in and out of the transistors, which in turn affects the temperature of the circuit. The transistors are therefore treated as the current sources in the model. The focus of attention, the interconnect layers, together with the current sources (the transistor diffusion regions) are extracted and imported into ANSYS WORKBENCH.

After the importing of the essential structures, additional layers that are present in the chip such as the Si-substrate, SiO₂, SiN etc. and the packaging materials such as the plastic encapsulant, adhesive die attach, die pad are added into the model as shown in Figure 3, so as to represent the realistic chip condition.

Figure 3. Illustration of plastic used in a microelectronic device [12].

A 1000x1000x300μm³ 3D model is created after adding the above layers (Figure 4), with the inverter circuit enclosed at the center just above the silicon substrate layer. The properties of the various materials used in the model are shown in Table 1.

Figure 4. 3D model showing different layers and the enlarged view of the inverter region after removing the covered layers.

Table 1. Material properties of various layers [12-14].

Materials	Properties						
	Young's Modulus (MPa)	Poisson's Ratio	Density (kg/m ³)	Thermal Expansion (1/°C)	Thermal Conductivity (W/m.°C)	Specific Heat (J/kg.°C)	Resistivity (Ohm-m)
Copper	1.298x10 ⁵	0.34	8920	1.65x10 ⁻⁵	401	3.85	1.724x10 ⁻⁸
Si Substrate	1.3x10 ⁵	0.28	2330	2.6x10 ⁻⁶	149	700	1x10 ¹⁷
As-doped Si							9.9x10 ⁻³
B-doped Si							2.81x10 ⁻²
Heavily doped Si							1x10 ⁻⁵
SiO ₂	7.14x10 ⁴	0.16	2200	6.8x10 ⁻⁷	1.75	1000	1x10 ¹⁷
SiN	2.2x10 ⁵	0.27	3100	3.2x10 ⁻⁶	30	700	1x10 ¹³
Polyimide	3100	0.33	1430	5x10 ⁻⁵	0.18	1100	1x10 ¹⁵
96% Alumina	276	0.25	3965	7.1	20.9	779	1x10 ¹³

The 3D ANSYS geometry model is then meshed and exported to ANSYS Classic for transient analysis.

2.2. Transient Thermal-Electrical Analysis

2.2.1. Boundary Conditions

To simulate the normal operating condition of the circuit, the initial and boundary conditions of the model are set as shown in Figure 5, with a convection heat transfer coefficient of 20W/m².°C to simulate the 90°C ambient condition [15].

Figure 5. Initial and boundary conditions of the 3D model, view from the back.

2.2.2. Current and Voltage Loads

The instantaneous source and drain currents flowing in and out of the diffusion regions of the transistors are the current loads. This current, together with the voltage across the interconnect lines, will cause the interconnect lines to heat up. The current values applied in the finite element analysis are determined from Cadence.

When PMOS is on, there will be current flowing from V_{dd} through the interconnect line into PMOS source, and then goes through the diffusion region to PMOS drain, after that goes to the output line. Similar current flow applies to the NMOS-on condition. Four current sources (as listed below), together with their corresponding voltage values, are treated as inputs in the ANSYS transient thermal simulation.

- (1). current flowing from V_{dd} to PMOS source - I_{ps};
- (2). current flowing from PMOS drain to output line - I_{pd};
- (3). current flowing from output line to NMOS drain - I_{nd};
- (4). current flowing from NMOS source to ground - I_{ns}.

Literature [2] had shown that, the steady-state simulation using the RMS value will give the same final temperature as the transient simulation. However, in the realistic AC operation condition, besides the current

values, the corresponding voltage values are also varying, which means that the current-voltage coupled effect will vary from time to time. Therefore, simply using the RMS value of the current and voltage for the steady-state simulation is not suitable in this circumstance.

This work, as a combination of Cadence and ANSYS, uses the current and voltage simulation results extracted from Cadence under realistic circuit operating condition as the inputs in ANSYS.

As an example, the inverter circuit shown in Figure 1, with a resistive load of 50K is used for Cadence simulation. The instantaneous current and voltage of the transistors at the specified positions, namely the source and drain of the MOSFETs, the input and output lines of the circuit are measured at an operating frequency of 100MHz.

Figures 6 and 7 show the simulation results from Cadence. When the inverter is operating, there is current flow in the circuit, either through PMOS or NMOS. The magnitude of the current flow depended on the load in the circuit.

Figure 6. Instantaneous source and drain current for PMOS and NMOS at 100MHz.

Figure 7. Instantaneous input and output voltage at 100MHz.

Beside these normal operation currents, it can be seen from Figure 6 that, there are two current spikes due to the switching of the two MOSFETs respectively within one period. These current spikes, although occurs in a very short time duration, is hundreds or thousands times larger in magnitude than the normal operation current, and will contribute a significant portion of the total power

consumption of the circuit. The magnitude of the power consumption during the current spike is more than thousand times larger than during normal operation ($4.3 \times 10^{-3} \text{W}$ and $7.5 \times 10^{-3} \text{W}$ as compared to $1 \times 10^{-6} \text{W}$ and $7.5 \times 10^{-6} \text{W}$ under normal condition). Therefore, it is important to include these current spikes in the simulation.

For simplification, the inverter circuit operation within one period is divided into the following seven steps as shown in Figure 8.

Figure 8. Vin and Ids variation with time (not to scale) showing the seven load steps.

The above seven steps correspond to seven load steps in the transient simulation. For circuit simulation with an operation frequency of 100MHz, the instantaneous voltage and current within one cycle (from 0s to 10ns) are shown in Table 2.

Table 2. Instantaneous voltage and current values (extracted from Cadence).

Load Steps	Time (s)	Vin (V)	Vout (V)	Ips (pA)	Ipd (pA)	Ins (pA)	Ind (pA)
Load Step 1	0	0	4.922	1.00×10^8	-1.00×10^8	-1.36×10^3	1.78×10^6
Load Step 2	4.00×10^{-12}	0.4073	5.035	-2.71×10^8	-1.21×10^8	-1.18×10^8	2.05×10^7
Load Step 3	3.20×10^{-11}	3.209	3.473	5.70×10^8	-1.34×10^8	-1.54×10^9	1.27×10^9
Load Step 4	5.00×10^{-11}	5	0.2028	-7.62×10^7	-1.15×10^8	-4.27×10^8	1.11×10^8
Load Step 5	5.05×10^{-9}	5	1.35×10^{-4}	3.18×10^4	-1.80×10^2	-2.39×10^2	1.77×10^2
Load Step 6	5.07×10^{-9}	3.236	1.11	1.75×10^9	-1.37×10^9	-1.14×10^9	1.34×10^9
Load Step 7	5.10×10^{-9}	0.2254	4.486	9.16×10^8	-1.54×10^8	4.19×10^7	6.42×10^7

*Vdd and Gnd are fixed at 5V and 0V respectively.

A do-loop can be used to repeat the above load steps in the case of multiple cycles to represent a continuous circuit operation.

2.2.3. Application of the Current and Voltage Loads

Eight nodes thermal-electric element SOLID69 is used in the transient simulation. The locations of applying the current and voltage sources in the 3D model are shown in Figure 9, and these correspond to the measurement locations in Cadence.

Figure 9. Current and voltage inputs in (a) isometric view, (b) tilted view shown the current flow direction.

2.3. Application of Submodeling

A fine mesh is critical in achieving an accurate simulation result. The original full model is too large and thus very time and resource consuming for ANSYS transient analysis if a fine mesh is applied. As a result, submodeling methodology is used in this simulation.

Submodeling, which is also known as the cut-boundary displacement method or the specified boundary displacement method, cuts through the global model. Fine mesh is done on the “cut out” region, while the global model can be meshed much coarser. Mesh refinement is achieved on the cut out submodel region for obtaining an accurate simulation result, and also greatly eliminates the redundant effort on solving the region that is not the focus of attention.

When submodeling is applied, a cut boundary (the boundary that cuts through the coarse model) is specified, displacement and temperature results calculated on the cut boundary of the coarse model are applied as the boundary conditions for the submodel. According to the St. Venant's principle, if an actual distribution of forces is replaced by a statically equivalent system, the distribution of stress and strain is altered only near the regions of the load application. This implied that, acceptable results can be obtained in the submodel if the cut boundaries of the submodel are adequately far away from the stress concentration, in view of the fact that the stress concentration effects are localized around the concentration site [16].

A simple steady-state simulation is carried out on the full model to determine where the cut boundary should be, i.e. the size of the submodel. The first current spike values are used with 90°C as the initial temperature as this is the “worst case” value which will give a higher temperature than the normal operating condition, and it is thus adequate for determining the boundary location.

Figure 10. Steady-state temperature distribution of the inverter model using the “worst-case” input values for the global model.

From Figure 10, it can be seen that the temperature is almost constant at around 5μm away from the model center, and it is acceptable to place the cut boundary there. A 10x20x15μm³ submodel centered with the inverter region is cut out from the original 1000x1000x300μm³ full model as shown in Figure 11.

Figure 11. A cut out of the sub-model from the full model shown (a) sub-model and (b) full model

A local tetrahedron coarse mesh of size 0.5μm at the interconnect layer is used for the full model, while a local fine mesh of 0.1μm is applied to the submodel.

Figure 12. Tetrahedron mesh on the interconnect region shown (a) coarse mesh on the full model and (b) fine mesh on the sub-model.

The outer surfaces of the submodel are treated as the cut boundary. According to the transient submodeling analysis technique introduced by Wang et al. [17], the simulation results of the full model for each load step are recorded, and the solution for the first load step is retrieved and applied on the cut boundary of the submodel. The submodel is then solved with the cut boundary condition and the external current and voltage loads for that load step. This is repeated for the remaining load steps.

2.4. Transient Structural Analysis

Temperature gradient in interconnect is resulted from the current load, and due to the thermal mismatch of the materials in an interconnect structure, thermally induced hydrostatic stress occur in the materials. A transient structural analysis is carried out to study the stress distribution in the interconnects.

2.4.1. Boundary Conditions

All nodes at the model outer surface are fixed as they are not free to move. Stress free temperature (SFT) of 350°C for copper is used as the reference temperature in this simulation [18].

2.4.2. Thermal Load

LDREAD command in ANSYS is used to read the temperature results of all the load steps as obtained in the transient thermal-electric analysis in section 2.2. These temperature results, together with the time of their occurrence, are used as the thermal load in the transient structural analysis.

Thermal-electrical solid element SOLID69 is replaced by the equivalent structural element SOLID45 for the transient structural analysis. Submodeling technology described earlier is applied here also.

3. Results and Discussions

Figures 13 and 14 show the temperature and current density distributions of the interconnects and the diffusion regions after one and twenty load cycles.

Figure 13. (a) Temperature distribution (unit:°C) and (b) current density distribution (unit:pA/μm²) of the interconnect layer after one load cycle (i.e. 10ns) at load step 7, with an initial temperature of 90°C and an operating frequency of 100MHz.

Figure 14. (a) Temperature distribution (unit:°C) and (b) current density (unit:pA/μm²) of the interconnect layer after twenty load cycle (i.e. 200ns) at load step 140, with an initial temperature of 90°C and an operating frequency of 100MHz.

A general increasing trend in temperature of the chip is observed after continuous circuit operation.

(a)

(b)

Figure 15. Temperature variation with time of the contact region of the interconnect for (a) one load cycle (10ns), and (b) multiple load cycles (200ns). Here PD denotes PMOS drain, PS denotes PMOS source, ND denotes NMOS drain, and NS denotes NMOS source.

Time evolution of hydrostatic stress at different locations in the model can be plotted based on the transient structural simulation results, as shown in Figure 16.

(a)

(b)

Figure 16. Time evolution of hydrostatic stress of (a) the interconnect contact at PMOS region, (b) the interconnect contact at NMOS region within one load cycle (10ns). The solid line denotes the contact at the drain region and the dotted line denotes the contact at the source region.

It is observed that the stress decreases with time as the interconnect temperature increases, which is as expected as the interconnect temperature approaches its stress free temperature. The change in stress is small because the temperature increase in the interconnect is small in this circumstance. A comparison of the temperature and stress curve in Figure 17 shows the inverse relationship of the two.

Figure 17. Comparison of stress and temperature profile at contact PD. The solid line is the temperature profile and the dotted line is the stress profile.

The stress distribution of the model at the end of one load cycle is shown in Figure 18.

Figure 18. Stress distribution of the 3D model at the end of one load cycle (10ns). Only the interconnects, the diffusion regions are shown here for clarity.

4. Conclusions

This work demonstrates a step by step approach of converting a 2D circuit layout into 3D model. The methodology of performing transient thermal and structural analysis using ANSYS with submodeling technology is also illustrated.

Thermal and stress distribution at any location in the model can be plotted from the simulation results, which can then be used in subsequent analysis for layout modification and thus enhance the circuit reliability.

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