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Rofail, Samir S.; Yeo, Kiat Seng

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Experimentally-Based Analytical Model of Deep-Submicron LDD pMOSFET's in a Bi-MOS Hybrid-Mode Environment

Samir S. Rofail, *Senior Member, IEEE*, and Yeo Kiat Seng

Abstract—The hybrid-mode operation of deep-submicron LDD pMOSFET's has been investigated experimentally. Based on the experimental results, analytical models for the threshold voltage, the device currents, the transconductance, and the output conductance were derived. The various current components in this mode of operation were extracted and identified. The effects of independently biasing the source, drain, gate, and body potentials on the device currents and parameters were examined. The body-induced-barrier-lowering (BIBL) effect, which is one of the V_{SB} effects and introduced for the first time, has been used to account for the changes in both the threshold voltage and the device currents caused by the forward source-body bias.

NOMENCLATURE

Λ_1, Λ_2	LDD region fitting parameters.
α	Fitting parameter used in the unified MOS current equation.
ϵ_{ox}	Permittivity of silicon dioxide.
ϵ_{si}	Permittivity of silicon.
Θ	Charge-sharing factor.
η	Drain-induced-barrier-lowering factor.
γ	Overall V_{SB} effects factor.
λ	Source barrier height lowering fitting parameter.
Φ_s	Surface potential.
μ_p	Hole mobility in the channel.
μ_{peff}	Effective hole mobility.
v_{sat}	Saturation velocity of carriers.
a_1, a_2	Charge-sharing model fitting factors.
$A_{bipolar}$	Effective cross-sectional area for the bipolar current.
A_{space}	Effective cross-sectional area for the space charge current.
C_{ox}	Gate oxide capacitance.
D_p	Hole diffusion constant.
E_c	Critical electric field.
g_{m1}	Principal transconductance.
g_{m2}	Secondary transconductance.
g_{sd}	Output conductance.
J_n	Electron current density.
J_p	Hole current density.
l_c	Characteristic length.
L	Device drawn channel length.
L_d	Electrical channel length for the MOS current.

L_e	Electrical channel length for the bipolar and space charge current.
L_{eff}	Device effective channel length.
L_p	Length of the LDD P-region.
m_1	Space charge current model fitting parameter.
n_f	Ideality factor.
n_i	Intrinsic concentration of silicon.
N_a	Source/Drain concentration.
N_{a-}	LDD P-concentration.
N_{sub}	Channel doping concentration.
P_c	Hole concentration at the edge of the drain (collector)/n-well junction.
P_e	Hole concentration at the edge of the source (emitter)/n-well junction.
q	Electronic charge.
r_j	LDD P-implant junction depth.
R_{well}	N-well resistance.
T_{ox}	Gate oxide thickness.
V_{bi}	Built-in potential of the LDD P-/n-well regions.
V_t	Thermal voltage.
V_{FB}	Flat-band voltage.
V_J	Source-body or drain-body junction voltages.
V_{SB}	Source-body voltage.
$V_{SB,eff}$	Effective source-body voltage.
V_{SD}	Source-drain voltage.
$V_{SD,eff}$	Effective source-drain voltage.
V_{SG}	Source-gate voltage.
$V_{T,eff}$	Effective threshold voltage.
W	Device channel width.
X_d	Depletion width at the drain.
X_{dep}	Depletion layer thickness.
X_{dm}	Depletion width at the drain's surface.
X_j	P+ implant junction depth.
X_s	Depletion width at the source.

I. INTRODUCTION

RECENTLY, hybrid-mode devices employing lateral p-n-p BJT in a pMOS structure have received much attention due to its high current gain and simple technology [1], [2]. However, the studies of these devices were mainly done with the gate connected to the body, and the effects of independently biasing the source, drain, gate, and body potentials on the device performance could not be examined.

In this paper, the performance characterization as measured by the key device parameters of scaled LDD pMOSFET's is

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The authors are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798.

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Fig. 1. The cross section of an LDD pMOS device.

presented. Two sets of fundamental quantities are investigated. These are 1) the device currents—the principal MOS current, the lateral bipolar current, and the space charge current; and 2) the device parameters—the threshold voltage, the transconductance, and the output conductance. The results and findings, experimentally based, are backed by some physical and analytical verifications. We have also introduced for the first time, the body-induced-barrier-lowering (BIBL) effect which accounts for changes in both the threshold voltage and the device currents when the source-body is forward biased. The significance of the work stems from the increasing need not only to accurately model short-channel MOSFET's, but also to study the device performance in a bipolar/MOS hybrid-mode environment. The latter has been used frequently in CMOS/BiCMOS circuit design for low-voltage low-power applications [3], [4].

II. DEVICE STRUCTURE AND FABRICATION

A cross-sectional view of an LDD pMOSFET residing in a phosphorus implanted n-well is shown in Fig. 1. The various current components flowing in the device under the Bi-MOS hybrid-mode environment are illustrated in Fig. 2. The pMOS devices were fabricated using a twin-well CMOS process on a p/p-epi substrate of 6–9 $\Omega \cdot \text{cm}$ resistivity. Phosphorus was used for the n-well implantation with a dose of $10^{13}/\text{cm}^2$ and an energy of 150 keV. The n-well junction depth was 2 μm and it has a sheet resistance of 1 $\text{k}\Omega/\square$. Modified LOCOS isolation was performed with 0.15 $\mu\text{m}/\text{side}$ bird's beak. Next, a gate oxide of 13 nm thickness was grown, followed by the deposition of n++ poly gate. Boron was then selectively implanted to form a shallow (0.12- μm junction depth), p-type LDD region. The LDD structure not only suppresses the band-to-band tunneling current but also permits closer separation of the S/D regions and tighter isolation pitch. Using the sidewall oxide spacer technology, high-quality oxide was deposited and later removed with an anisotropic etchback for poly planarization. This was followed by the S/D implantation. BF_2 with a dose of $5 \times 10^{15}/\text{cm}^2$ and an energy of 70

Fig. 2. The currents flowing in the MOS device during the hybrid-mode environment.

keV were used. The p+ junction depth was 0.22 μm with a sheet resistance of 100 $\Omega/\square$. Next, TiW/Al-Si-Cu/ARC interconnect for metals 1 and 2 and SOG planarization were carried out. Finally, tapered contact and via for good step coverage were performed, followed by the oxide/nitride dual passivation layers deposition process.

III. THE THRESHOLD VOLTAGE

The threshold voltage is often used as an indicator in evaluating short-channel effects of scaled technologies. The 'Transconductance Peak' method is used to extract the threshold voltage of a few LDD pMOS devices. This method is relatively insensitive to the interface states, normal field mobility degradation, and series resistance [5].

The proposed model for the threshold voltage takes the form

$$V_{T_{\text{eff}}} = V_{T0} - \eta V_{SD_{\text{eff}}} - \gamma V_{SB_{\text{eff}}} \quad (1)$$

where

$$V_{T0} = V_{FB} + \phi_s + \frac{\Theta}{C_{\text{ox}}} \sqrt{2q\epsilon_{\text{si}} N_{\text{sub}} \phi_s} \quad (1a)$$

$$\Theta = a_1 - \frac{a_2 r_j}{L_{\text{eff}}} \quad (1b)$$

V_{T0} is the threshold voltage at $V_{SD} = V_{SB} = 0$ V and is modeled by extending the classical threshold voltage expression using the charge-sharing model [6], [7] to account for the reduction of its value when the channel length is reduced. The modeling of the factors η [8] and γ will be described in the next section. The introduction of η and γ enables the effects of both the drain-induced-barrier-lowering (DIBL) and the forward source-body bias on the threshold voltage to be studied separately.

For LDD devices, to account for the voltage drop in the LDD region, the effective source-drain and source-body voltages are found to be [9]

$$V_{SD_{\text{eff}}} = \frac{V_{SD}}{1 + \frac{\Lambda_1 L_p}{L_c}} \quad (2a)$$

$$V_{SB_{\text{eff}}} = \frac{V_{SB}}{1 + \frac{\Lambda_2 L_p}{L_c}} \quad (2b)$$

where

$$l_c = \sqrt{\frac{\epsilon_{si} T_{ox} X_{dep}}{\epsilon_{ox} \eta}} \quad (2c)$$

$$X_{dep} = \sqrt{\frac{2\epsilon_{si}}{qN_{sub}} (\phi_s - V_{SB_{eff}})} \quad (2d)$$

where $\Lambda_1 = \Lambda_2 = 0.3$ is found to give the best fit for our threshold voltage model. It was found that the effective drain voltage for the LDD device, based on the extracted process parameters, is about 20% less than the actual applied drain voltage. This explains why LDD devices exhibit better threshold voltage stability for short-channel lengths.

A. Drain-Induced-Barrier-Lowering (DIBL) Effect

For short-channel MOS devices, and due to the proximity of the source and drain, the threshold voltage is affected by the source-drain bias, especially at high values of V_{SD} . The drain region can be thought of as a second gate causing the channel length modulation and affecting the potential distribution near the source. The DIBL factor η for a given technology is defined as

$$\eta = \frac{\Delta V_{T_{eff}}}{\Delta V_{SD}} \quad \text{at } V_{SB} = 0 \text{ V} . \quad (3)$$

In determining the DIBL factor, a family of curves $V_{T_{eff}}$ versus V_{SD} at various source-body bias and for different channel lengths have been generated. The η value for a particular technology and source-body bias condition is obtained by taking a small change in the threshold voltage over a small change in V_{SD} at the particular V_{SD} of concern. An iterative matching process has been adopted to determine the expression for η by fitting the set of experimental η values for various channel lengths and different V_{SD} . The results in Fig. 3(a) show that η against V_{SD} is fairly constant, and therefore the expression used to model the DIBL effect is given as

$$\eta = 1.03e^{-(7.8L^2 - 3L + 2.5)} \quad (4)$$

where L is in μm . As depicted from Fig. 3(b), ηV_{SD} increases with reducing channel lengths.

B. The V_{SB} Effects

Forward V_{SB} values affect the threshold voltage through the following.

- 1) The channel length modulation, caused by the changes in the depletion width of the source and drain junctions. As V_{SB} increases, the electrical channel length increases which tends to increase the threshold voltage.
- 2) The reduction of the depletion layer thickness under the gate, X_{dep} , thereby reducing the threshold voltage.
- 3) BIBL, the lowering of the source-body barrier height, which triggers holes injection into the channel region. This phenomenon tends to reduce the threshold voltage.

Fig. 3. (a) The effect of V_{SD} bias on the factor η . (b) The DIBL effect for different channel lengths and V_{SD} bias.

The correlations between V_{SB} and the electrical length, depletion layer thickness, and hole injection phenomenon are illustrated in Table I. While the threshold voltage, in general, decreases with increasing V_{SB} bias, the trend becomes modest for short channel devices as the electrical channel length increases by a higher percentage.

The composite effect of V_{SB} on the threshold voltage, for a given technology, is defined by the factor γ where

$$\gamma = \frac{\Delta V_{T_{eff}}}{\Delta V_{SB}} \quad \text{at } V_{SD} = 0 \text{ V} . \quad (5)$$

The threshold voltage has been plotted against V_{SB} for various source-drain bias and different channel lengths. The extraction of the factor γ for a particular channel length and V_{SD} is done by taking a small change in the threshold voltage over a small change in V_{SB} at the particular V_{SB} of concern. The experimental γ values for various channel lengths were computed and plotted against V_{SB} to show a fairly linear

TABLE I
THE CORRELATIONS BETWEEN V_{SB} AND THE ELECTRICAL LENGTH, DEPLETION LAYER THICKNESS, AND HOLE INJECTION PHENOMENON

Source-Body Voltage $\uparrow$				
Channel Length	Electrical Channel Length	Depletion Layer Thickness	Hole Injection	Threshold Voltage
$> 0.6\mu\text{m}$	$\uparrow$	$\downarrow$	$\uparrow$	$\downarrow\downarrow$
$< 0.5\mu\text{m}$	$\uparrow\uparrow$	$\downarrow$	$\uparrow$	$\downarrow$

Fig. 4. The product γV_{SB} against the channel length for various V_{SB} bias.

response. Therefore, our model for γ takes the form $(\gamma_0 + \zeta V_{SB})$, where γ_0 is the y -intercept and ζ is the gradient. An iterative matching process was used to obtain the expression to model this composite effect. It was found that γ can be expressed as

$$\gamma = 0.22(1 - e^{-15L^3}) - \left(\frac{0.1}{L + 0.05} - 0.1 \right) V_{SB} \quad (6)$$

where L is in μm . The effect of the channel length and the source-body bias on the factor γ is illustrated in Fig. 4. The results show that the factor γ gets weaker for shorter channel lengths. However, for longer channel lengths, the product γV_{SB} increases by approximately 0.02 V for every 0.1 V increase in the source-body potential. The reasons for these changes can be explained as follows: Firstly, decreasing the body bias causes both the source-body and drain-body junctions to be more forward biased and less reverse biased, respectively. As a result, the depletion widths at the source and the drain decrease causing the electrical channel length to increase and consequently the threshold voltage to increase. On the other hand, and as the study in [9] indicates, as V_{SB} increases, the depletion layer thickness reduces and the threshold voltage decreases as a result.

The effect of the forward source-body bias on the threshold voltage for various channel lengths is shown in Fig. 5. The results show that increasing V_{SB} for the shorter channel lengths reduces the rate of decline of the threshold voltage

Fig. 5. The effect of V_{SB} on the threshold voltage.

before leveling off at high V_{SB} . This is because the changes in the threshold voltage due to both the reduction of the depletion layer thickness under the gate and the channel length modulation at the source and drain regions become comparable. However, the former effect prevails for longer channel lengths.

C. ΔV_{TH} Shift

The change in the threshold voltage, ΔV_{TH} shift, is defined as

$$\Delta V_{TH} = \eta V_{SD} + \gamma V_{SB}. \quad (7)$$

As depicted from Figs. 3(b) and 4, for $L = 0.4\mu\text{m}$, ΔV_{TH} increases by about 0.01 V and 0.08 V as V_{SB} changes from 0.3 V to 0.6 V and V_{SD} increases from 1 V to 2 V, respectively. However, for $L = 0.7\mu\text{m}$, the same changes in V_{SB} and V_{SD} bring about an approximate 0.06 V and 0.02 V increase in ΔV_{TH} , respectively. Further, and as illustrated in Fig. 6, while changing V_{SD} from 1 V to 2 V causes the threshold voltage to drop by about 3% and 14% for the $0.7\mu\text{m}$ and $0.4\mu\text{m}$ devices, respectively, an increase of 0.6 V in the forward source-body bias can reduce the threshold voltage by 13%–16% and 5%–8% for the $0.7\mu\text{m}$ and $0.4\mu\text{m}$ devices, respectively. Using these values as indicators, we can deduce that the DIBL effect gets stronger as the channel length is scaled down, while the V_{SB} effects dominate for longer channel lengths.

Fig. 6. The effect of scaling the channel length on the threshold voltage for two different values of V_{SD} and V_{SB} voltages.

IV. DEVICE CURRENTS: EXTRACTION, CHARACTERIZATION, AND MODELING

The device currents were extracted using the HP4156 precision semiconductor parameter analyzer. The measurement was performed on a vibration-free table with the probing station enclosed in a light shield box. In the hybrid-mode operation, where V_{SB} is forward biased, the total drain current I_{SD} is found to consist of three current components, namely: 1) the principal MOS current (I_{mos}), 2) the parasitic lateral bipolar current ($I_{bipolar}$), and 3) the space charge current (I_{space}).

While the space charge current is obtained by setting both the source-gate and source-body potentials to zero, and varying the source-drain voltage, the bipolar current is measured with the source-gate bias set to zero, sweeping the source-body potential from 0 to 0.6 V for various values of source-drain voltage, and subtracting away the corresponding space charge current. The MOS current is computed by subtracting both the space charge and the bipolar currents from the measured drain current at different source-gate, source-body, and source-drain voltages.

A. The MOS Current

The MOS current described here is derived based on the two-region piecewise carrier drift velocity model [10] and the engineering model for short-channel MOS devices [11]. However, these models do not consider the lowering of the barrier height at the source edge when the source-body is forward biased. To account for this effect, the factor $(1 + \lambda V_{SB,eff})$ was introduced. Therefore, the MOS current I_{mos} in the ohmic and saturation region is modified to [11], [12]

$$I_{mos}(tri) = \frac{\mu_{p,eff} C_{ox} W}{L_{eff}} \frac{1 + \lambda V_{SB,eff}}{1 + \frac{V_{SD,eff}}{E_c L_{eff}}} \times \left(V_{SG} - V_{T,eff} - \frac{1}{2} V_{SD,eff} \right) V_{SD,eff} \quad (8a)$$

$$I_{mos}(sat) = \frac{1 + \lambda V_{SB,eff}}{1 + \frac{V_{SD,eff}}{E_c L_{eff}}} v_{sat} C_{ox} W (V_{SG} - V_{T,eff}) \quad (8b)$$

Fig. 7. The analytical and experimental results of the MOS current in the ohmic and saturation regions.

where

$$L_d = L_{eff} - X_{dm} \quad (8c)$$

$$X_{dm} = \sqrt{\frac{2\epsilon_{si}}{qN_{sub}}} [V_{bi} - \phi_s + V_{SD,eff} - V_{SB,eff}] \quad (8d)$$

$$V_{bi} = V_t \ln \frac{N_{sub} N_a}{n_i^2} \quad (8e)$$

$$\phi_s = 2V_t \ln \frac{N_{sub}}{n_i} \quad (8f)$$

The parasitic source and drain resistances give a serious limitation to the current of drain engineered devices like the LDD. The classical way to account for this is by modeling the drain and source series resistances together with an intrinsic device [13] and using them to derive the MOS current. Another approach, adopted in this paper, is to modify the value of V_{SD} according to the physical and process parameters.

The experimental results show that $\lambda = 0.5$ gives the best fit for our MOS current model. Moreover, by setting $V_{SB,eff}$ to zero, (8a) and (8b) reduce to the conventional MOS currents given in the engineering model [11]. As depicted from (8a) and (8b), the MOS current is influenced explicitly through the factor $(1 + \lambda V_{SB,eff})$ and implicitly through the parameter γ of the threshold voltage. The factor $(1 + \lambda V_{SB,eff})$ accounts for the increasing hole injection into the channel region due to the lowering of the source-body barrier height. The analytical and experimental plots of the MOS current in the triode and saturation regions, illustrated in Fig. 7, were found to be in close agreement. The figure shows the extent of the further increase in the MOS current if scaling the channel length is coupled with a forward source-body bias.

A unified MOS current equation has been derived separately to generate a smooth transition between the triode and saturation regions and adapt the model to the SPICE environment. This equation is shown in (9) where α is a constant determining the width of the transition region between the linear and saturation regime. Although for small values of $V_{SD,eff}$, (9) does not have the same form as that of (8a), a reasonably good fit is obtained through proper selection of the

factor α . For large values of $V_{SD\text{eff}}$, (9) reduces to (8b)

$$I_{\text{mos}} = \frac{1 + \lambda V_{SB\text{eff}}}{1 + \frac{E_c L_d}{V_{SG} - V_{T\text{eff}}}} v_{\text{sat}} C_{\text{ox}} W (V_{SG} - V_{T\text{eff}}) \times \left[1 - e^{\frac{-\alpha \mu_p \text{eff} V_{SD\text{eff}}}{v_{\text{sat}} L_{\text{eff}}}} \right]. \quad (9)$$

B. The Bipolar Current

In very short channel MOS devices (less than sub-half micrometer channel length), and especially under forward source-body bias condition, the lateral bipolar action should be included in modeling the total drain current. Moreover, as the base (channel length) shrinks to dimensions of the same order of magnitude as the mean free path between collisions, the analysis of carrier flow by diffusion becomes questionable [14], [15]. A modified transport equation is given by [14], [16]

$$J_p = \frac{q\mu_p p E - qD_p \frac{dp}{dx}}{1 + \frac{D_p \frac{dp}{dx}}{p v_{\text{sat}}}}. \quad (10)$$

In the channel, $J_n = 0$ and the electric field E can be shown to be given by

$$E = -\frac{V_t}{n} \frac{dn}{dx}. \quad (11)$$

Since charge neutrality exists in the base region (n-well), and assuming the donor atoms to be fully ionized at room temperature, (11) can be rewritten as

$$E = -\frac{V_t}{N_{\text{sub}}} \frac{dp}{dx}. \quad (12)$$

Substituting (12) into (10) and integrating dx and dp from 0 to L_e and P_e to P_c , respectively, (10) becomes

$$J_p = q\mu_p V_t (P_e - P_c) \frac{\frac{P_e + P_c}{2N_{\text{sub}}} + 1}{L_e - \frac{D_p}{v_{\text{sat}}} \ln \frac{P_e}{P_c}} \quad (13)$$

where

$$L_e = L_{\text{eff}} - X_s - X_d \quad (13a)$$

$$X_s = \sqrt{\frac{2\epsilon_{\text{si}}}{qN_{\text{sub}}}} (V_{\text{bi}} - V_{j1}) \quad (13b)$$

$$X_d = \sqrt{\frac{2\epsilon_{\text{si}}}{qN_{\text{sub}}}} (V_{\text{bi}} - V_{j2}) \quad (13c)$$

$$V_{j1} = V_{SB\text{eff}} - I_S R_{\text{well}} \left[e^{\frac{V_{j1}}{n_f V_t}} - 1 \right] \quad (13d)$$

$$V_{j2} = V_{SB\text{eff}} - V_{SD\text{eff}} - I_S R_{\text{well}} \left[e^{\frac{V_{j2}}{n_f V_t}} - 1 \right]. \quad (13e)$$

(13d) and (13e) are transcendental equations which are solved by using numerical analysis techniques. For low level injection, (13) reduces to

$$J_p = \frac{q\mu_p V_t (P_e - P_c)}{L_e - \frac{D_p}{v_{\text{sat}}} \ln \frac{P_e}{P_c}} \quad (14)$$

where

$$P_e = \frac{n_i^2}{N_{\text{sub}}} e^{\frac{V_{SB\text{eff}}}{n_f V_t}}. \quad (14a)$$

Fig. 8. The bipolar and space charge currents of a 0.4 μm LDD pMOS device.

For very short channel lengths ($L < 0.4 \mu\text{m}$), and especially at large V_{SD} and V_{SB} , the two terms in the denominator of (14) become comparable in magnitude and a lower-bound for P_c is found to be

$$P_c = P_e e^{-\frac{L_e v_{\text{sat}}}{D_p}}. \quad (15)$$

Therefore, P_c can be expressed as

$$P_c = P_e e^{-\frac{\zeta L_e v_{\text{sat}}}{D_p}}, \quad \zeta < 1. \quad (16)$$

Substituting (16) into (14), the bipolar current can be shown to be

$$I_{\text{bipolar}} = \frac{q\mu_p V_t P_e A_{\text{bipolar}}}{L_e (1 - \zeta)} \left[1 - e^{-\frac{\zeta L_e v_{\text{sat}}}{D_p}} \right]. \quad (17)$$

In determining the factor ζ , a family of curves I_{bipolar} versus V_{SD} were obtained experimentally for various source-body bias and for different channel lengths. The values of ζ were first obtained by substituting for the parameters in (17) with their known values and then solving (17) iteratively. The results show that the factor ζ can be expressed as

$$\zeta = \frac{V_{SD\text{eff}}}{V_{SD\text{eff}} + 0.00016e^{7L}} \quad (18)$$

where L is in μm . The analytical and experimental plots of the bipolar current for a 0.4 μm LDD pMOSFET with different V_{SD} is shown in Fig. 8, where an excellent agreement is apparent. In Fig. 9, the effect of reducing the channel length on the MOS and bipolar currents is illustrated. Beside scaling the channel length, the other key device parameters such as the gate oxide thickness and the channel doping have been scaled according to [17]. The results show that for very short channel lengths, the contribution of the bipolar current to the total drain current becomes very significant.

In Fig. 10, the effect of L_e on the ratio P_c/P_e is shown. The results show that decreasing the channel length will cause the ratio P_c/P_e to increase substantially. This can be explained by the fact that decreasing the channel length will reduce the mean free path between collisions. The lateral bipolar current gain, β , (defined as the ratio of the bipolar current to the substrate current) of scaled LDD pMOSFET's for different

Fig. 9. The effect of scaling the channel length on the MOS and bipolar currents.

Fig. 11. The bipolar current gain as a function of the channel length.

Fig. 10. The analytical plot of the ratio P_c/P_e against the electrical channel length, L_e .

V_{SD} is illustrated in Fig. 11. A current gain higher than 1000 has been achieved for $L = 0.4 \mu\text{m}$ and $V_{SD} > 1.5 \text{ V}$. Similar findings were also reported in [1] and [2].

C. The Space Charge Current

It can be shown that in the very short channel length regimes and under high drain potential, even with no gate bias, carriers are swept from the source to the drain due to the high lateral electric field existing in the channel. This current, known as the space charge current [12], can be modeled as

$$I_{\text{space}} = \frac{m_1 A_{\text{space}} \epsilon_{\text{si}} \mu_p V_{\text{SDeff}}^2}{L_e^3}, \quad \frac{\mu_p V_{\text{SDeff}}}{L_e} \leq v_{\text{sat}} \quad (19a)$$

$$I_{\text{space}} = \frac{m_1 A_{\text{space}} \epsilon_{\text{si}} v_{\text{sat}} V_{\text{SDeff}}}{L_e^2}, \quad \frac{\mu_p V_{\text{SDeff}}}{L_e} \geq v_{\text{sat}} \quad (19b)$$

Fig. 12. The total drain current against the channel length for different values of V_{SB} and V_{SG} voltages.

where m_1 is the space charge current model fitting factor. The analytical and experimental plots of the space charge current for a $0.4\text{-}\mu\text{m}$ device for different V_{SD} are shown in Fig. 8. This current exhibits a square-law characteristics at low V_{SD} and becomes linear at high V_{SD} bias due to velocity saturation of carriers.

D. The Total Drain Current

The total drain current of a MOS device working in a Bi-MOS hybrid-mode environment can be expressed analytically as follows

$$I_{SD} = I_{\text{mos}} + I_{\text{bipolar}} + I_{\text{space}}. \quad (20)$$

To demonstrate the accuracy of the model, the total drain current was plotted for different channel lengths, two values of the source-body bias, and two values of the source-gate voltage. The agreement between the model predictions and the experimental results is evident from Fig. 12.

Fig. 13. The effects of both the channel length and the device potentials on g_{m1} .

V. DEVICE PARAMETERS

A. The Device Transconductance

The equation governing the device transconductances of a MOSFET operating in a Bi-MOS hybrid-mode environment is defined as (see Appendix A)

$$\Delta I_{SD} = g_{m1} \Delta V_{SG} + g_{m2} \Delta V_{SB} \quad (21)$$

where

$$g_{m1} = \frac{\delta I_{SD}}{\delta V_{SG}} \quad \text{at constant } V_{SB} \text{ and } V_{SD} \quad (21a)$$

$$g_{m2} = \frac{\delta I_{SD}}{\delta V_{SB}} \quad \text{at constant } V_{SG} \text{ and } V_{SD} \quad (21b)$$

$$\frac{\delta I_{SD}}{\delta V_{SG}} = \frac{\delta I_{mos}}{\delta V_{SG}} + \frac{\delta I_{bipolar}}{\delta V_{SG}} + \frac{\delta I_{space}}{\delta V_{SG}} \quad (21c)$$

$$\frac{\delta I_{SD}}{\delta V_{SB}} = \frac{\delta I_{mos}}{\delta V_{SB}} + \frac{\delta I_{bipolar}}{\delta V_{SB}} + \frac{\delta I_{space}}{\delta V_{SB}}. \quad (21d)$$

The experimental and analytical plots of g_{m1} are illustrated in Fig. 13. The results show that reducing the channel length if accompanied by a large V_{SD} could result in a further increase in the device transconductance. For short-channel devices operating in the hybrid-mode, and especially at high V_{SD} , the effect of g_{m2} on the change in the drain current cannot be neglected. As illustrated in Fig. 14 for $L = 0.4 \mu\text{m}$, g_{m2} could be 15% of g_{m1} when biased at $V_{SD} = 2 \text{ V}$ and $V_{SG} = 1.5 \text{ V}$.

B. The Output Conductance

The output conductance is defined as (see Appendix B)

$$\begin{aligned} g_{sd} &= \frac{\delta I_{SD}}{\delta V_{SD}} \quad \text{at constant } V_{SG} \text{ and } V_{SB} \\ &= \frac{\delta I_{mos}}{\delta V_{SD}} + \frac{\delta I_{bipolar}}{\delta V_{SD}} + \frac{\delta I_{space}}{\delta V_{SD}}. \end{aligned} \quad (22)$$

The effects of the device potentials and scaling the channel length on the output conductance both experimentally and analytically are shown in Figs. 15 and 16. As evident from these figures, g_{sd} increases, in general, with V_{SG} . While the

Fig. 14. The secondary transconductance against the channel length for two values of V_{SD} bias.

Fig. 15. The output conductance for different channel lengths and V_{SG} bias.

output conductance increases substantially with V_{SB} in the triode region, it remains fairly constant in the saturation region. However, it was found that for V_{SD} between 2.5 V and 3 V, there is a slight increase in the output conductance (about 1%–15%). This is attributed to the hot-carrier substrate current. For shorter channel length, the lateral electric field is able to sweep more carriers from the source to the drain across the channel. This, if coupled with a deeper inversion region when V_{SG} is increased will cause even more carriers to be swept from the source to the drain regions. It was also observed in Fig. 16 that increasing V_{SB} enhances the values of g_{sd} especially for shorter channel lengths ($L < 0.5 \mu\text{m}$) and lower V_{SD} values.

VI. CONCLUSION

The performance of CMOS-compatible lateral p-n-p BJT in a pMOS structure as a result of scaling, forward V_{SB} , and the combined effect of both has been studied. Both the experimental and analytical results show that while the drain-induced-barrier-lowering effect prevails in shorter channel lengths, the V_{SB} effects dominate in longer channel lengths.

Fig. 16. The effects of V_{SD} , V_{SB} , and the channel length on g_{sd} .

Although scaling increases the short-channel effects, increasing V_{SB} has the opposite effect. The space charge and bipolar currents have been found to increase with scaling the channel length and increasing the source-drain potential. It has been predicted that in the Bi-MOS hybrid-mode environment, if the channel length is reduced below $0.2 \mu\text{m}$, the bipolar and MOS currents become comparable. This mode of operation has been shown to add a second transconductance, the value of which increases with the device potentials and scaling the channel length. Further, the output conductance increases substantially, with V_{SB} , in the triode region, but remains relatively constant in the saturation region.

APPENDIX A THE DEVICE TRANSCONDUCTANCE

$$\frac{\delta I_{\text{mos(tri)}}}{\delta V_{SG}} = \frac{I_{\text{mos(tri)}}}{V_{SG} - V_{T_{\text{eff}}} - \frac{1}{2}V_{SD_{\text{eff}}}} \quad (\text{A1})$$

$$\frac{\delta I_{\text{mos(sat)}}}{\delta V_{SG}} = \frac{I_{\text{mos(sat)}}}{V_{SG} - V_{T_{\text{eff}}}} \frac{V_{SG} - V_{T_{\text{eff}}} + 2E_c L_d}{V_{SG} - V_{T_{\text{eff}}} + E_c L_d} \quad (\text{A2})$$

$$\frac{\delta I_{\text{bipolar}}}{\delta V_{SG}} = 0 \quad (\text{A3})$$

$$\frac{\delta I_{\text{space}}}{\delta V_{SG}} = 0 \quad (\text{A4})$$

$$\frac{\delta I_{\text{mos(tri)}}}{\delta V_{SB}} = \frac{I_{\text{mos(tri)}}}{1 + \frac{\Lambda_2 L_p}{t_c}} \left(\frac{\lambda}{1 + \lambda V_{SB_{\text{eff}}}} + \frac{\gamma - \left[\frac{0.1}{L+0.05} - 0.1 \right] V_{SB}}{V_{SG} - V_{T_{\text{eff}}} - \frac{1}{2}V_{SD_{\text{eff}}}} \right) \quad (\text{A5})$$

$$\frac{\delta I_{\text{mos(sat)}}}{\delta V_{SB}} = \frac{I_{\text{mos(sat)}}}{1 + \frac{\Lambda_2 L_p}{t_c}} \left(\left(\gamma - \left[\frac{0.1}{L+0.05} - 0.1 \right] V_{SB} \right) \times \left(\frac{2}{V_{SG} - V_{T_{\text{eff}}}} - \frac{1}{V_{SG} - V_{T_{\text{eff}}} + E_c L_d} \right) + \frac{\lambda}{1 + \lambda V_{SB_{\text{eff}}}} - \frac{E_c \epsilon_{\text{si}}}{q N_{\text{sub}} X_{\text{dm}} (V_{SG} - V_{T_{\text{eff}}} + E_c L_d)} \right) \quad (\text{A6})$$

$$\frac{\delta I_{\text{bipolar}}}{\delta V_{SB}} = \frac{I_{\text{bipolar}}}{1 + \frac{\Lambda_2 L_p}{t_c}} \left(\frac{\varsigma P_c \epsilon_{\text{si}} v_{\text{sat}} (X_s^* + X_d^*)}{q D_p N_{\text{sub}} X_s^* X_d^* (P_e - P_c)} + \frac{1}{n_f V_t} - \frac{\epsilon_{\text{si}} (X_s^* + X_d^*)}{q N_{\text{sub}} L_e X_s^* X_d^*} \right) \quad (\text{A7})$$

$$X_s^* = X_s \left[1 + \frac{I_s R_{\text{well}}}{n_f V_t} e^{\frac{V_{j1}}{n_f V_t}} \right] \quad (\text{A7a})$$

$$X_d^* = X_d \left[1 + \frac{I_s R_{\text{well}}}{n_f V_t} e^{\frac{V_{j2}}{n_f V_t}} \right] \quad (\text{A7b})$$

$$\frac{\delta I_{\text{space}}}{\delta V_{SB}} = \frac{I_{\text{space}}}{1 + \frac{\Lambda_2 L_p}{t_c}} \left(\frac{-3\epsilon_{\text{si}} (X_s^* + X_d^*)}{q N_{\text{sub}} L_e X_s^* X_d^*} \right) \quad \text{if } \frac{\mu_p V_{SD_{\text{eff}}}}{L_e} \leq v_{\text{sat}} \quad (\text{A8a})$$

$$\frac{\delta I_{\text{space}}}{\delta V_{SB}} = \frac{I_{\text{space}}}{1 + \frac{\Lambda_2 L_p}{t_c}} \left(\frac{-2\epsilon_{\text{si}} (X_s^* + X_d^*)}{q N_{\text{sub}} L_e X_s^* X_d^*} \right) \quad \text{if } \frac{\mu_p V_{SD_{\text{eff}}}}{L_e} \geq v_{\text{sat}} \quad (\text{A8b})$$

APPENDIX B THE OUTPUT CONDUCTANCE

$$\frac{\delta I_{\text{mos(tri)}}}{\delta V_{SD}} = \frac{I_{\text{mos(tri)}}}{1 + \frac{\Lambda_1 L_p}{t_c}} \left(\frac{V_{SG} - V_{T_{\text{eff}}} - (1 - \eta)V_{SD_{\text{eff}}}}{(V_{SG} - V_{T_{\text{eff}}} - \frac{1}{2}V_{SD_{\text{eff}}})V_{SD_{\text{eff}}}} - \frac{1}{E_c L_{\text{eff}} + V_{SD_{\text{eff}}}} \right) \quad (\text{B1})$$

$$\frac{\delta I_{\text{mos(sat)}}}{\delta V_{SD}} = \frac{I_{\text{mos(sat)}}}{1 + \frac{\Lambda_1 L_p}{t_c}} \left(\frac{-\eta}{(V_{SG} - V_{T_{\text{eff}}} + E_c L_d)} + \frac{2\eta}{V_{SG} - V_{T_{\text{eff}}}} + \frac{E_c \epsilon_{\text{si}}}{q N_{\text{sub}} X_{\text{dm}} (V_{SG} - V_{T_{\text{eff}}} + E_c L_d)} \right) \quad (\text{B2})$$

$$\frac{\delta I_{\text{bipolar}}}{\delta V_{SD}} = \frac{I_{\text{bipolar}}}{1 + \frac{\Lambda_1 L_p}{t_c}} \left(\frac{\epsilon_{\text{si}}}{q N_{\text{sub}} L_e X_d^*} + \frac{\varsigma}{V_{SD_{\text{eff}}}} + \frac{\varsigma v_{\text{sat}} P_c}{D_p (P_e - P_c)} \left(\frac{L_e (1 - \varsigma)}{V_{SD_{\text{eff}}}} - \frac{\epsilon_{\text{si}}}{q N_{\text{sub}} X_d^*} \right) \right) \quad (\text{B3})$$

$$\frac{\delta I_{\text{space}}}{\delta V_{SD}} = \frac{I_{\text{space}}}{1 + \frac{\Lambda_1 L_p}{t_c}} \left(\frac{2}{V_{SD_{\text{eff}}}} + \frac{3\epsilon_{\text{si}}}{q N_{\text{sub}} L_e X_d^*} \right) \quad \text{if } \frac{\mu_p V_{SD_{\text{eff}}}}{L_e} \leq v_{\text{sat}} \quad (\text{B4a})$$

$$\frac{\delta I_{\text{space}}}{\delta V_{SD}} = \frac{I_{\text{space}}}{1 + \frac{\Lambda_1 L_p}{t_c}} \left(\frac{1}{V_{SD_{\text{eff}}}} + \frac{2\epsilon_{\text{si}}}{q N_{\text{sub}} L_e X_d^*} \right) \quad \text{if } \frac{\mu_p V_{SD_{\text{eff}}}}{L_e} \geq v_{\text{sat}} \quad (\text{B4b})$$

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Samir S. Rofail (S'74–M'78–SM'86) received the B.Sc. degree in electrical engineering from Cairo University, Cairo, Egypt, and the B.Sc. degree in mathematics from Ain Shams University, Cairo, in 1971 and 1973, respectively. He received the M.A.Sc. and the Ph.D. degrees, both in electrical engineering, from the University of Waterloo, Waterloo, Ont., Canada, in 1975 and 1978, respectively.

He has been involved in teaching, research, and consultancy in the areas of the semiconductor devices and integrated circuits for the last eighteen years. He worked for Cairo University from 1971 to 1973, and for the University of Waterloo as a Research and Teaching Assistant from 1973 to 1978. He held faculty positions in the U.S., Saudi Arabia, and Canada. From 1990 to 1992, he was with the VLSI group of the University of Waterloo. He has been with Nanyang Technological University since 1992, where he is currently the Coordinator of the IC-design group. His research interests include the modeling of deep submicrometer MOSFET's, the IC-design of CMOS/BiCMOS circuits for low-voltage, low-power applications, and multiple-valued logic current mode circuits. He is a Technical Reviewer for several international journals and has published more than 25 journal papers, several of which are on IC-design for low-power environment.

Yeo Kiat Seng received the B.Eng. (Hons.) and Ph.D. degrees in electrical engineering from Nanyang Technological University, Singapore, in 1993 and 1996, respectively.

He joined Nanyang Technological University in 1993 as a Research and Teaching Assistant. In 1996, he was with the University as a Lecturer in the Division of Circuits and Systems. He has been extensively involved in the modeling and fabrication of small MOS/Bipolar integrated technologies for the last three years. His research interests also include the design of new circuits and systems (based on scaled technologies) for low-voltage low-power applications, IC-design of CMOS/BiCMOS multiple-valued logic circuit, domino logic, and memories. He has published more than 10 international journal papers.