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2010

Meaamar, A., Boon, C. C., Yeo, K. S., & Do, M. A. (2008). A Wideband Low Power Low-Noise Amplifier in CMOS Technology. IEEE Transactions on Circuits and Systems—I. 57(4), 773-782.

<https://hdl.handle.net/10356/92090>

<https://doi.org/10.1109/TCSI.2009.2028592>

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A Wideband Low Power Low-Noise Amplifier in CMOS Technology

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Abstract—A T-coil network can be implemented as a high order filter for bandwidth extension. This technique is incorporated into the design of the input matching and output peaking networks of a low-noise amplifier. The intrinsic capacitances within the transistors are exploited as a part of the wideband structure to extend the bandwidth. Using the proposed topology, a wideband low-noise amplifier with a bandwidth of 3–8 GHz, a maximum gain of 16.4 dB and noise figure of 2.9 dB (min) is achieved. The total power consumption of the wideband low-noise amplifier from the 1.8 V power supply is 3.9 mW. The prototype is fabricated in 0.18 μm CMOS technology.

Index Terms—T-coil network, feedback, bandwidth extension, gain-flatness, center-tap inductor, wideband low-noise amplifier (LNA).

I. INTRODUCTION

ULTRA-WIDEBAND (UWB) radio, potentially offers higher communication speeds than traditional narrowband transceivers. The advantage of the UWB transceiver over narrowband systems is low cost, low power, and high data rate due to the large bandwidth. A significant difference between traditional radio transmission and UWB radio transmission is that traditional communications systems transmit data by varying the power level, frequency, and/or phase of a sinusoidal wave. However, in UWB radio, data is transmitted either as impulse radio (IR) or multiband orthogonal frequency division multiplex (OFDM). The IR UWB transmits data based on the transmission of very short pulses. In some cases, impulse transmitters are employed where the pulses do not modulate a carrier. This technique results in lower-data rate and -design complexity compared to the OFDM system. On the other hand, in the multiband OFDM technique each band with 528 MHz width encodes the data using QPSK modulation. Using this technique a data rate of 480 Mb/s can be achieved. However, the design of this system is more challenging.

One of the major challenges in wideband communications systems is the design of a wideband low-noise amplifier (LNA). As the first active component in the receiver chain, the LNA should offer sufficient gain and low noise to keep the overall receiver noise figure as low as possible. In most applications, it is desirable to obtain wideband on-chip input matching to a 50 Ω antenna/filter, good linearity, and low power consumption. In addition, gain-flatness over the entire frequency range of interest is necessary to meet the

design specifications. These properties are the cornerstones of the wideband LNA design which affect the total broadband communication system characteristics.

The cost and integration advantages of CMOS technology have motivated extensive studies in the high speed CMOS design for wireless applications. Recently, many wideband LNA designs in CMOS technology have been reported [1]–[4]. The wideband LNA designs can be classified as multi-band LNAs, distributed amplifiers (DA), and broadband noise canceling LNAs. Among wideband LNA designs, distributed and common-gate amplifiers suffer from high noise figure. Alternatively, the feedback amplifier topology provides wide bandwidth while reducing the gain of the circuit. Another important property of the negative feedback is the suppression of the nonlinearity. However, in feedback circuits the stability may suffer if the loop gain is too high which the phase margin reaches -180° or the phase margin is so much that the feedback becomes positive. Therefore, compensation techniques are required to eliminate the instability problem. In the noise canceling technique reported in [3], 5 inductors are used and the noise figure is 4.5–5.1 dB from 1.2–11.9 GHz with 20 mW power consumption, which makes it unattractive for low cost, low power applications. In [2], several narrowband amplifiers with different resonance frequencies are cascaded. Therefore, the resulting multistage amplifier provides a broadband response. This circuit required 8 inductors in a differential architecture and since many stages are cascaded it is prone to poor linearity and stability problems.

This paper introduces a T-coil network to achieve wideband input matching and wideband output response. In this technique the parasitic capacitors of the transistors and inherent mutual inductance of the inductors are taken as a part of the design [4]. In this work 3 inductors are used which 2 of inductors are center-tap inductor. Section II will cover the basic concepts of inductive peaking circuits. In section III, the T-coil network technique is utilized in a cascode amplifier to realize the wideband LNA for the UWB/multiband applications. In section IV, an example based on the proposed technique is presented along with experimental results.

II. CIRCUIT DESIGN: THEORY AND PRACTICE

In [5], a Chebyshev type bandpass filter is used at the input of a common-source amplifier in order to provide good matching over a wide bandwidth. These kind of filters necessitate the use of many components which occupy a large area and reduce the circuits integration level. Furthermore, the loss associated with the components deteriorates the noise

Fig. 1. Common-source amplifier with output parasitic capacitance C_p

figure of the circuit. Therefore, techniques to alleviate these issues without degrading performance is required.

In general, when the LNA circuit is cascaded to the next stage, the interstage parasitic reactance attenuates the desired bandwidth of the LNA. For example, in Fig. 1 parasitic gate-source capacitance C_p of a mixer or buffer, reduces the circuit performances as it shunts with the output load R of the common-source amplifier. A dominant pole due to the parasitic C_p is created at frequency of $1/RC_p$ which reduces the bandwidth. One way to compensate C_p is to insert an inductor in series with R at the output of Fig. 1 to resonate out C_p . However, the existence of resistor R will require extra voltage headroom, which limits the allowable bias current. In the discussions below, different peaking techniques are introduced to improve the bandwidth.

Shown in Fig. 2(a), a series inductor L across R and C is used to create a series peaking in the frequency response. The series inductor creates a second-order RLC resonant circuit with a resonance frequency of $\omega_0=1/\sqrt{LC}$. In this circuit transfer function is not changed by exchanging R and C since L is in series with C in both cases. The transfer function of the series inductive peaking circuit is

$$H_1(s) = \frac{R}{s^2LC + sRC + 1} = \frac{1}{mR^2C^2} \cdot \frac{R}{s^2 + s/mRC + 1/mR^2C^2} \quad (1)$$

where $L = mR^2C$, m is a dimensionless parameter that defines the poles location and determines the overdamped response of the filter. From (1), the complex conjugate poles are

$$s_{1,2} = -\frac{1}{2mRC} \pm j\sqrt{\frac{1}{mR^2C^2} - \frac{1}{4m^2R^2C^2}} = \frac{1}{2mRC} (-1 \pm j\sqrt{4m-1}). \quad (2)$$

From the frequency response shown in Fig. 2(b), the circuit including the series peaking inductor improves the bandwidth compare to the circuit without L . For this circuit with $m = 0.25$ poles are equal to $s_1 = s_2 = -2/RC$ near to the critically damped response. As the value of m increases ($m > 0.25$) poles become complex conjugate and travel along the real axis towards the $j\omega$ axis, Fig. 2(c). If we equate the standard 2nd-order Butterworth poles with (2), the components values are calculated and maximum gain-flatness response is satisfied. As shown in Fig. 2(c), poles angle (φ) should be equal to 45° from origin to get the maximum gain-flatness response [6]. The circuit in Fig. 2(a) with two reactance components represents one resonance frequency. The circuits

Fig. 2. (a) Series inductive peaking circuit, (b) frequency response of the circuit (a) with and without L , (c) complex poles location for maximum gain-flatness response, (d) shunt-series inductive peaking circuit, (e) frequency response of the shunt-series peaking circuit, (f) series-shunt-series peaking including a T-coil peaking network, (g) series-shunt-series peaking frequency response.

with more than two reactance components have more than one resonance mode. A multi-resonance circuit can be utilized to cover a wider range of frequency than a single resonance circuit. For this reason, the resonance frequencies should be chosen properly to optimize the bandwidth of interest.

Now consider the circuit shown in Fig. 2(d). An inductor L_a in series with R adds a shunt peaking to the series peaking L_b , results in a shunt-series peaking circuit which improve the bandwidth. The frequency response of this circuit is shown in Fig. 2(e). The transfer function of the shunt-series peaking network is determined as

$$H_2(s) = \frac{V_o}{I_{in}} = \frac{sL_a + R}{s^2C(L_a + L_b) + sCR + 1} = \frac{1}{C(L_a + L_b)} \cdot \frac{sL_a + R}{s^2 + sR/(L_a + L_b) + 1/C(L_a + L_b)} \quad (3)$$

where from denominator, the complex poles are

$$s_{1,2} = \frac{-R}{2(L_a + L_b)} \pm j\sqrt{\frac{1}{(L_a + L_b)C} - \left(\frac{R}{2(L_a + L_b)}\right)^2} \quad (4)$$

The inductor L_a in series with R adds a real zero $-R/L_a$ to the numerator of the transfer function in (3). The addition of a zero improves the bandwidth but also peaks the response. To reduce the peaking issue in the frequency response of Fig. 2(e), the components values are equated to the standard 2^{nd} -order polynomial normalized Butterworth system. For this reason, let us normalize the transfer function $H_2(s)$ by putting $R = 1$ and $C = 1$ and then

$$\begin{aligned} L_a &= m_1 R^2 C \\ L_b &= m_2 R^2 C, \quad m_2 < m_1 \end{aligned} \quad (5)$$

where L_a and L_b are selected to get the maximum gain flatness. Note that in this paper we are trying to keep an agreement between the bandwidth and the gain flatness.

Combining the circuits in Fig. 2(a) and Fig. 2(d), a series-shunt-series circuit which involves a T-coil network (L_{a-c}) is resulted in Fig. 2(f). The parasitic capacitors C_1 and C_2 are separated by the T-coil network (L_{a-c}). The transfer function of this circuit is the product of the transfer function in (1) and (3). For simplicity of the analysis, R_b is neglected (as $R_b \gg R_a$) and two valid cases are assumed. The first case is when the input impedance $Z_i = R_a$, and the second case is when $Z_i = R_a + jb$. For the first case it can be seen intuitively that at low frequencies the inductors short the input to R_a while the capacitors are open. For higher frequencies Z_i contains the imaginary part jb due to the existence of the passive components. So the transfer function for the case 1 and 2 are consecutively as follow

case1:

$$\begin{aligned} H_1(s) &= \frac{R_a / m_1 R_a^2 C_1^2}{s^2 + s / m_1 R_a C_1 + 1 / m_1 R_a^2 C_1} \\ &\times \frac{m_1 (s + 1 / m_1 R_a C_1) / C_2 (m_1 + m_2)}{s^2 + s / R_a C_2 (m_1 + m_2) + 1 / R_a^2 C_2^2 (m_1 + m_2)}. \end{aligned} \quad (6)$$

case2:

$$\begin{aligned} H'_1(s) &= \frac{(R_a + jb) / m_1 (R_a + jb)^2 C_1^2}{s^2 + (s + 1 / C_2 (R_a + jb)) / (R_a + jb) (m_1 + m_2)} \\ &\times \frac{m_1 (s + 1 / m_1 R_a C_1) / C_2 (m_1 + m_2)}{s^2 + (s + 1 / C_2 (R_a + jb)) / C_2 (R_a + jb) (m_1 + m_2)}. \end{aligned} \quad (7)$$

The denominator of (6), includes four poles given by

$$s_{1,2} = \frac{1}{2R_a C_1 m_1} (-1 \pm j\sqrt{4m_1 - 1}). \quad (8)$$

and

$$s_{3,4} = \frac{1}{2R_a C_2 (m_1 + m_2)} (-1 \pm j\sqrt{4(m_1 + m_2) - 1}). \quad (9)$$

In (6), two left hand complex poles extend the bandwidth much further compared to the poles in (3), because the circuit in Fig. 2(f) represents more than one resonance mode. Assuming $C_2 > C_1$ so poles $s_{1,2}$ are located at higher frequency than poles $s_{3,4}$. Fig. 2(g) illustrates the frequency response improvement of the circuit in Fig. 2(f). If we replace R_a in (8) and (9) by $R_a + jb$, the poles of (7) are obtained. A similar circuit to Fig. 2(f) is presented in [7] which the

transfer function of the circuit is normalized to find the relation between the components for maximum bandwidth.

III. WIDEBAND AMPLIFIER DESIGN

In this section the series-shunt-series circuit in Fig. 2(f) is applied to a common-source amplifier to realize a wideband LNA design.

A. Output Peaking Network

The use of 3 inductors in Fig. 2(f) leads to difficulties in the layout. Fortunately, this issue can be resolved through implementation of a center-tap (CT) inductor. The circuit shown in Fig. 3(a) is a common-source amplifier incorporating the CT inductor with a magnetic coupling coefficient k between L_1 and L_2 to form the T-coil peaking network at the output network. The basic functionality of this T-coil network is similar to the circuit in Fig. 2(f) that was explained above. The CT inductor is employed to save die area and reduce the loss associated with the inductors. The CT inductor with the negative mutual coupling ($-M$) leads to greater improvements compare to the circuit in Fig. 2(f).

Since only one CT inductor is used in Fig. 3(a), less parasitic components are introduced to the circuit. The equivalent small-signal model of the output peaking network is shown in Fig. 3(b). Since $C_2 > C_1$ we assume that $C_2 = (1 + \alpha)C/2$ and $C_1 = (1 - \alpha)C/2$, where $0 < \alpha < 1$. The CT inductor in this network has a symmetrical structure, hence $L_1 = L_2 = L$, $k = M/L$ and from here $L_X = L_Y = L(k + 1)$ and $L_Z = -kL$. The mutual coupling between L_1 and L_2 as an extra term can be exploited to modify the bandwidth extension. In order to optimize the required gain-flatness over the entire bandwidth, k -factor should be determined precisely. For this reason, the relationship between group-delay and the k -factor of the T-coil network (Fig. 3(a)) is simulated in Fig. 4. In this simulation the loss of the inductors are included into the circuit model to get more accurate results. As the k -factor increases, flatter group delay over wider bandwidth is resulted. In addition, the total attenuation of the symmetric T-coil network at different frequencies versus k -factor is plotted in Fig. 5. As the frequency increases, the attenuation of the T-coil network increases simultaneously. Therefore, a higher k -factor is required to reduce the attenuation specially at high frequencies. However, the design of a CT inductor to present a very high k -factor is not easy. The reason is that the k -factor is limited by the parasitic capacitances and resistances of the inductor. To eliminate the nonideal characteristic of the inductor, stacked top metal layers are implemented while the center-to-center distance of the turn-to-turn winding should be reduced [8]. More importantly, if the parasitic capacitances of the output CT inductor become significant, more parasitic capacitances are added to C_1 , which makes C_1 comparable with C_2 . This reduces the desirable bandwidth and makes the bandwidth extension technique inefficient. It is shown in the subsequent section that by increasing C_2/C_1 ratio the bandwidth is further improved. Fig. 6 plots the attenuation of the output T-coil network versus frequency for $k=0.5$ and 0.9 , respectively. The attenuation is more gradual for $k=0.9$

Fig. 3. (a) Common-source amplifier with symmetric T-coil peaking network, (b) simplified small-signal equivalent circuit of the T-coil peaking

Fig. 4. Group delay response of the T-coil network.

and its deviation from 3 to 8 GHz is about 1.8 dB which is flatter compared to the attenuation of $k=0.5$.

Now, in order to prove the feasibility of the technique explained above, the T-coil peaking network is implemented in a cascode amplifier. Fig. 7 shows the complete single-ended cascode LNA with the CT inductor at the input and the output of this circuit. An extra peaking inductor L_L is added into the output peaking network as a part of the load, to prevent

Fig. 5. Amplitude response of the T-coil network vs. k -factor at different frequencies.

Fig. 6. Amplitude response of the T-coil network vs. frequency.

the gain roll-off and to improve the gain-flatness. A resistor R at the output load in series with L_L reduces the quality factor of this inductor which extends the bandwidth of the LNA. However, the existence of R causes some drawbacks like peaking in the gain response and additional noise. In order to reduce the peaking in the gain response, a resistive-feedback path is connected across nodes “A” and “B”. In Fig. 8 the frequency response of the wideband LNA with/without the feedback path is simulated. Clearly, the peaking issues are minimized due to the feedback path effect. That is, R_F moves the complex conjugate poles away from $j\omega$ axis to get $\varphi = 45^\circ$. Therefore, proper selection of R_F value is critical to minimize the peaking in the frequency response. If the series parasitic resistance of the output inductors are high enough (low Q inductors), R can be removed from the output peaking circuit.

B. Input Matching Network

Shown in Fig. 9 is the equivalent circuit model of the LNA input matching network. The input matching network

Fig. 7. Wideband LNA using symmetrical center-tap inductor (biasing circuitry not shown).

Fig. 8. Simulated frequency response of the LNA, in here $R = 0$. The wideband LNA with/without feedback path is simulated for comparison, the 3 dB bandwidth is adjusted later.

is implemented using T-coil network, similar to the output peaking network. This technique helps to minimize the number of inductors at the input stage. The input impedance of this circuit is expressed as

$$Z_{IN} = (sL_X + r_X) + \left[sL_Z + \left(\frac{R_F}{1 - A_v} \right) \right] \parallel \left[sL_Y + r_Y + \frac{1}{s(C_{gs} + C_\mu)} \right]. \quad (10)$$

where A_v is the open loop voltage of the amplifier, r_X , r_Y are the loss associated with L_X , L_Y , respectively and C_μ

Fig. 9. Input impedance equivalent network of the LNA.

is the Miller capacitor. The real part of (10) is defined as $R_s = \Re(Z_{IN})$ where $\Re(Z_{IN})$ is directly dependant to R_F . Regardless of the loss associated with the inductors, the input resistance of the LNA is approximated by $R_{in} = R_F / (1 - A_v)$, which introduces a low input impedance and reduces the effect of input dominant pole

$$s_{in} = \frac{1}{R_{in}(C_B + C_{gs} + C_\mu)} = \frac{|A_v|}{R_F(C_B + C_{gs} + C_\mu)}. \quad (11)$$

where $R_{in} \approx R_F / |A_v|$ if $A_v \gg 1$. The input matching network is implemented as bandpass filter. The tuning condition of the filter is dependant to the proper value of the components. For instance, the right selection of the blocking capacitor C_B is very important because a large value of C_B adds to the overall parasitic capacitance at the input, affecting the overall bandwidth of the circuit. A small value on the other hand, has significant AC impedance that leads to the gain reduction.

The quality factor (Q) of the input network is given by

$$Q_T = \frac{1/\omega_0((C_{gs} + C_\mu) \parallel C_B)}{\left[R_s + r_X + r_Y + \frac{\omega_0^2(L(k+1))^2}{R_P} \right]}. \quad (12)$$

where resistor $R_P = (R_F / (1 - A_v))(1 + Q_{L_Z}^2)$ is the parallel equivalent resistance of the inductor L_Z , and ω_0 corresponds to the resonance frequency of the network as

$$\omega_0 = \frac{1}{\sqrt{((C_{gs} + C_\mu) \parallel C_B)[L_X + (L_Z' \parallel L_Y)]}}. \quad (13)$$

As k -factor of the input CT inductor increases, the attenuation reduces and the input network bandwidth increases. By tuning R_P in (12), Q_T of the input network would be tuned and desired input matching can be obtained. Note that the tradeoff between the input matching and the noise figure should be considered when the value of k -factor is selected. From (13), it is seen that the parasitic $C_{gs} + C_\mu$ can be tuned out with proper selection of the components values.

C. Noise Analysis

There are many factors which may directly affect the NF of the proposed LNA design. The input impedance matching network, feedback resistor, biasing circuitry and drain current

Fig. 10. Simplified small-signal model of Fig. 3(a), noise contribution of M_2 is ignored.

noise of the MOS device M_1 , are the major contributors. In saturation, the drain current noise is mainly due to the drain current and weakly is dependant to drain voltage [9]. The output load resistance and the output buffer, which generally assumed to have insignificant noise contribution, also add to the NF. The parasitic components of the input CT inductor which reduce Q_T of the matching network and channel length effect of the transistor M_1 are inevitable issues, which need careful design strategies to overcome. Since the noise contribution of the cascode transistor M_2 is negligible, its noise effect is neglected [10].

The equivalent small signal noise model of the wideband LNA is shown in Fig. 10. Since the mutual coupling M between two halves of the inductors is noiseless, the effect of $L_Z = -M$ is neglected in the NF calculations. By solving the small-signal model for $Z_{IN1} = R_s$ at resonance and following the noise calculation method explained in [11], we get

$$F = \frac{R}{R_s} \left(1 + \frac{R}{R_s} \frac{\omega_0^2 R_s g_m \gamma}{\omega_{T0}^2 \alpha} \chi \right). \quad (14)$$

where,

$$\chi = \frac{\delta \alpha^2}{5\gamma} [1 + Q_T^2] + 1 - 2|c| \sqrt{\frac{\delta \alpha^2}{5\gamma}}. \quad (15)$$

$$R = R_s + R_{EQ}, \quad \alpha = \frac{g_m}{g_{d0}}, \quad \omega_{T0} = \frac{g_m}{C_{gs} + C_\mu}. \quad (16)$$

$$R_{EQ} = R_g + r_X + r_Y + \frac{(L_X \omega_0)^2}{R_F / 1 - A_v}. \quad (17)$$

where $\delta \approx 1.33 - 4$, $\gamma \approx 0.67 - 1.33$ are excess noise parameters, $c \approx j0.4$ [10], and g_{d0} is the channel conductance at $V_{DS} = 0$. For the noise analysis, parasitic resistances of L_X , L_Y , and gate resistance of the transistor M_1 are lumped into R_{EQ} . In order to determine the NF contribution due to R_F , the open loop gain A_v is assumed to be consistent across the bandwidth. An increase in R_F reduces noise linearly. However, an increase in R_F pushes the input dominant pole in (11) to a lower frequency. The NF can be lowered by choosing the right value of R_F which alters Q_T in (15). Given in (16), ω_{T0} increases as the transconductance increases and consequently improves the NF. Any extra physical input resistance r_g adds an additional term of r_g/R_s to (14). Since only one CT inductor is employed at the input of the LNA, less loss is contributed to the NF.

D. Design Sensitivity to Process Variations

Due to the frequency and process dependency of the components, variations in the design specifications are expected. In this part susceptibility of the LNA to these variations and its effect on the performances is briefly evaluated. For instance, mismatch between the components in the input matching network, frequency dependency of the components, modeling inaccuracy and manufacturing variations as technology scales, are the important parameters which increases the design sensitivity. In this wideband LNA, the gain, NF, and linearity specifications are constrained to be met with minimum power consumption. A key parameter that degrades the NF of the amplifier is the noise resistance R_n which is investigated in [12]. Clearly, by reducing R_n the NF improves to some extent. In Fig. 11 variation of the measured R_n versus frequency is plotted. The bias current constraint is kept to less than 3.5 mA. Since the width (W) of the device is inversely proportional to R_n [12], proper selection of W results in an optimum value of R_n that reduces the variation of the noise figure (ΔNF). However, the device size cannot be made arbitrarily larger to make R_n smaller because the parasitic C_{gs} increases as W increases. As shown, the variation of normalized R_n in this design is less than 0.8Ω over a wide range of frequency at three different DC currents. It is noted that the variations of R_n is almost constant over the wide range of frequency. As a conclusion, since the variations of R_n are the same for 3 different currents, we cannot improve the NF necessarily from this point of view in this design.

The mismatch between the components degrade the gain and high frequency performances of the LNA. The focus in here is mainly on the sensitivity of the gain and noise figure to the parameters variations. Basically, with a higher voltage gain, a better NF performance can be resulted. On the other hand, this LNA is designed to be used with a mixer, and high gain LNA reduces the linearity of the whole design (LNA+Mixer). Therefore, LNA should meet the tradeoff between all the design characteristics. To gain more insights, we would calculate the voltage gain of the LNA. To derive the voltage gain of the amplifier, notice that R , L_L , which are in series with L_2 , and the parasitic C_1 are neglected and $L_1 = L_2 = L$. The overall gain is

$$\frac{v_{out}}{v_s} = \frac{-g_m}{sC_{gs}(R_s + Z_{IN})} \cdot \frac{(R_F \parallel sL)}{s^2 L_Z C_2 + sC_2(R_F \parallel sL) + 1}. \quad (18)$$

where $v_s = i_s R_s - v_{in}$ and assuming $i_{d1} \approx i_{d2}$, then the output current i_{d1} is $v_s \cdot g_m / sC_{gs}(R_s + Z_{IN})$. Equation (18) shows that the gain rolls-off if C_{gs} is large. The impact of C_{gs} is reduced with higher f_T or reduction of the mismatch between the input matching components to guarantee that C_{gs} is resonated out over the frequency of interest. Moreover, the output capacitor C_2 causes reduction in the voltage gain. The reduction in the voltage gain would increase the NF. These parameters should be considered to keep the agreement between the gain and NF performances.

Fig. 12 is plotted to show the sensitivity of the NF to 20% devices variations at 3.2 mA current consumption. As shown

Fig. 11. Variations of normalized R_n with three different currents vs. frequency.

Fig. 12. Device variations effect on the noise figure performance.

in the solid line plot, the worst case in the NF degradation is when W of the transistor M_1 and $L_{3,4}$ are increased (20%) and an extra pad capacitor is added to the circuit. This plot shows that the NF has a better performance at the frequencies lower than 5.5 GHz compared to the case when no variation is applied. This difference is due to the higher current from the larger device size. It should be noted that the frequency at which the minimum sensitivity to process variations in NF is observed (about 5.75 GHz from Fig. 12), is very close to the frequency at which the minimum value of R_n occurs (5.5 GHz in Fig. 11). However, the NF degrades at frequencies higher than 5.8 GHz due to the reduction in the gain and Q -factor of the inductors. The deterioration of the noise figure at higher frequencies is partially due to the gate resistance noise and gate induced noise (both are $\propto f^2$) [10].

IV. EXPERIMENTAL RESULTS

From the discussion above, a wideband LNA with the bandwidth of 3.168–7.920 GHz is designed for the multiband

TABLE I
COMPONENT VALUES OF THE LNA

$(W/L)_{M_1}$	$(W/L)_{M_2}$	$L_{1,2}^*$	$L_{3,4}^*$	L_L	R_F
120/0.18	40/0.18	9 nH	2.92 nH	1.31 nH	1.14 kΩ

* $L_{1,2}$ and $L_{3,4}$ are the center-tap inductor.

Fig. 13. Contour plots of α variation (variation of the next stage parasitic capacitance) and its effect on the gain peaking vs. frequency.

OFDM standard. The components values are listed in Table I. The size of M_1 is selected properly to get low current consumption. From simulation, this wideband LNA provides a maximum gain of 20 dB with maximum NF of 2.9 dB under 2.2 mA current consumption. Since the sum of series parasitic resistances of the output inductors $L_L + L_{1,2}$ is high enough, which is about 55 Ω at 7 GHz, R in Fig. 7 was removed from the final design. This enables the transistors to have enough voltage headroom with the optimum device size which efficiently reduces the current consumption of the LNA. In addition, it improves the gain and the NF without extra current consumption.

By the size of the transistor M_1 , the parasitic C_{gs} can be found out. From the blocking capacitor C_B of 1 to 2 pF, the value of the input CT inductor is determined to get the desirable input matching. On the other hand, the size of M_2 determines the parasitic capacitance C_1 at the output network. The output response of Fig. 7 is simulated in Fig. 13 to show the different loading (C_2) effects. As α increases, $C_1 = (1 - \alpha)C/2$ reduces and $C_2 = (1 + \alpha)C/2$ increases. As shown in Fig. 13, with a reduction in C_1 and an increase in C_2 , the output T-coil network exhibits larger bandwidth with smaller peaking especially when C_2 dominates ($\alpha = 0.9$). So the size of M_2 is selected to be much smaller than the size of M_1 , to decrease the parasitic C_1 and to reduce the peaking in the response at high frequencies. Since this wideband LNA will be interfaced with a mixer in the UWB design, the input capacitance of the I/Q downconversion mixer should be taken into account as it determines the gain-flatness of the LNA. In this design, a current reuse buffer is implemented to obtain 50 Ω output matching for the measurement purposes. The loading effect of the buffer is determined to be about the same

Fig. 14. Die micrograph of the wideband LNA.

Fig. 16. Measured and simulated S_{22} and S_{12} of the LNA vs. frequency.

Fig. 15. Gain and input reflection coefficient of the LNA vs. frequency.

Fig. 17. Simulated IIP3 at 6.5 GHz.

as the mixer loading effect on the LNA stage.

The prototype of the wideband LNA is fabricated in a six-metal $0.18 \mu\text{m}$ CMOS technology. The die micrograph is shown in Fig. 14. The total die area including the output buffer is $0.76 \times 0.81 \text{ mm}^2$. The inductors are mounted on the pattern ground shield structure for better efficiency [13]. The empty spaces are covered with metal-filling to reduce the process variations effects. The transistors M_1 and M_2 are divided into six units to reduce the gate parasitic resistance. The simulated and measured results of the S-parameters are plotted in Fig. 15 and Fig. 16, respectively. The measured gain has a maximum peak of 16.4 dB from 3.19 to 3.8 GHz frequency. The gain-flatness of 2.1 dB from 4 to 7.6 GHz frequency is obtained with 2.16 mA current consumption. The gain rolls-off by 3.5 dB from 7.6 to 8 GHz frequency. This drift can be corrected by adjusting the inductors in the subsequent silicon iteration. The measured input reflection coefficient is well below -10 dB for the entire operating frequencies. As explained before, the output matching of the LNA is set by a current reuse buffer just for the test purposes. The comparison

between the measured and simulated S_{22} and S_{12} is plotted in Fig. 16.

The third order input intercept point (IIP3) is simulated versus different frequencies. Fig. 17 plots an IIP3 of -3.2 dBm at 6.5 GHz frequency. Two-tone test is used to simulate the IIP3 with 1 MHz frequency space between the tones.

The simulated and measured NF over the bandwidth is shown in Fig. 18. Several dies were measured and mean value of the NF is plotted. The difference between the measured and simulated NF is owed to the process variations as explained before. A minimum NF of 2.7 dB is measured at 2.8 GHz and the NF at 3 GHz is 2.9 dB. The maximum NF is 4.66 dB at 7 GHz and it falls to 3.8 dB at 8 GHz frequency. Fig. 19 depicts the measured quality factors of the input and the output inductors. The Q -factor of the input inductor effects the NF directly. The measured Q -factors are $8 < Q_{L_L} < 11.8$, $8.8 < Q_{L_{1,2}} < 10.7$, and $11.5 < Q_{L_{3,4}} < 13.9$ for 3–8 GHz frequency. A high Q inductor at the input is chosen for better NF, and lower Q inductors at the output were used for the gain-bandwidth tradeoff. Table II indicates the performance comparisons of the proposed wideband LNA with prior works.

TABLE II
WIDEBAND LNA PERFORMANCE SUMMARY AND COMPARISON

Reference	Technology	BW (GHz)	S11 (dB)	Gain _{max} (dB)	NF (dB)	IIP3 (dB)	Power (mW)	Area(mm ²)	FOM
This work	0.18 μ m CMOS	3–8	<-10	16.4	2.9–4.66	-2.2 to -4.3*	3.9	0.62	4.4–8.9
[5] STD	0.18 μ m CMOS	2.3–9.2	<-9.9	9.3	4–8	-6.7 [†]	9	1.1	0.3–1.5
[5] TW	0.18 μ m CMOS	2.4–9.5	<-9.4	10.4	4.2–8	-8.8 [†]	9	1.1	0.49–1.6
[3]	0.18 μ m CMOS	3.1–10.6	<-11	9.7	4.5–5.1	-6.2	20	0.59	0.5–0.6
[7] LNA#2	0.18 μ m CMOS	1.3–12.3	<-9	8.2	4.6–5.5	7.6–9.1	4.5	1	2.69–3.64
[14]	0.18 μ m SiGe	3–10	<-10	21	2.5–4.2	<-1 [‡]	30	1.8	1.6–3.4
[15]	0.18 μ m CMOS	0.4–10	<-10	12.4	4.4–6.5	-6	12	0.42	1–1.99
[16]	0.18 μ m CMOS	2.8–7.2	–	19.1	<3.8	-1 [§]	32	1.63	0.88
[17]	0.13 μ m CMOS	1.5–8.1	<-9	11.7	3.6–6	11.7–14.1	2.62@1.3V	0.58	3.25–7.5
[18]	0.18 μ m SiGe/CMOS	0.1–11	<-12	8	2.9	-3.55	21.6	0.76	1.3
[19]	65 nm CMOS	0.2–5.2	–	15.6	<3.5	>0	14@1.2V	0.009	1.7
[20]	0.18 μ m CMOS	0.048–1.2	-9	14 [×]	3 [◇]	3 [◇]	15.8@2.2V	0.37	1.84
[21]	0.13 μ m CMOS	0.8–2.1	-8.5	14.5	2.6	+16	17.4@1.5V	0.0992	0.48
[22]	0.13 μ m CMOS	3.1–10.6	<-9.9	16.5	2.07–2.93	-5.1 to -8.5 [◊]	9@1.2V	0.87	5.78–9.1

* at 3–8 GHz. [†] at 6 GHz. [‡] at 5.4 GHz, 5.6 GHz. [◊] at 4–8 GHz. [§] at 6 GHz. [×] power gain. [◇] at maximum gain.

Fig. 18. Simulated and measured noise figure of the wideband LNA.

Fig. 19. Measured quality factor of the inductors.

A figure-of-merit (*FOM*) is used here to compare the performance of different LNAs with similar functionality. The *FOM* in here evaluates the gain, -3 dB bandwidth, excess noise factor and power consumption of the LNA which is defined as

$$FOM = \frac{|S_{21}| BW_{GHz}}{(F - 1) P_{mW}}. \quad (19)$$

Based on the *FOM* calculated in Table. II, the proposed wideband LNA shows comparable performances to the other designs.

V. CONCLUSION

In this paper, a technique to attain the wide bandwidth LNA is presented using 0.18 μ m CMOS technology. The introduced technique tunes-out the parasitic capacitances of the transistors

over a wide bandwidth. The relations of the components to the standard form of the Butterworth filter are calculated to get the desired gain-flatness. The number of inductors are minimized to reduce the loss associated with them. Using this technique, a single stage wideband LNA is obtained with a low power consumption.

VI. ACKNOWLEDGMENT

The authors would like to thank MediaTek Inc. Singapore, for their support in this work and Chartered Semiconductor Manufacturing Singapore, for chip implementation. They would also like to thank Lim Wei Ming, for his help in the measurement.

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